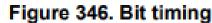
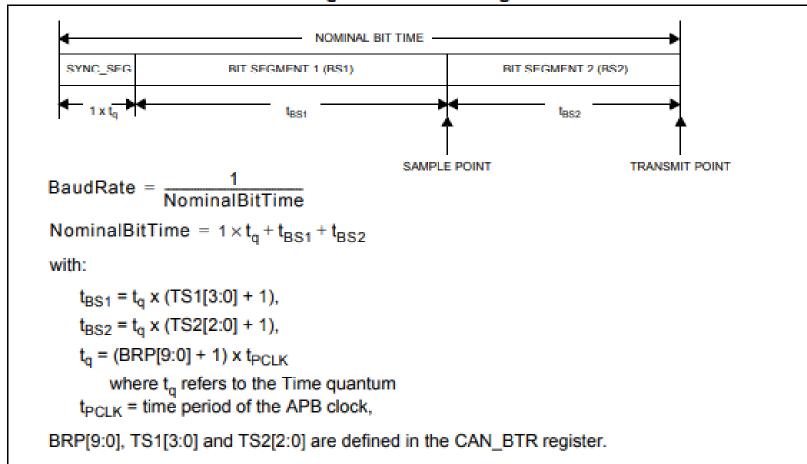
CAN transmission

• Enable the clock for the CAN module. (**RCC_APB1ENR**). Set the CAN1EN and CAN2EN with logical 1 according to your test mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UART8 EN	UART7 EN	DAC EN	PWR EN	Reser- ved	CAN2 EN	CAN1 EN	Reser- ved	I2C3 EN	I2C2 EN	I2C1 EN	UART5 EN	UART4 EN	USART 3 EN	USART 2 EN	Reser- ved
rw	rw	rw	rw		rw	rw	-	rw	e	rw	rw	rw	rw	rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI3 EN	SPI2 EN	Rese	Reserved		Reserved		TIM14 EN	TIM13 EN	TIM12 EN	TIM7 EN	TIM6 EN	TIM5 EN	TIM4 EN	TIM3 EN	TIM2 EN
rw	rw			rw			rw	rw	rw	rw	rw	rw	rw	rw	rw

• Calculate the bitrate through the BTR registers. (*Bit Timing Register*) Doing some calculations according to our datasheet.





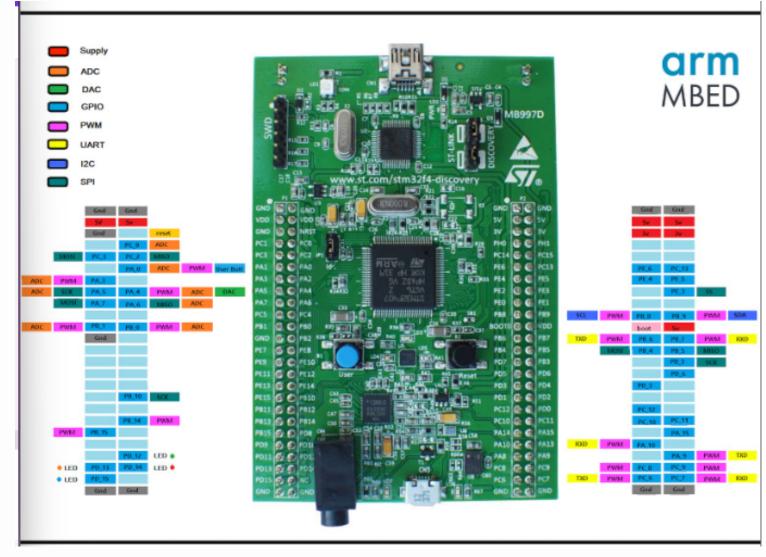
• Configurate the mode test of the CAN controller. It could be: normal, loopback, sleep.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
SILM	LBKM		Rese	unuad.		SJW[1:0] Re		Res.	TS2[2:0]			TS1[3:0]					
rw	rw		rvese	aveu		rw	rw		rw	rw	rw	rw	rw	rw	rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	Description							BRP[9:0]									
	Reserved						rw	rw	ΓW	rw	rw	ΓW	rw	rw	rw		

• Configurate the mode test of the CAN controller. It could be: normal, loopback, sleep.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	SILM	LBKM		Rese	nund		SJW[1:0]		Res.	TS2[2:0]			TS1[3:0]				
	ΓW	rw		rvese	aveu		rw	rw		rw	rw	rw	ΓW	rw	rw	rw	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Reserved										BRP	[9:0]					
								rw	rw	ΓW	rw	rw	ΓW	rw	rw	rw	

 Configure the pin associated with CAN.
Basically, we have to see the pinout of our model and find the RX and TX pines.



Frame prepare

- Prepare the data that is going to be sent in the frame.
- Configure the ID of the frame, determine the priority of CAN bus.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
	STID[10:0]/EXID[28:18]												EXID[17:13]						
rw	rw	rw	ΓW	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	ΓW	rw				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
					E	EXID[12:0]						IDE	RTR	TXRQ				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw				

Bits 31:21 STID[10:0]/EXID[28:18]: Standard identifier or extended identifier

The standard identifier or the MSBs of the extended identifier (depending on the IDE bit value).

Bits 20:3 EXID[17:0]: Extended identifier

The LSBs of the extended identifier.

Bit 2 **IDE**: Identifier extension

This bit defines the identifier type of message in the mailbox.

- 0: Standard identifier.
- 1: Extended identifier.

Bit 1 RTR: Remote transmission request

- 0: Data frame
- 1: Remote frame

Frame transmission

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	TIME[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	ΓW	rw	rw	rw	ΓW	rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Reserved								Rese	nund		DLC[3:0]				
reserved							rw		rvese	aveu		rw	rw	rw	rw	

- Write the register data that is suitable for the CAN controller
- Configure the length of the frame.
- Configure the ID frame.
- Initialize the transmission.

Bits 31:16 TIME[15:0]: Message time stamp

This field contains the 16-bit timer value captured at the SOF transmission.

Bits 15:9 Reserved, must be kept at reset value.

Bit 8 TGT: Transmit global time

This bit is active only when the hardware is in the Time Trigger Communication mode, TTCM bit of the CAN_MCR register is set.

0: Time stamp TIME[15:0] is not sent.

1: Time stamp TIME[15:0] value is sent in the last two data bytes of the 8-byte message: TIME[7:0] in data byte 7 and TIME[15:8] in data byte 6, replacing the data written in CAN_TDHxR[31:16] register (DATA6[7:0] and DATA7[7:0]). DLC must be programmed as 8 in order these two bytes to be sent over the CAN bus.

Bits 7:4 Reserved, must be kept at reset value.

Bits 3:0 DLC[3:0]: Data length code

This field defines the number of data bytes a data frame contains or a remote frame request. A message can contain from 0 to 8 data bytes, depending on the value in the DLC field.

Data transmission

- Uses a lossless bitwise arbitration method of contention resolution.
- CAN specifications use the terms *dominant* (0) and *recessive* (1) bits.

	Start	ID bits											The rest
	bit	10	9	8	7	6	5	4	3	2	1	0	of the frame
Node 15	0	0	0	0	0	0	0	0	1	1	1	1	
Node 16	0	0	0	0	0	0	0	1		g			
CAN data	0	0	0	0	0	0	0	0	1	1	1	1	