REFERENCE MANUAL: STM32F103C8T6, *STM32F407G-DISC1

By: Michelle Cámara González

Processor: *ARM* Cortex-M3 with embedded Flash and SRAM.

Crystal Oscillator: *HSE* 4-16 MHz Crystal/ceramic resonator oscillator.

SRAM: 20 Kbytes.

Debug mode: Serial wire debug (SWD) and JTAG interfaces

I/O:

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage(2)	TTL ports	–0.5		0.8	V
V_{IH}	IO TC input high level voltage(2)		2		V_{DD}+0.5	
	IO FT high level voltage(2)		2		5.5V	
V_{IL}	Input low level voltage(2)	CMOS ports	–0.5		0.35 V_{DD}	V
V_{IH}	Input high level voltage(2)		0.65 V_{DD}		V_{DD}+0.5	
V_{hys}	IO TC Schmitt trigger voltage hysteresis(3)			200		mV
	IO TC Schmitt trigger voltage hysteresis(3)			5% V_{DD}(4)		mV
I_{lkg}	Input leakage current (5)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os			±1	µA
		V_{IN}= 5 V 5 V tolerant I/Os			3	
R_{PU}	Weak pull-up equivalent resistor(6)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	$V_{IN} = V_{DD}$	30	40	50	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. V_{DD} = 3.3 V, T_A = -40 to 105 °C unless otherwise specified.
2. Values based on characterization results, and not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. With a minimum of 100 mV.
5. Leakage could be higher than max. if negative current is injected on adjacent pins.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Table 30. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time		V_{DD}–0.4		
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time		2.4		
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V		1.3	V
V_{OH} (2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time		V_{DD}–1.3		
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V		0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time		V_{DD}–0.4		

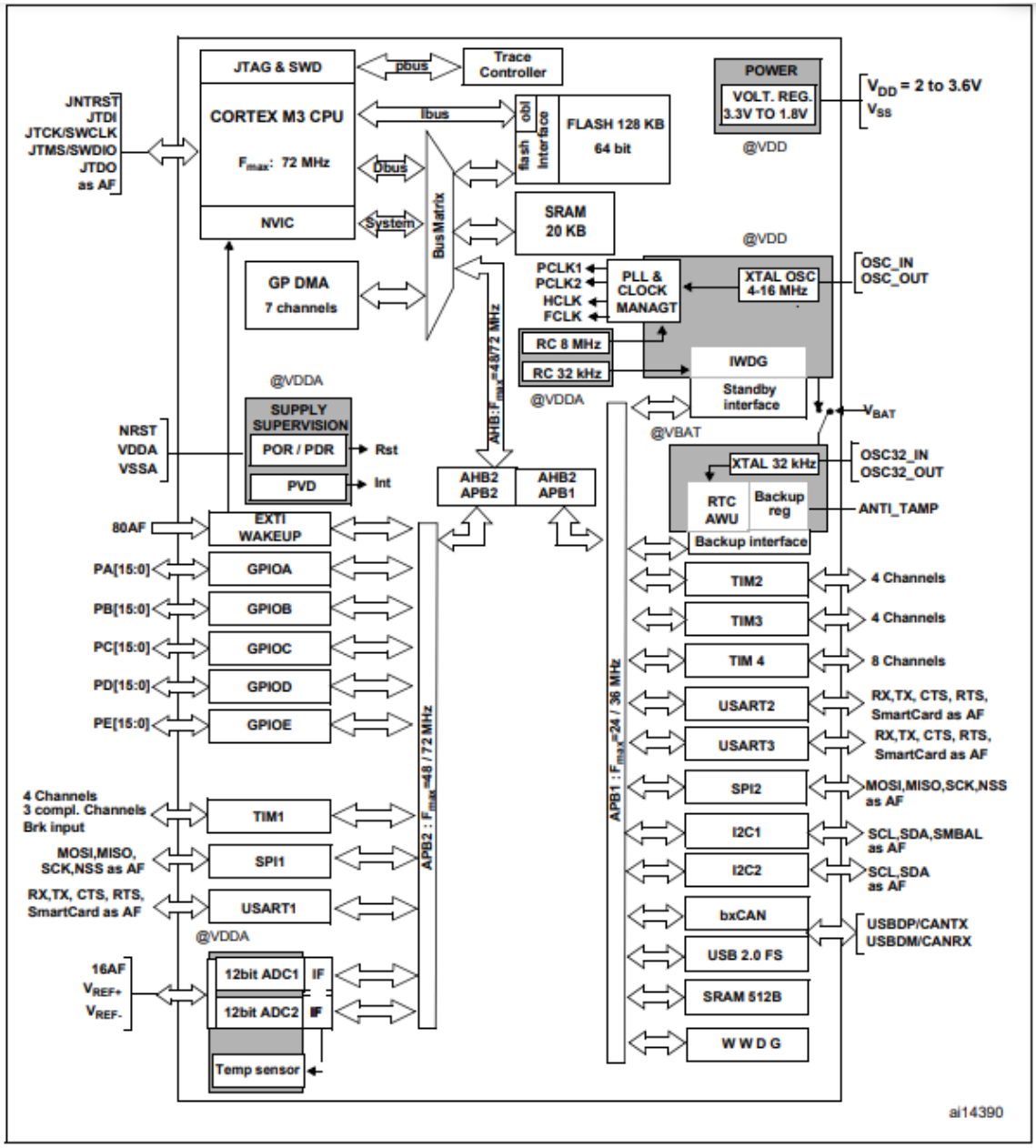
1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 5* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 5* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 31. I/O AC characteristics(1)

I/O mode(1)	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		2	MHz
	$t_{f(IO)out}$	Output high to low level fall time(3)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		125	ns
	$t_{r(IO)out}$	Output low to high level rise time(3)			125	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		10	MHz
	$t_{f(IO)out}$	Output high to low level fall time(3)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		25	ns
	$t_{r(IO)out}$	Output low to high level rise time(3)			25	
11	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		20	MHz
	$t_{f(IO)out}$	Output high to low level fall time(3)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12	
	$t_{r(IO)out}$	Output low to high level rise time(3)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10		ns

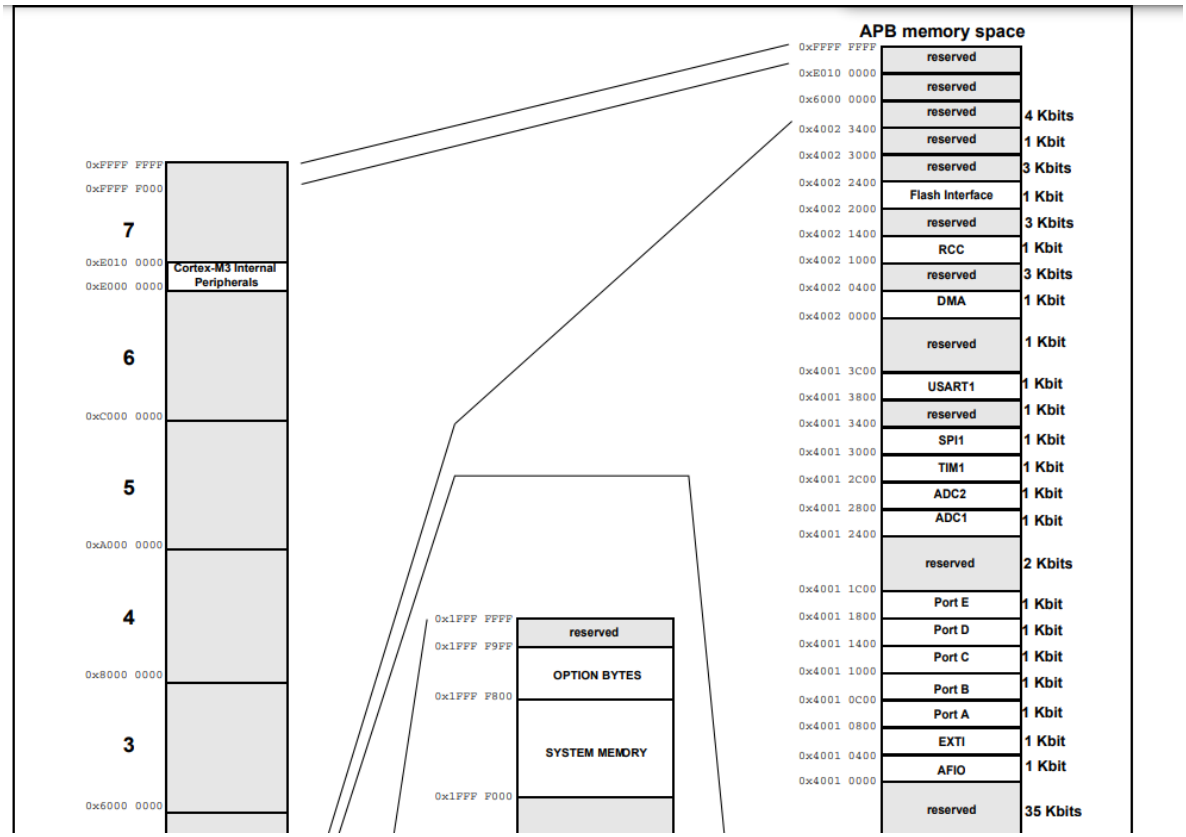
1. Refer to the Reference user manual UM0306 for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 16*.

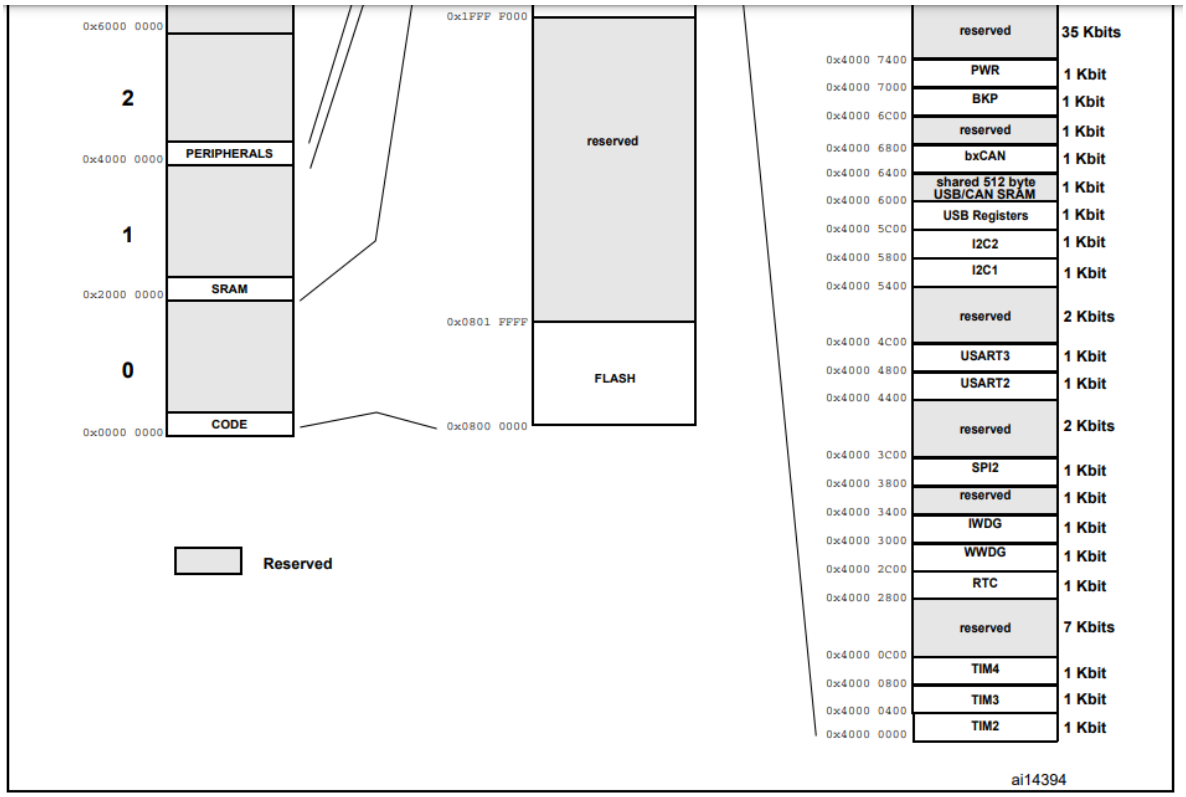
BLOCK DIAGRAM:



1. T_A = –40 °C to +105 °C (junction temperature up to 125 °C).
2. AF = alternate function on I/O port pin.

Memory Map:


APB memory space
0xFFFF FFFF
0xFFFF F000
7
0xE010 0000
0xE000 0000
Cortex-M3 Internal Peripherals
6
0xC000 0000
5
0xA000 0000
4
0x8000 0000
3
0x6000 0000
0x1FFF FFFF
0x1FFF F9FF
reserved
0x1FFF F800
OPTION BYTES
SYSTEM MEMORY
0x1FFF F000
0xFFFF FFFF
0xE010 0000
0x6000 0000
0x4002 3400
0x4002 3000
0x4002 2400
0x4002 2000
0x4002 1400
0x4002 1000
0x4002 0400
0x4002 0000
0x4001 3C00
0x4001 3800
0x4001 3400
0x4001 3000
0x4001 2C00
0x4001 2800
0x4001 2400
0x4001 1C00
0x4001 1800
0x4001 1400
0x4001 1000
0x4001 0C00
0x4001 0800
0x4001 0400
0x4001 0000
reserved
4 Kbits
reserved
1 Kbit
reserved
3 Kbits
Flash Interface
1 Kbit
reserved
3 Kbits
RCC
1 Kbit
reserved
3 Kbits
DMA
1 Kbit
reserved
1 Kbit
USART1
1 Kbit
reserved
1 Kbit
SPI1
1 Kbit
TIM1
1 Kbit
ADC2
1 Kbit
ADC1
1 Kbit
reserved
2 Kbits
Port E
1 Kbit
Port D
1 Kbit
Port C
1 Kbit
Port B
1 Kbit
Port A
1 Kbit
EXTI
1 Kbit
AFIO
1 Kbit
reserved
35 Kbits



MEMORY MAP

1. What's the base address of AHB1 Bus Peripherals?
   - 0x4002 0000
2. What's the base address of RCC engine registers of the MCU?
   - 0x4002 1000
3. What's the base address of APB1 Peripherals?
   - 0x4000 0000
4. What's the base address of SRAM2?
   - 0x2000 0000
5. What's the base address of ADC registers?
   - 0x4001 2400 – ADC1
   - 0x4001 2800 – ADC2

BLOCK DIAGRAM

1. System Bus can operate at the speed up to 180 MHz?
   - False it cannot operates because it has a maximum speed of 72 MHz.
2. SRAMS are connected to System Bus T/F?
   - True.
3. APB1 bus can operate at the speed up to 180 MHz?

- No, it cannot operate at speeds of up to 180 MHz. The maximum speed of it is 36 MHz.

4. Let's say I have a peripheral whose datasheet says that its operating frequency or speed must be Above 95 MHz, can I connect that peripheral via APB2 Bus?
    - No due to the maximum APB2 frequency.
5. What is the MAX HCLK value of your MCU?
    - 72 MHz
6. What is the MAX P1CLK (APB1) value of your MCU?
    - 36 MHz
7. What is the MAX P2CLK (APB2) value of your MCU?
    - 72 MHz.
8. GPIOs and processor communicate over AHB1 bus T/F?
    - True. Because the GPIO Block is directly connected to AHB1 bus.
9. USB OTG and processor communicate over AHB2 bus T/F?
    - False. USB OTG and other high-speed peripherals are connected to AHB1 bus.

GLOSSARY

- **ARM:** *Advanced RISC Machine*. It refers to a Reduced Instruction Set Computing (RISC) architecture developed by ARM Holdings. It is widely used in the design of microcontrollers and processors for embedded systems.

- **SWD:** *Serial Wire Debug*. It is a debugging and programming protocol used in embedded systems for communication between a development device and a microcontroller or processor.

- **ITM:** *Instrumentation Trace Macrocell.* It is a feature used in debuggers to trace events and provide additional information during software development in embedded systems.

- **JTAG:** *Joint Test Action Group*. It refers to a standard test interface used for debugging and programming microcontrollers and other electronic devices.

- **FIFO:** *First In, First Out*. It refers to a data structure that follows the principle that the first element to enter is the first to be removed.

- **HSE:** *High-Speed External.* It is used in the context of an external oscillator with ad adjustable frequency between 4 and 16 megahertz.

- **SRAM:** *Static Random Access Memory.* It is a type of volatile memory used to store and access data quickly in embedded systems.

- **POR:** *Power-On Reset.* It refers to a circuit that generates a reset pulse when the system is powered on.

- **PDR:** *Power-Down Reset.* Like POR, it refers to a circuit that generates a reset pulse when the system is powered down or enters a low-power mode.

- **PVD:** *Programmable Voltage Detector.* It refers to a programmable voltage detector that generate a reset or an interrupt when the supply voltage falls below a set threshold.
- **MCU:** *Microcontroller Unit.* A microcontroller is an integrated circuit that includes a central processing unit (CPU), memory and input/output peripherals.