Gen6 F2 Touch Controller

ASIC Specification

IC-DS-220825

v1.2

May 9, 2023

Prepared By:	J. Baldwin
Reviewer Approval:	J. Bertrand
Release Approval:	P. Vincent

This document describes the Gen6 F2 1p3 series Cirque capacitive touch controllers. The “x’s” in the part number are based on ordered configuration. Sample hardware and firmware are available upon request.

Part Numbers:

- QFN64 “Olympus”: 10-02A1A3-XXX
- QFN42 “Timp”: 10-02F1A3-XXX

Document Revision History

Date	Version Number	Description
AUGUST 2022	v1.0	Initial release
DECEMBER 2022	v1.1	Added Section 9: Explanation of tBuf requirement
MAY 2023	v1.2	Corrected GPIO pin type details

Table 1: Document Revision History

Copyright and Patent Information

Table of Contents

Gen6 Platform Summary

The Gen6 touch controller family features the latest evolution of Cirque's precision capacitive sensing technology. Designed for high flexibility and performance, Gen6 touch controllers can be utilized for various trackpad, touch screen and proximity sensing applications.

Key Features

- Mutual and self-capacitive sensing modes.
- Full image sensing with multi-touch.
- Flexible Analog System:
  - 16 custom ADC channels.
  - Wide range and channel specific gain and offset control.
  - Dedicated driven shield for self-capacitance modes.
- CPU:
  - 32-bit RISC.
- Analog Co-processor with DSP:
  - Provides image pre-processing for reduced CPU load, or direct high-speed connection to the AFE for development flexibility.
- Memory:
  - Flash: 128 KB + 2 KB secure boot capable.
  - RAM: 12 KB + 4 KB.
  - In-circuit programmable.
- Interfaces:
  - I²C (standard, fast and fast mode plus)
  - GPIO.
  - Dual UART.
  - PS2

Gen6 ASIC Family

- **Gen6** (QFN64 "Olympus"):
  - 48 programmable TX/RX electrodes, 16 ADCs.
  - 6 electrodes can be configured as dedicated button inputs.
  - Up to 9 GPIO (with PWM) in addition to dedicated I²C.
  - Multi-IC sync enables large touch panel support.

- **Gen6s** (QFN42 "Timp"):
  - 30 programmable TX or RX electrodes, 16 ADCs.
  - 6 electrodes can be configured as dedicated button inputs.
  - Up to 4 GPIO (with PWM) in addition to dedicated I²C.

Electrical & Mechanical Details

- Main supply: 2.7 – 3.6V.
- Interface supply: 1.8 – 3.6V.
- Environmental:
  - Operating Temp: -25 to 85° C.
  - Storage Temp: -40 to 125° C.
- Gen6 QFN64 physical dimensions:
  - 7x7x0.55mm.
- Gen6s QFN42 physical dimensions:
  - 4.5x4.5x0.55mm

Firmware Features

- Microsoft Precision Touchpad (PTP) support.
- Multi-touch tracking.
- Palm detection and rejection.
- Advanced moisture and noise immunity.
- Dynamic power management.
- Supports optional pointing stick.

Development Tools

- Various Arduino-based development kits and sample code available.
- Cirque TouchTools3 software for quick and easy configuration and testing of capacitive sensors.
- All parts contain an I²C bootloader. The bootloader can be used to easily load specific firmware into the device.

Application Examples

- The Gen6 platform supports various implementation configurations, including:
  - NotePC PTP trackpads.
  - General purpose trackpads.
  - Game controllers
  - Touch screens
  - Trackpads + self-capacitive buttons
  - Trackpads + proximity sensing

- Proximity Sensing

1. Introduction and Features

1.1. Feature Highlights

- 48 configurable drive/sense channels (QFN64 Olympus 7x7x0.5mm)
- 30 configurable drive/sense channels (QFN42 Timp 4.5x4.5x0.5mm)
- All new analog design for high SNR in harsh environments.
- Multi-core architecture combines a 32-bit RISC CPU with a dedicated analog coprocessor enabling advanced touch detection and auto compensation algorithms.
- Wide range gain and offset controls for enhanced flexibility.
- Multi-IC sync for large touch panel or large trackpad support.
- Gen6 firmware platform includes advanced compensation, multi-finger tracking and native Microsoft PTP support.

1.2. Block Diagrams

1.2.1. Gen6 Block Diagram

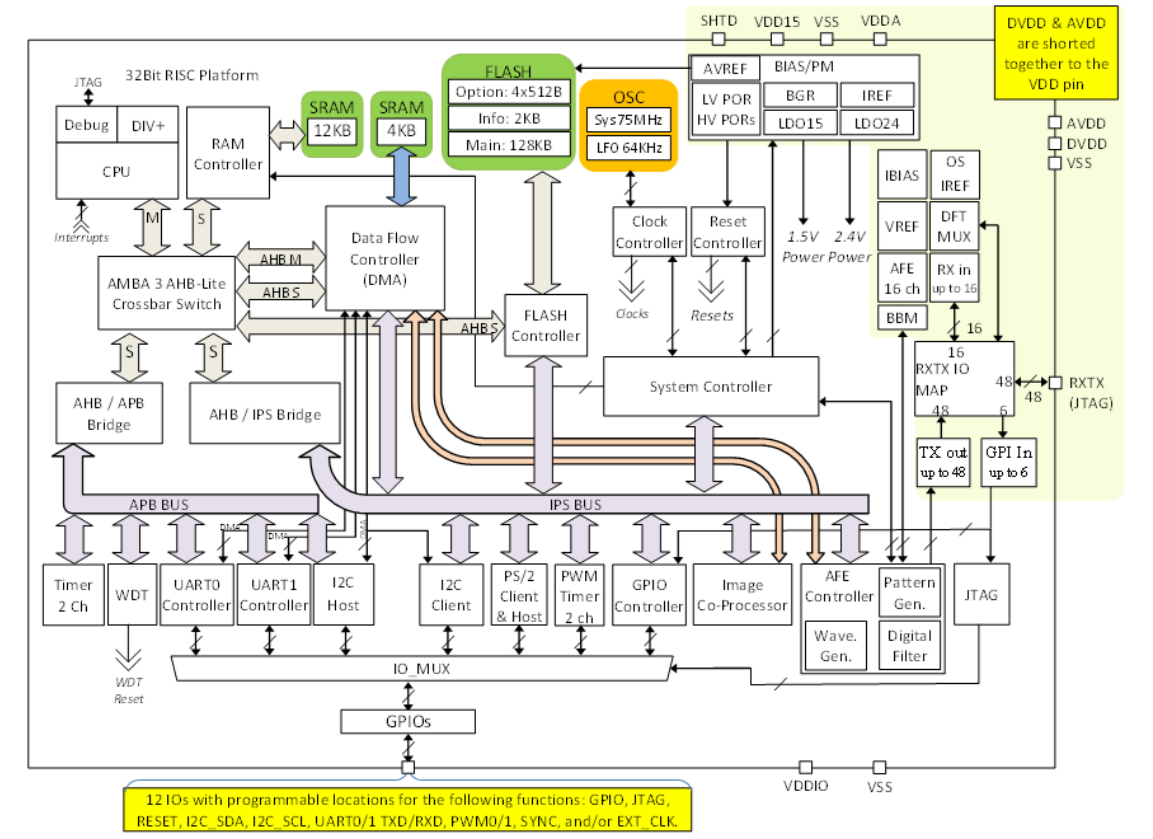


Figure 1: Gen6 Touch Controller Block Diagram

1.2.2. Typical Implementation Diagrams

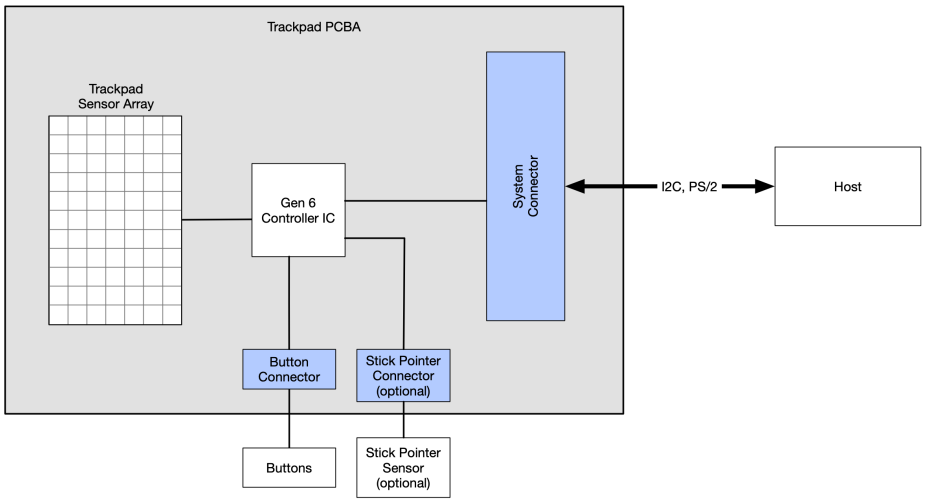


Figure 2: Touchpad Implementation Example Block Diagram

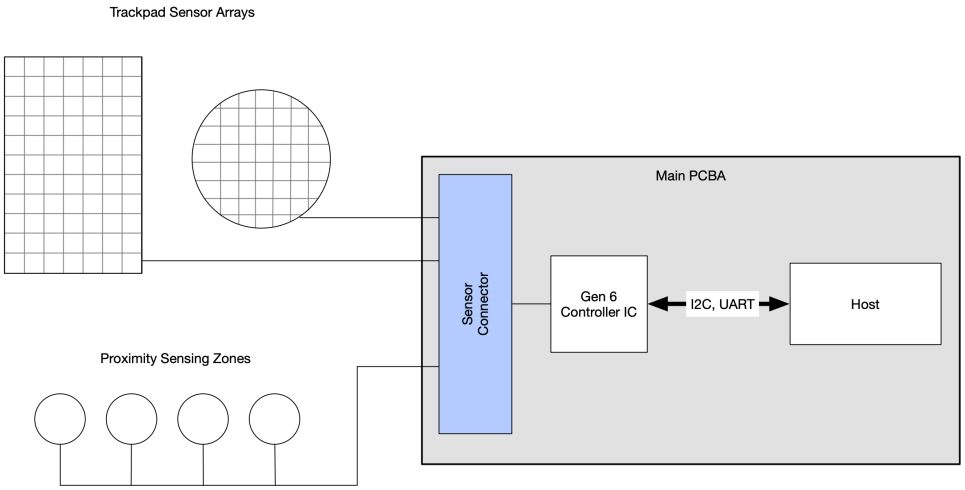


Figure 3: Game Controller Implementation Example Block Diagram

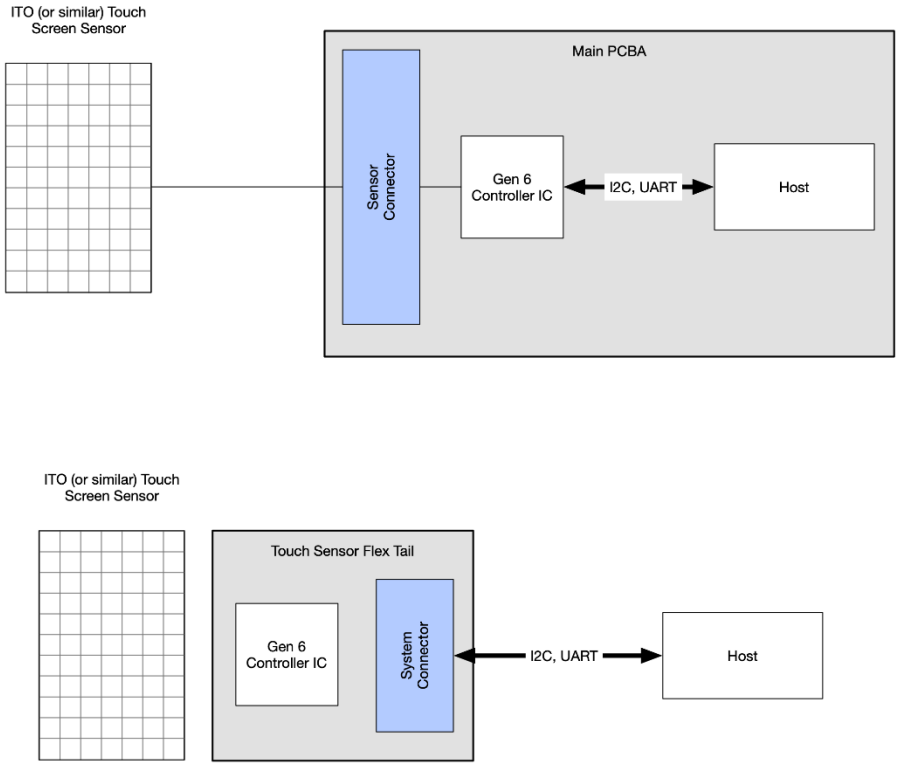


Figure 4: Touch Screen Example Implementation Block Diagram

2. Pin Out Details

2.1. QFN64 "Olympus" Pin Assignments

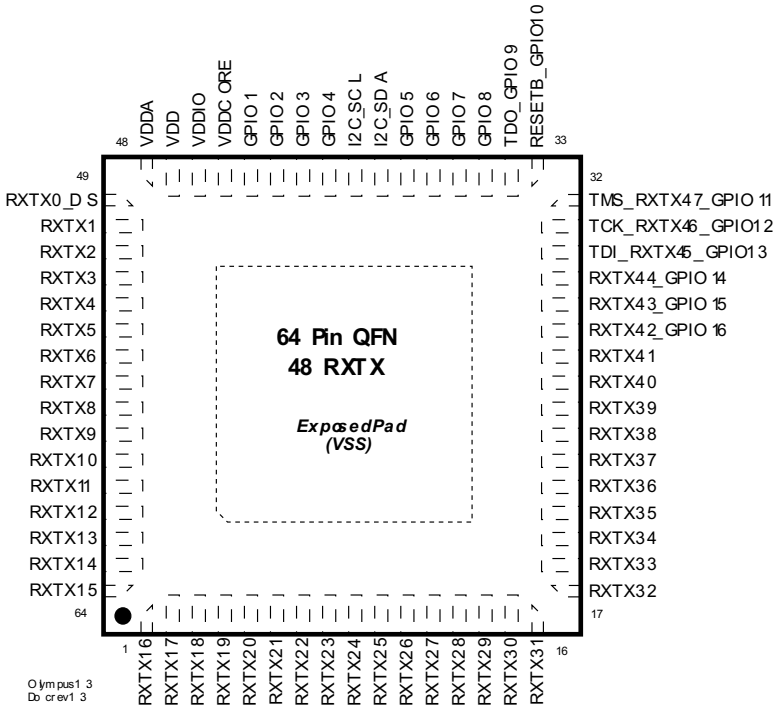


Figure 5: Olympus QFN64 Pin Assignment Diagram

Pin Numbers	Pin Names	Type	Description
1 – 26	RXTX16 – RXTX41	IN/OUT	Sensor connection to AFE (configurable TX or RX)
27 – 29	RXTX42_GPI16 – RXTX44_GPI14	IN	Sensor connection to AFE (configurable TX or RX), configurable as general-purpose input (3.3V only)
30	RXTX45_GPI13_TDI	IN	Sensor connection to AFE (configurable TX or RX), configurable as general-purpose input (3.3V only) or JTAG programming pin.
31	RXTX46_GPI12_TCK	IN	Sensor connection to AFE (configurable TX or RX), configurable as general-purpose input (3.3V only) or JTAG programming pin.
32	RXTX47_GPI11_TMS	IN	Sensor connection to AFE (configurable TX or RX), configurable as general-purpose input (3.3V only) or JTAG programming pin.
33	RESET_B_GPIO10	IN/OUT	System Reset. Defaults as a system reset input (active low) or programmable as general-purpose input/output.
34	TDO_GPIO9	IN/OUT	JTAG programming pin or optional general-purpose input/output.
35 – 38	GPIO8 – GPIO5	IN/OUT	General-purpose input/output with PWM.
39	I2C_SDA	IN/OUT	I²C slave/master data input/output

Pin Numbers	Pin Names	Type	Description
40	I2C_SCL	IN/OUT	I²C slave/master clock input/output
41 – 44	GPIO4 – GPIO1	IN/OUT	General-purpose input/output with PWM
45	VDDCORE	POWER	Digital core power rail. LDOCORE output. 1.514V typical. **NOTE:** VDDCORE requires a 1.0µF bypass capacitor to VSS.
46	VDDIO	POWER	Interface power supply (I/O voltage). **NOTE**: VDDIO requires 0.1 µF bypass capacitor to VSS.
47	VDD	POWER	Main supply. **NOTE**: VDD requires 4.7 µF + 0.1µF bypass capacitor to VSS.
48	VDDA	POWER	ADC power rail. LDOA output. 2.90V typical **NOTE:** VDDA requires a 1.0µF bypass capacitor to VSS.
49	RXTX0_DS	IN/OUT	RX0 (AD0), TX0, or Driven Shield output. Sensor connection to AFE (configurable TX or RX). Unique driven shield capability that means it may be programmed as a *low impedance* connection to the Driven Shield buffer for improved self-capacitance shielding. Note: all pins can be configured for driven shield but this pin can be improved driven shield due to its low impedance connection.
50 – 64	RXTX1 – RXTX15	IN/OUT	Sensor connection to AFE (configurable TX or RX).
EP	VSS	GND	Exposed pad, VSS, must be connect to ground.

Table 2: Pin Assignments for Olympus QFN64

2.2. QFN42 "Timp" Pin Assignments

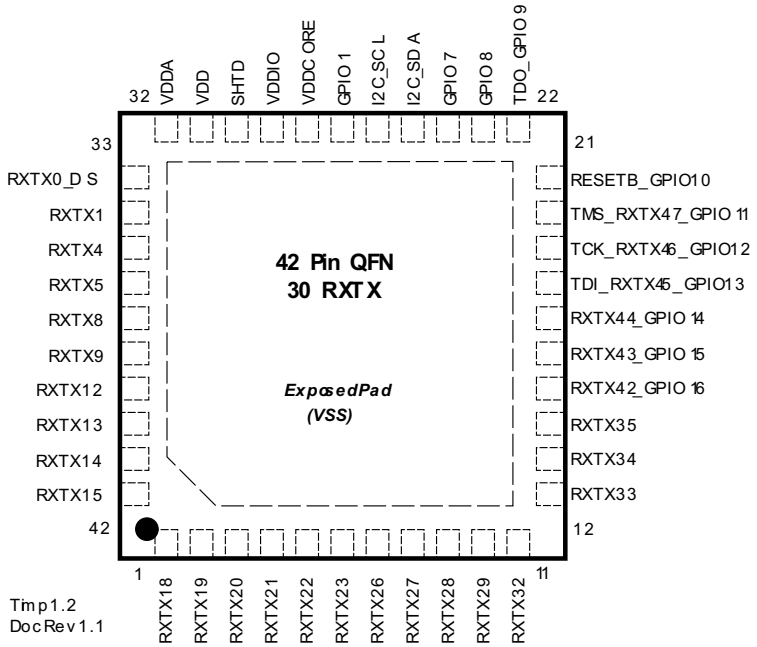


Figure 6: Timp QFN42 Pin Assignment Diagram

Pin Numbers	Pin Names	Type	Description
1 – 14	RXTX18 – RXTX35	IN/OUT	Sensor connection to AFE (configurable TX or RX)
15 – 17	RXTX42_GPI16 – RXTX44_GPI14	IN	Sensor connection to AFE (configurable TX or RX), configurable as general-purpose input (3.3V only)
18	RXTX45_GPI13_TDI	IN	Sensor connection to AFE (configurable TX or RX), configurable as general-purpose input (3.3V only) or JTAG programming pin.
19	RXTX46_GPI12_TCK	IN	Sensor connection to AFE (configurable TX or RX), configurable as general-purpose input (3.3V only) or JTAG programming pin.
20	RXTX47_GPI11_TMS	IN	Sensor connection to AFE (configurable TX or RX), configurable as general-purpose input (3.3V only) or JTAG programming pin.
21	RESET_B_GPIO10	IN/OUT	System Reset. Defaults as a system reset input (active low) or programmable as general-purpose input/output.
22	TDO_GPIO9	IN/OUT	JTAG programming pin or optional general-purpose input/output.
23 – 24	GPIO8 – GPIO7	IN/OUT	General-purpose input/output with PWM.
25	I2C_SDA	IN/OUT	I²C slave/master data input /output
26	I2C_SCL	IN/OUT	I²C slave/master clock input / output with PWM
27	GPIO1	IN/OUT	General-purpose input/output with PWM.
28	VDDCORE	POWER	Digital core power rail. LDOCORE output. 1.514V typical. **NOTE:** VDDCORE requires a minimum 1.0µF bypass capacitor to VSS.
29	VDDIO	POWER	Interface power supply (I/O voltage). **NOTE:** VDDIO requires a minimum 0.1µF bypass capacitor to VSS.
30	SHTD	IN	Active High Shutdown input pin. Connect to GND when not used.
31	VDD	POWER	Main supply. **NOTE:** VDD requires a minimum 4.7µF bulk + minimum 0.1µF bypass capacitor to VSS.
32	VDDA	POWER	ADC power rail. LDOA output. 2.90V typical. **NOTE:** VDDA requires a minimum 4.7µF bulk + minimum 0.1µF bypass capacitor to VSS.
33	RXTX0_DS	IN/OUT	RX0 (AD0), TX0, or Driven Shield output. Sensor connection to AFE (configurable TX or RX). Unique driven shield capability means it may be programmed as a low impedance connection to the Driven Shield buffer for improved self-capacitance shielding. Note: all pins can be configured for driven shield, but this pin can be improved driven shield due to its low impedance connection.
34 – 42	RXTX1 – RXTX15	IN/OUT	Sensor connection to AFE (configurable TX or RX).
EP	GND	GND	Exposed pad, connect to ground.

Table 3: Pin Assignments for Timp QFN42

3. Electrical Specification

This section describes the maximum ratings, operating conditions, and other key electrical details of the Gen6 touch controller family.

3.1. Key Technical Details

Item	Specification	Notes
Touch Sensing System:	Custom mutual/self-capacitance analog front end with 16 ADC channels	The system supports self-cap, mutual cap, or a combination of the two.
Touch Sensing Electrode Channels:	**QFN64:** 48 configurable RX/TX	6 electrodes can be configured as dedicated button inputs. Each electrode can be an RX (with a connection to an A/D), a TX, ground, or floating.
	QFN42: 30 configurable RX/TX	
Host Interface:	I²C, PS/2, Serial UART	
GPIO:	**QFN64:** 9 GPIO with PWM support plus 6 electrodes configurable as button inputs.	Schmitt input, push-pull, three-state output (I / F power) LED drive support (PWM: 2ch, assignable to one of 3 ports)
	QFN42: 4 GPIO with PWM support plus 6 electrodes configurable as button inputs.	
Programming Interface:	JTAG or I²C in-circuit.	Parts come with Cirque I²C bootloader already installed.
CPU Core:	32-bit RISC 37.5 MHz	
Memory:	Flash: 128 KB + 2 KB secure boot capable. RAM: 16 KB + 4 KB	

Table 4: Gen6 Key Technical Details

3.2. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{DD}	Main Supply Voltage	-0.3	3.6	V	
V_{DDIO}	Interface Supply (I/O Supply)	-0.3	3.6	V	
V_{DDA}	ADC Supply	-0.3	V_{DD} + 0.3 3.6 Max	V	
V_{AIN}	Input Voltage (analog)	-0.3	V_{DD} + 0.3	V	
V_{DIN}	Input Voltage (digital)	-0.3	V_{DDIO} + 0.3	V	
V_{HBM}	ESD HBM	-	2	kV	
V_{CDM}	ESD CDM	-	750	V	
T_{stg}	Storage Temp	-40	125	°C	
H_{stg}	Storage Humidity	5	95	% RH	Non-condensing

Table 5: Gen6 Absolute Maximum Ratings

3.3. Operating Conditions

3.3.1. Operating Condition Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{DD}	Main Supply Voltage	3.1/2.7 (see note)	3.3	3.6	V	Minimum operating voltage may go down to 2.7 if V_{DDA} is tied to VDD and LDOA is disabled.
V_{DDIO}	Interface Supply Voltage	1.71 (see note)	1.8	V_{DD}	V	Usually tied to V_{DD} (typically 3.3V). Alternatively, V_{DDIO} can connect to voltages down to 1.8V
V_{DDA}	ADC Supply Voltage	2.7	2.90	V_{DD} + 0.3 3.6 Max	V	Usually powered from LDOA.
T_{opr}	Operating Temp	-25	-	85	°C	
H_{opr}	Operating Humidity	5		95	% RH	Non-condensing

Table 6: Gen6 Operating Conditions

3.3.2. Recommended Mutual Cap Sensor Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
C_{TR}	TX – RX capacitance	0.3	-	1.3	pF	Capacitance from transmit to receive (offset) under typical ASIC operating conditions. Minimize this for best performance
ΔC_{TR}	TX – RX capacitance change	60	-	300	fF	Peak change in transmit to receive capacitance with finger directly over XY junction. Maximize this for best performance
C_{TG}	TX – GND capacitance	-	30	60	pF	Includes parasitic capacitance. Minimize this for best performance
C_{RG}	RX – GND capacitance	-	30	60	pF	Includes parasitic capacitance. Minimize this for best performance.

Table 7: Gen6 Mutual Cap Sensor Characteristics

3.3.3. Power Consumption Specifications

Power consumption is dependent on the specific firmware codebase being used and the implementation for a specific product. Several examples are shown below, (examples shown below are tested at room temperature using a 3.3V supply):

Typical Touchpad Implementation - GlidePoint PTP Firmware (Borax v2.12)

Symbol	Parameter	Typical	Unit	Notes
$I_{SCANNING}$	Current Consumption	16.3	mA	Full-speed scanning, no finger being tracked
$I_{TRACKING}$		16.8	mA	Full-speed scanning, finger present and tracking
I_{IDLE1}		3.2	mA	Polling, after 5 seconds of no finger contact
I_{SLEEP}		0.5	mA	No scanning, Lid closed or SetPowerOFF

Table 8: Gen6 Power Consumption running GlidePoint PTP firmware

Typical Proximity Sensor Implementation – CustomMeas Firmware (Ver 8A87)

Symbol	Parameter	Typical	Unit	Notes
$I_{SCANNING}$	Current Consumption	6.63	mA	LPM = Disabled, 100 fps, 6 measurements
I_{IDLE1}		5.01	mA	LPM = Enabled, target 100 fps (90 fps actual), 6 measurements per frame.
I_{SLEEP}		0.100	mA	Scanning halted.

Table 9: Gen6 Power Consumption running CustomMeas firmware

3.3.4. Power State Definitions

The power states mentioned above use the following definitions:

Scanning/Tracking
The IC is making measurements using the fastest possible scan (or the requested scan rate). For touchpad applications the measurements are being monitored for finger activity. In this mode the latency is lowest, but the power consumption is highest. The system is in Scanning Mode whenever it is tracking a finger.

Idle
In Idle mode, the device enters a lower power state where most activity is suspended. For touchpad applications the device will periodically resume activity, enter the high-power state, and check if the pad has been touched. If this polling does not detect the touch the system will re-enter the low power state again. This polling interval is configurable.

Idle mode occurs after an identified period of inactivity. The device will go into idle mode if the pad has not been touched for a period longer than the specified time out. This period can vary depending on implementation (values typically range from <1 second to 10 seconds).

Sleep
Sleep mode enters a very low power state where all activity is suspended. The device can enter sleep mode after a specified timeout. The device can also enter sleep mode when the Host sets the Disable signal on the touchpad module.

3.4. Electrical Characteristics

NOTE: Hereafter, unless otherwise noted, Topr = 25°C, and VDD, VDDIO = 3.3V

3.4.1. Regulator Specification

Values shown are for factory trimmed regulators. Firmware configurations may change these values.

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
LDOCORE	Core regulator output voltage	1.45	1.514	1.55	V	Regulator from VDD supply. Ties to V_{DDCORE}.
LDOA	ADC regulator output voltage	2.86	2.90	2.98	V	Regulator from V_{DD} supply. Connected to V_{DDA}. Can be disabled and an external voltage applied for lower voltage operation.
V_{OLDOA}	Regulator overhead voltage	200			mV	VDD – V_{OLDOA} must be > LDOA to maintain ADC performance.

Table 10: Regulator Specification

3.4.2. Power-On-Reset

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
Vrelease	Reset Release Voltage	1.255	1.32	1.4	V	Reset is monitoring LDOCORE
Vreset	Reset Voltage	1.10	1.25	1.35	V	
T_{hys}	Hysteresis Width	0.06	0.11	0.16	V	

Table 11: Power-On-Reset Characteristics

3.4.3. Built-in Oscillator Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
f_{75M}	Oscillation Frequency	71.7	73.5	75.5	MHz	
T_{F75M}	Temperature coefficient	See Figure 6			Hz/°C	Temp range

Table 12: Gen6 Oscillator Specification

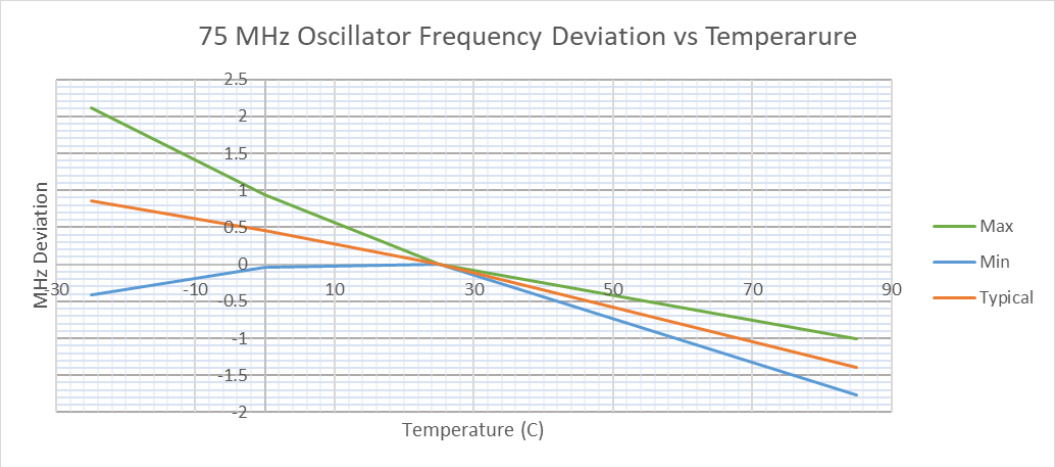


Figure 7: Oscillator Frequency Deviation vs. Temp

3.4.4. Typical Signal Detection Performance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
C_{FINGER}	Finger touch sensitivity	60 @ >40dB	100 @ >48dB	-	fF	Mutual cap mode. Nominal finger size ø 10 mm
C_{PROX}	Proximity sensitivity	10 @>12dB	40 @>24dB	460 @>48dB	fF	Self-cap mode.

Table 13: Gen6 Signal Detection Specification

3.4.5. Flash Memory Specification

Parameter	Minimum	Typical	Maximum	Unit	Notes
Endurance	100k	-	-	cycles	
Data Retention	10	-	-	years	100k cycles at T_{opr}
Erase Unit size	0.5	2	128	KB	

Table 14: Gen6 Flash Memory Characteristics

3.4.6. I2C Mode GPIO Terminal Characteristics

Symbol	Item	Standard Mode 100 kbit/s max		Fast Mode 400 kbit/s max		Fast Mode Plus 1 Mbit/s max		Unit	Notes
		Min	Max	Min	Max	Min	Max		
V_{IL}	Input voltage, LOW level	-0.3	$0.3*V_{DDIO}$	-0.3	$0.3*V_{DDIO}$	-0.3	$0.3*V_{DDIO}$	V	
V_{IH}	Input voltage, HIGH level	$0.7*V_{DDIO}$	$V_{DDIO}+0.3$	$0.7*V_{DDIO}$	$V_{DDIO}+0.3$	$0.7*V_{DDIO}$	$V_{DDIO}+0.3$	V	
V_{hys}	Input Hysteresis	-	-	$0.0318*V_{DDIO}$	-	$0.05*V_{DDIO}$	-		
V_{OL}	Output voltage, LOW level	0	0.4	0	0.4	0	0.4	V	Sink current 5.5/20mA, V_{DDIO} >2V
		-	-	0	$0.2*V_{DDIO}$	0	$0.2*V_{DDIO}$	V	Sink current 2.7mA/14, V_{DDIO} <= 2V
I_{OL}	Output current, LOW level	3	-	3	-	20[1]		mA	V_{OL} = 0.4V
		-	-	6	-	-	-	mA	V_{OL} = 0.6V
t_{of}	Output fall time (Vihmin to Vilmax)	-	250	$20*V_{DDIO/5.5}$	250	$20*V_{DDIO/5.5}$	120	ns	
t_{SP}	Input filter suppression pulse width	-	-	0	50	0	50	ns	
I_i	Input current	-10	10	-10	10	-10	10	µA	$0.1 * V_{DDIO} < V_i < 0.9V_{DDIO}$_max
C_i	Capacitance	-	10	-	10	-	10	pF	

[1] *The I2C IOs must be set to Fast Plus Mode to meet this specification*

Table 15: I²C Mode GPIO Terminal Characteristics

3.4.7. GPIO and PS/2 Mode GPIO Terminal Characteristics

Symbol	Item	Min	Typical	Max	Unit	Notes
V_{IL}	Input 'L' voltage	-0.3	—	0.3*VDDIO	V	
V_{IH}	Input 'H' voltage	0.7*VDDIO	—	VDDIO+0.3	V	
V_{hys}	Input Hysteresis	0.1 * VDDIO	—	—	V	
V_{OH}	Output 'H' voltage	VDDIO * 0.8	—	VDDIO	V	V_{DDIO}=3.3V, 1.8V
V_{OL}	Output 'L' voltage	VSS	—	VDDIO * 0.2	V	V_{DDIO}=3.3V, 1.8V

Symbol	Item	Min	Typical	Max	Unit	Notes
$\|I_{OL\_LV}\|$	Output current LV	3.0 6.0	—	—	mA mA	V_{DDIO}=1.8V, DS = 0 V_{DDIO}=1.8V, DS = 1
$\|I_{OH\_LV}\|$	Output current LV	3.0 6.0	—	—	mA mA	V_{DDIO}=1.8V, DS = 0 V_{DDIO}=1.8V, DS = 1
$\|I_{OL}\|$	Output current	10.0 20.0	—	—	mA mA	V_{DDIO}=3.3V, DS = 0 V_{DDIO}=3.3V, DS = 1
$\|I_{OH}\|$	Output current	10.0 20.0	—	—	mA mA	V_{DDIO}=3.3V, DS = 0 V_{DDIO}=3.3V, DS = 1
I_{I_Z}	Input leakage current	-10	—	10	µA	V_{DDIO}=1.8, 3.3V
I_{O_DZ}	Output off-leakage current	-1	—	1	µA	V_{DDIO}=1.8, 3.3V
R_{PU}	Pull-up resistor Pull-down resistor (GPIO [9:0])	49	60	72	kΩ	V_{DDIO}=3.3V, 1.8V, Pad's level is V_{SS} or V_{DDIO}
R_{PD}		49	60	72		

Table 16: Gen6 GPIO and PS/2 Mode Terminal Characteristics

3.4.8. Analog Terminal Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition[1]
V_{OH_TX}	Electrode output high voltage[2]	V_{DDA} * 0.8	-	V_{DDA}	V	RXTX (BUFSEL =0), V_{DD}=3.3V, I_{OHTX0}= -2.5mA
						RXTX (BUFSEL =1), V_{DD}=3.3V, I_{OHTX1}= -5.0mA
						RXTX (BUFSEL =2), V_{DD}=3.3V, I_{OHTX2}= -7.5mA
						RXTX (BUFSEL =3), V_{DD}=3.3V, I_{OHTX3}= -10.0mA
V_{OL_TX}	Electrode output low voltage[3]	V_{SS}	-	V_{DDA} * 0.2	V	RXTX (BUFSEL =0), V_{DD}=3.3V, I_{OHTX0}= -2.5mA
						RXTX (BUFSEL =1), V_{DD}=3.3V, I_{OHTX1}= 5.0mA
						RXTX (BUFSEL =2), V_{DD}=3.3V, I_{OHTX2}= 7.5mA
						RXTX (BUFSEL =3), V_{DD}=3.3V, I_{OHTX3}= 10.0mA
I_{OZL} / I_{OZH}	Electrode output off-leakage current	-1.0	-	1.0	µA	Rxterminal, V_{DD}=3.3V

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition[1]
R_{PURXBT}	Electrode pull up resistor	49	60	72	kΩ	Only applies to RXTX cells with multi-use button mode

[1] SR_CNT: TX terminal slew rate setting
[2] Excluding overshoot
[3] Excluding undershoot

Table 17: Analog Terminal Characteristics

4. Interface Specification

NOTE: For details on the firmware interface to the Gen6 platform, including memory map and register details consult GP-AN-190313 Interfacing to Gen6 App Note.

4.1. I²C Specification

4.1.1. I2C Timing Diagram

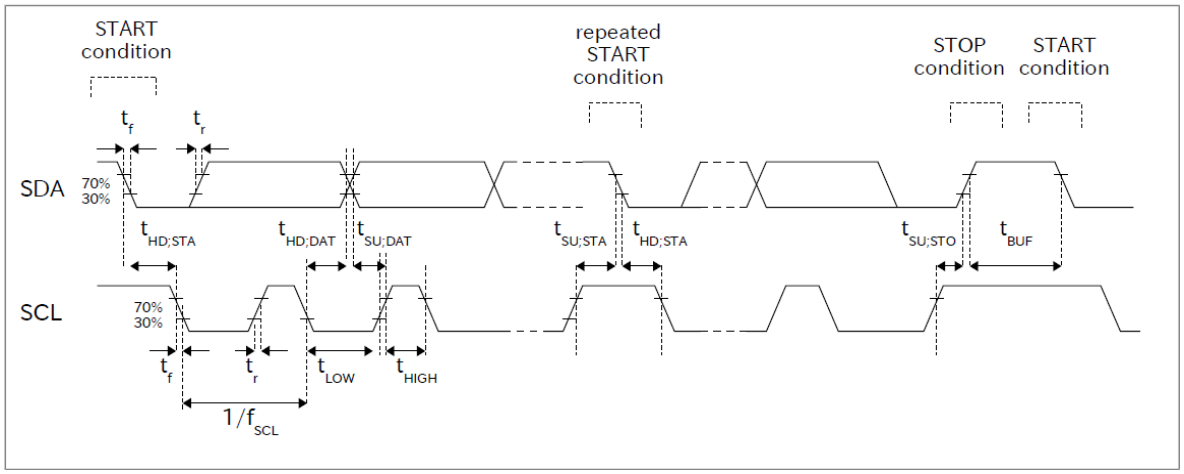


Figure 8: I²C Timing Diagram

4.1.2. SDA and SCL Bus Line Characteristics

Symbol	Item	Standard Mode		Fast Mode		Fast Mode Plus 1 Mbit/s max		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
t_{LOW}	SCL clock low time	4.7	-	1.0	-	0.5		µs
t_{HIGH}	SCL clock high time	4.0	-	0.6	-	0.26		µs
$t_{SU;DAT}$	SDA data setup time	250	-	100	-	50		ns
$t_{HD;DAT}$	SDA data hold time	0	-	0	-	0		µs
$t_{r\ (note\ 1)}$	SDA and SCL rise time	-	1000	20	300		120	ns

Symbol	Item	Standard Mode		Fast Mode		Fast Mode Plus 1 Mbit/s max		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{f\ (note\ 1)}$	SDA and SCL fall time	-	300	$20*V_{DDIO}/5.5$	300	$20*V_{DDIO}/5.5$	120	ns
$t_{HD;STA}$	START condition hold time	4.0	-	0.6	-	0.26		µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	-	0.6	-	0.26		µs
$t_{SU;STO}$	STOP condition set-up time	4.0	-	0.6	-	0.26		µs
t_{BUF}	Stop to Start condition time (bus free)	250	-	250	-	250		µs
C_b	Capacitive load for each bus line	-	400	-	400		500	pF
V_{nL}	Noise margin at the LOW level	$0.1*V_{DDIO}$	-	$0.1*V_{DDIO}$	-	$0.1*V_{DDIO}$		V
V_{nH}	Noise margin at the HIGH level	$0.2*V_{DDIO}$	-	$0.2*V_{DDIO}$	-	$0.2*V_{DDIO}$		V

Table 18: I2C Interface Specification

Note 1: When SCL/SDA are receiving Tf/Tr specs are min: 0 ns, max 300 ns. Tf/Tr specs shown are when device is driving the line. For SCL transmitting, Tf doesn't apply.

Note 2: Firmware may require time between I2C transactions. Touchpad firmware typically requires greater than 500 µs.

4.2. Programming the Gen6 IC

By default, the Gen6 touch controller ships with a bootloader installed. The bootloader can be utilized to load custom firmware to the IC's flash memory for customer applications. For details on utilizing this bootloader, reference the following document:

IC-AP-200415 Gen6 Bootloader Application Note

NOTE: Cirque cannot guarantee the validity of program code loaded onto the IC by third parties. It is the responsibility of the customer and customer manufacturing partner to ensure that the programming process is properly followed, and that firmware is configured for correct operation of the Gen6 IC.

4.3. Reading the Chip ID

Using the existing bootloader. The Read Extended Address command can be used to read out the Chip ID information. The following tables show details about the chip ID/wafer ID address(es) for the F2 chip:

Base Address	0x41000408
Length	20 bytes

Table 19: Olympus QFN64/Timp QFN42 Chip ID Address

Address Length	Description	Details
0x41000408 4 bytes	ASIC Final Test Date	• 0x41000408 – (byte) Day (1-31) • 0x41000409 – (byte) Month (1-12) • 0x4100040A – (byte) Last two decimal numbers of Year E.g., Year 2022 would be the "22" decimal 0x4100040B - Reserved (Should be 0xFF)
0x4100040C 4 bytes	IC Rev and Package	• 0x4100040C – (byte) IC revision (1p1 = 2, 1p3 = 4) • 0x4100040D – (byte) Package Type (QFN64 = 1, QFN42 = 2, Bare die or wafer = 0xFF) • 0x4100040E - Reserved (Should be 0xFF) • 0x4100040F - Reserved (Should be 0xFF)
0x41000410 8 bytes	Wafer Lot ID and Die Location	• 0x41000410 - 1st ASCII encoded character of Lot ID • 0x41000411 - 2nd ASCII encoded character of Lot ID • 0x41000412 - 3rd ASCII encoded character of Lot ID • 0x41000413 - 4th ASCII encoded character of Lot ID • 0x41000414 - 5th ASCII encoded character of Lot ID • 0x41000415 - 6th ASCII encoded character of Lot ID • 0x41000416 - 7th ASCII encoded character of Lot ID • 0x41000417 - 8th ASCII encoded character of Lot ID Characters that are not used are written as spaces (ASCII 0x20)
0x41000418 4 bytes	Wafer Number	• 0x41000418 - Wafer Number in hex format (valid numbers are 0x01 to 0x19) • 0x41000419 - Reserved (Should be 0xFF) • 0x4100041A – (byte) Y location • 0x4100041B – (byte) X location

Table 20: Olympus QFN64/Timp QFN42 Chip ID Details

5. Mechanical Specification

5.1. Physical Dimensions

5.1.1. Olympus QFN64

NOTE: Dimensions are in millimeters. Drawings are not to scale.

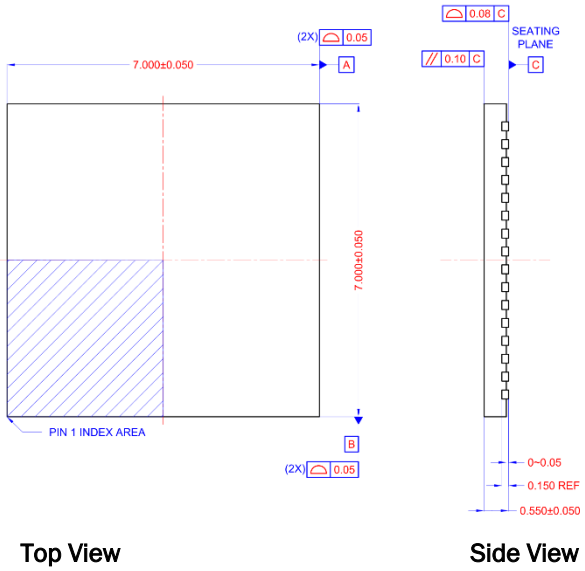


Figure 9: Olympus QFN64 Top & Side View Mechanical Drawings

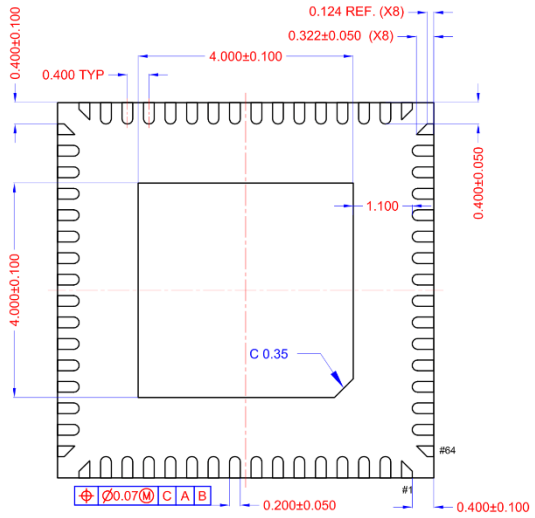
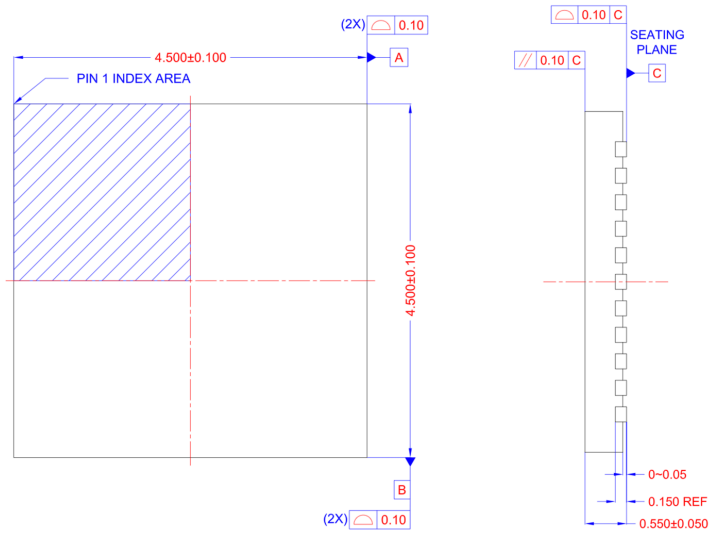


Figure 10: Olympus QFN64 Bottom View Mechanical Drawing

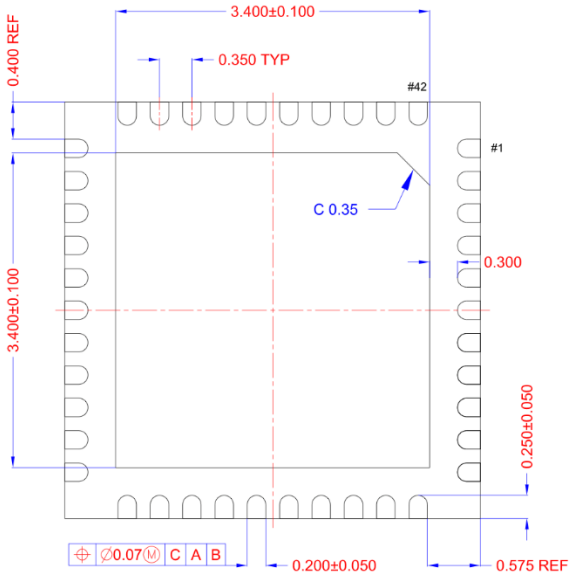
5.1.2. Timp QFN42

NOTE: Dimensions are in millimeters. Drawings are not to scale.



Top View **Side View**

Figure 11: Timp QFN42 Top & Side View Mechanical Drawings



Bottom View

Figure 12: Timp QFN42 Bottom View Mechanical Drawing

5.2. Reference SMT Land Footprints

5.2.1. Olympus QFN64

NOTE: Dimensions are in millimeters. Drawings are not to scale.

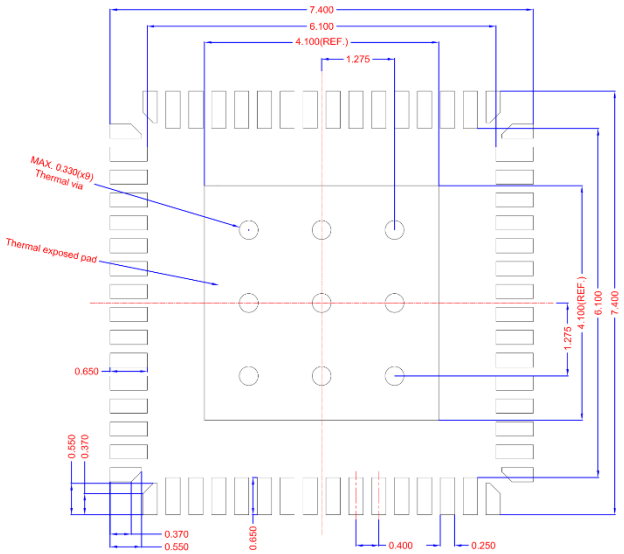


Figure 13: Olympus QFN64 Reference SMT Footprint

5.2.2. Timp QFN42

NOTE: Dimensions are in millimeters. Drawings are not to scale.

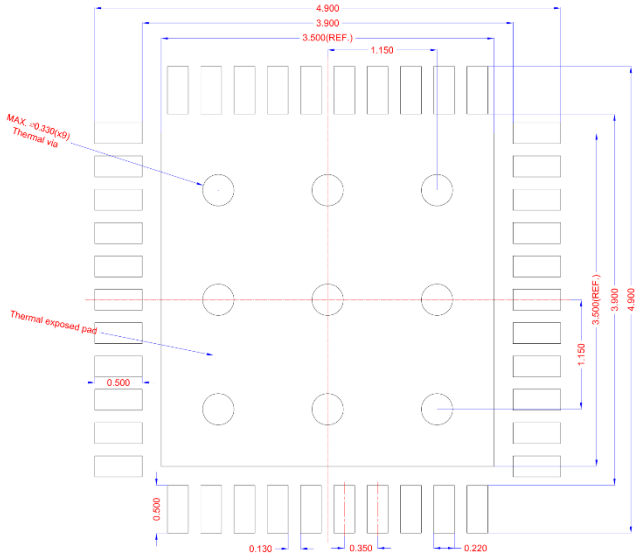


Figure 14: Timp QFN42 Reference SMT Footprint

5.2.3. SMT Reflow Heat Profile

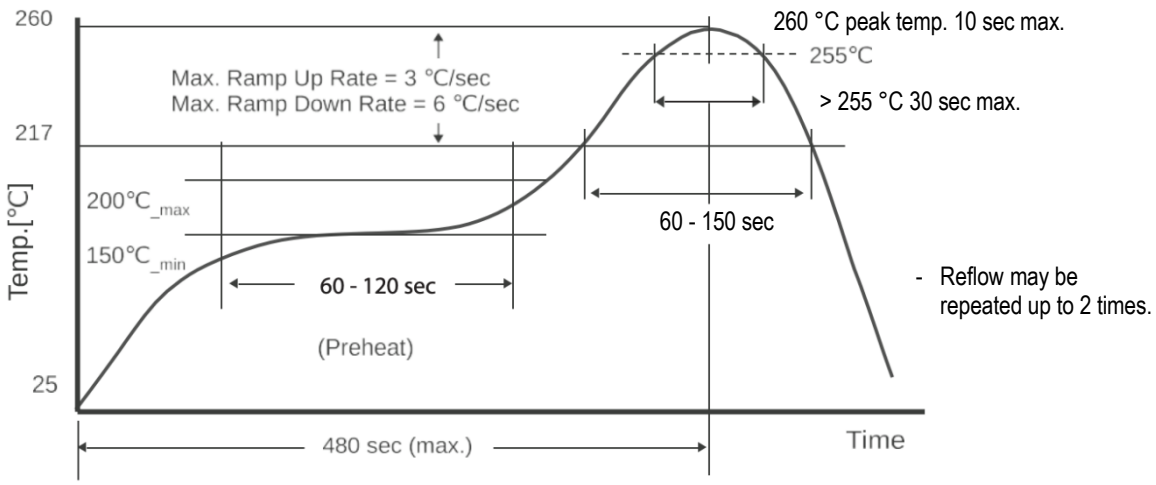


Figure 15: SMT Reflow Profile Chart

5.3. Part Marking Details

5.3.1. Olympus QFN64

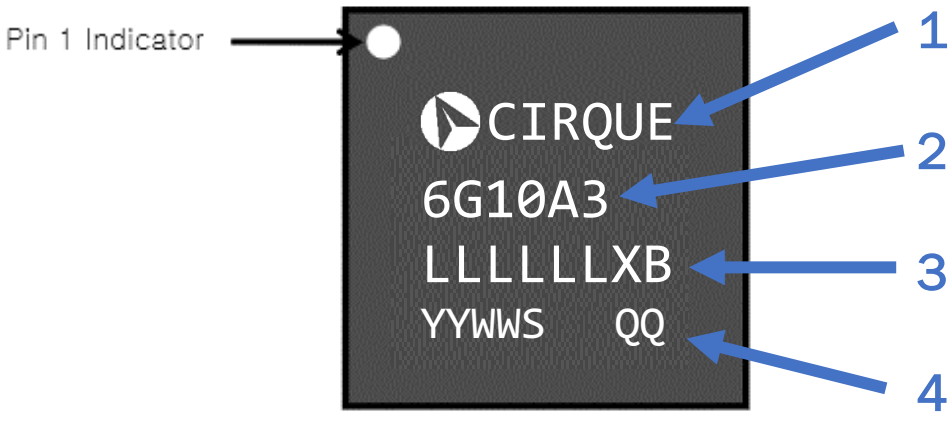


Figure 16: Olympus QFN64 Part Marking

Text Item	Marking	Detail
1	CIRQUE	Manufacturer Logo and name
2	6G10A3	Part number “10-02A1A3-111” will be part marked “6G10A3.”
3	LLLLLLXB	Six- or seven-character Lot number (LLLLLLX) + one-character sub-lot (B) Please note that the Lot number may use six or seven characters. Most lot numbers are comprised of six characters. In the case where the lot number is comprised of only six characters, the seventh character will always be a “-“. For example, if the Lot is 123ABC and the sub-lot is 0, then the marking will be “123ABC-0”. If the lot is 7 characters, then there will not be a “-:”, for example, if the lot is 1234ABC and the sub-lot is 0 then the marking will be “1234ABC0”.

Text Item	Marking	Detail
4	YYWWS QQ	Two-character Year (YY) + two-character Work week (WW) + assembly site (S)+ special designator (QQ) YYWW indicates the year and work week the IC was assembled. The YY contains the last two digits of the year and WW contains the work week. S indicates the package assembly site. (A "T" in this position indicates the assembly site is TICP, an "S" in this position indicates the assembly site is SFA.) The special designator (QQ) is an optional field and may be used to indicate Engineering Samples (ES) or other specialty designations. Please block this area for optical recognition.
*	*	The part is marked using a laser method.

Table 21: Olympus QFN64 Part Marking Specification

5.3.2. Timp QFN42

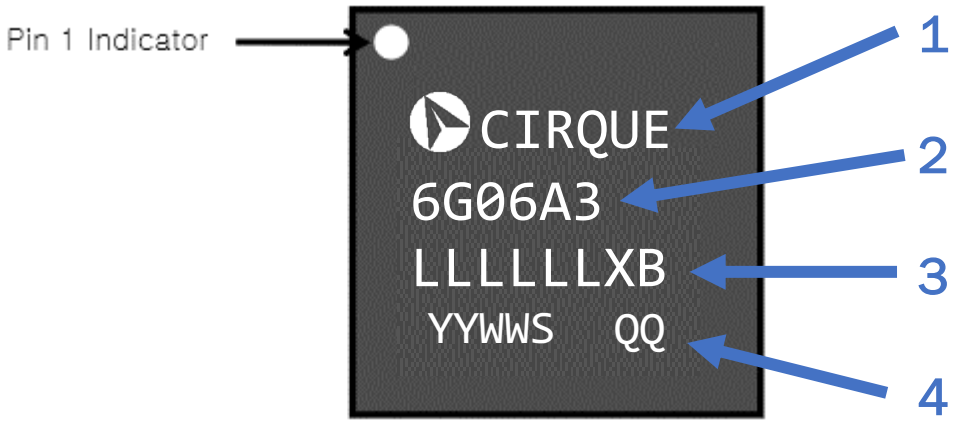


Figure 17: Timp QFN42 Part Marking

Text Item	Marking	Detail
1	CIRQUE	Manufacturer Logo and name
2	6G06A3	Part number “10-02F1A3-111” will be part marked “6G06A3.”
3	LLLLLLXB	Six- or seven-character Lot number (LLLLLLX) + one-character sub-lot (B) Please note that the Lot number may use six or seven characters. Most lot numbers are comprised of six characters. In the case where the lot number is comprised of only six characters, the seventh character will always be a “-“. For example, if the Lot is 123ABC and the sub-lot is 0, then the marking will be “123ABC-0”. If the lot is 7 characters, then there will not be a “-:”, for example, if the lot is 1234ABC and the sub-lot is 0 then the marking will be “1234ABC0”.
4	YYWWS QQ	Two-character Year (YY) + two-character Work week (WW) + assembly site (S)+ special designator (QQ) YYWW indicates the year and work week the IC was assembled. The YY contains the last two digits of the year and WW contains the work week. S indicates the package assembly site. (A “T” in this position indicates the assembly site is TICP, an “S” in this position indicates the assembly site is SFA.) The special designator (QQ) is an optional field and may be used to indicate Engineering Samples (ES) or other specialty designations. Please block this area for optical recognition.
*	*	The part is marked using a laser method.

Table 22: Timp QFN42 Part Marking Specification

6. Storage and Handling

6.1. Moisture Sensitivity Level

Parameter	Condition
JEDEC MSL	Level 3

Table 23: Olympus Moisture Sensitivity Rating

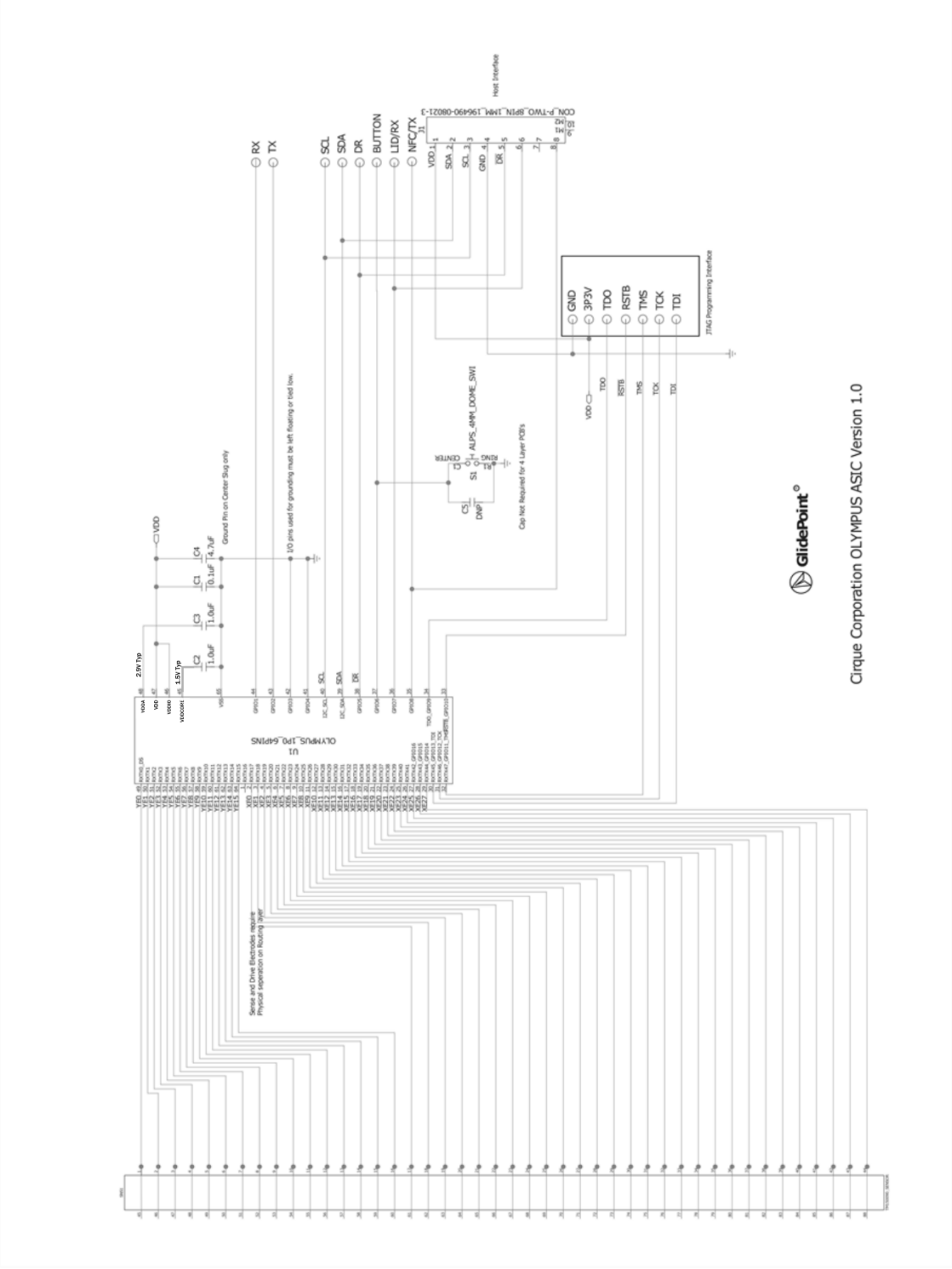
6.1.1. Recommended Storage Conditions

Parameter	Condition
Before opening package	▪ 5 – 40°C ▪ 40 – 90% RH
Storage period before opening package	▪ Can be stored up to 12 months in accordance with recommended storage conditions.
After opening package	▪ 5 – 30°C ▪ 40 – 60% RH
Storage period after opening package	▪ Can be opened up to 168 hours (~7days) (Per JEDEC MSL 3). ▪ If opened longer than the time specified above, the Gen6 ASIC should be baked before being implemented. ▪ Baking treatment is 125°C for ~24 hours. ▪ Use a heat resistant tray and pay attention to oxidation on terminals.

Table 24: Recommended Storage Details

7. Reference Schematic

Example shown represents a typical Gen6 “click pad” implementation.



8. Packing Information

8.1. Olympus QFN64 Tape and Reel Details

8.1.1. QFN64 Reel Specifications

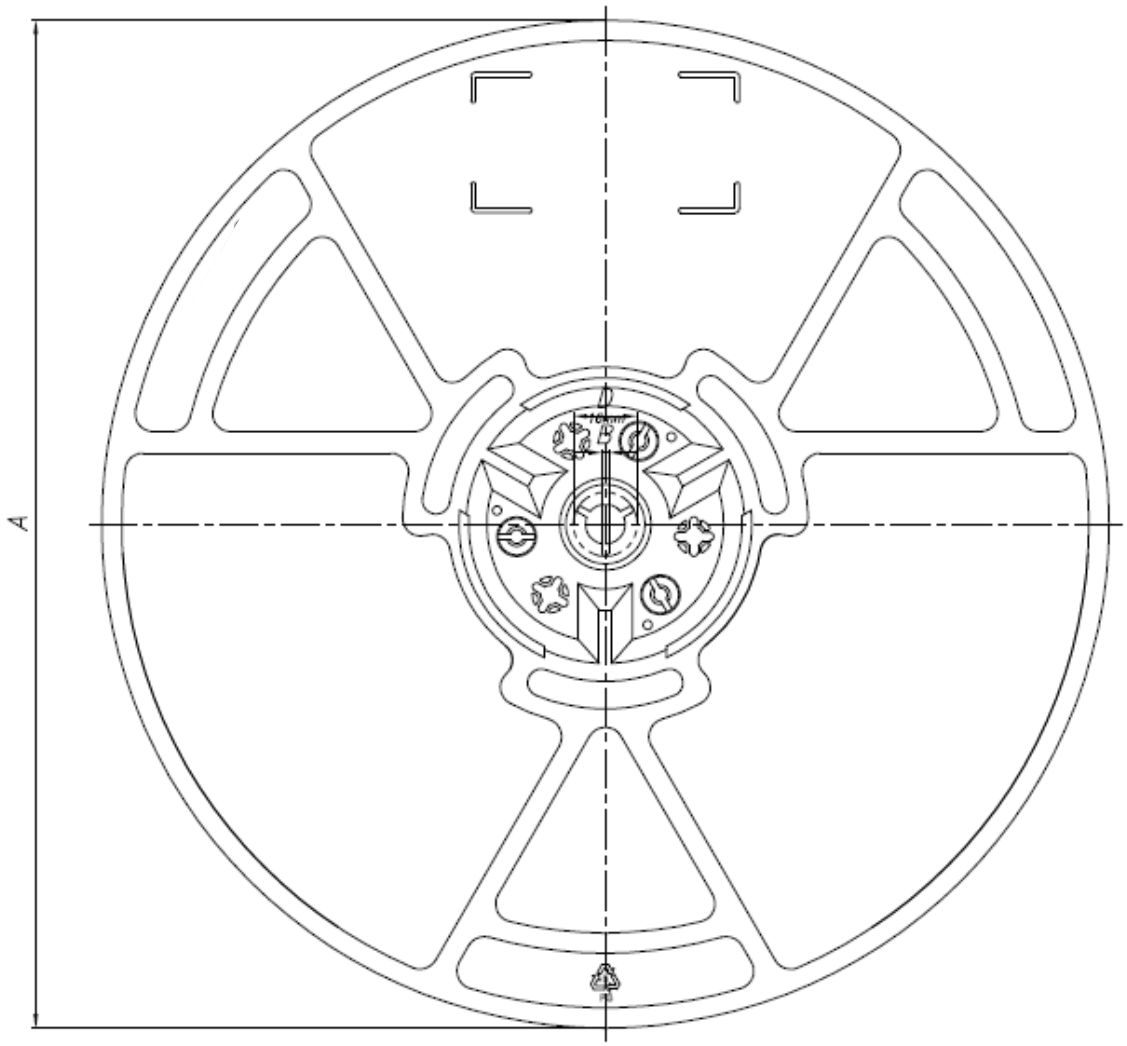


Figure 18: QFN64 Reel Top Diagram

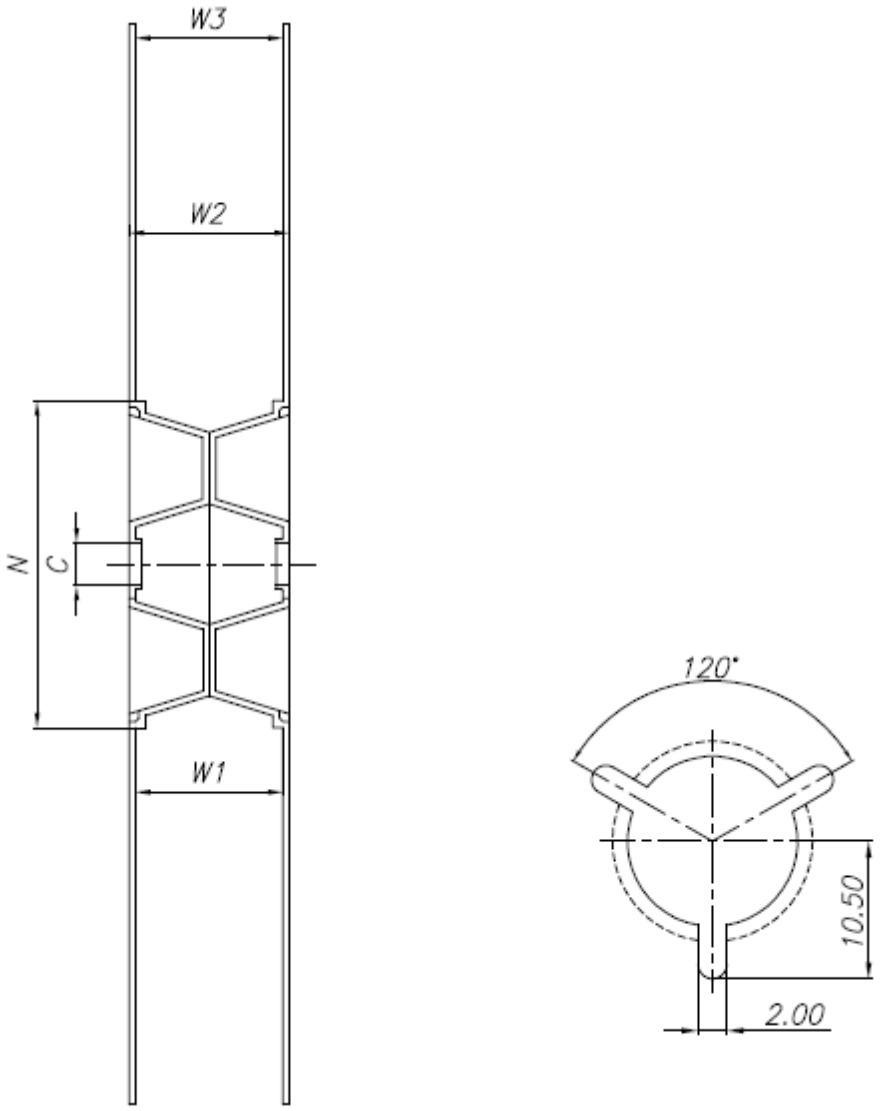


Figure 19: QFN64 Reel Side and Hub Diagram

Outer Width (W2)	Carrier Width (W1)	Outer Dia.(A)	Inner Dia. (N)	Inner Hub Dia. (C)	Outer Hub Spoke Dia. (D)	Hub Spoke Width
20.4 mm	16.4 mm	330 mm	100 mm	13 mm	20.2 mm	2.0 mm

Table 25: QFN64 Typ. Reel Dimensions

8.1.2. QFN64 Tape and Reel Dimensions

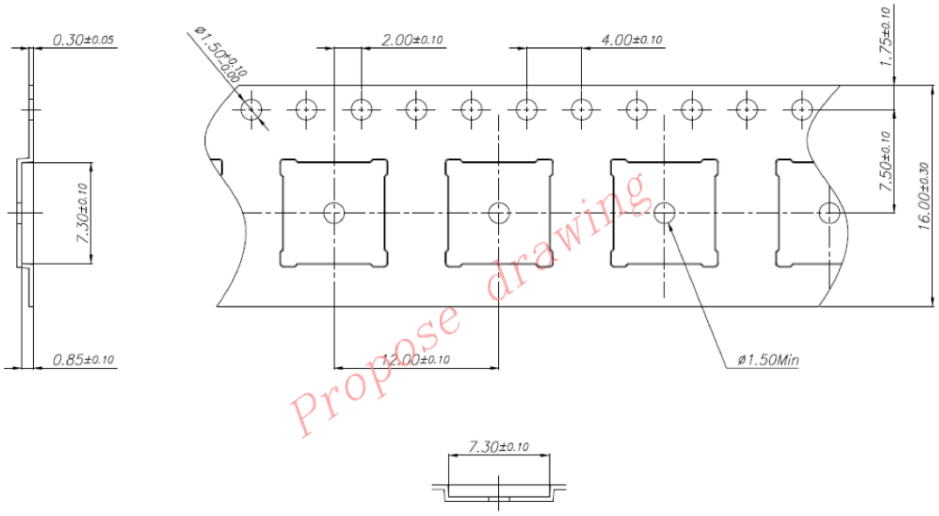


Figure 20: QFN64 Tape and Reel Dimension Drawing

Body Size	Carrier Tape Width	Cover Tape Width
7.0 x 7.0 mm	16.0 ± 0.3 mm	13.0 ± 0.1 mm

Table 26: QFN64 Carrier Tape Dimensions

8.1.3. QFN64 Lead and End Details

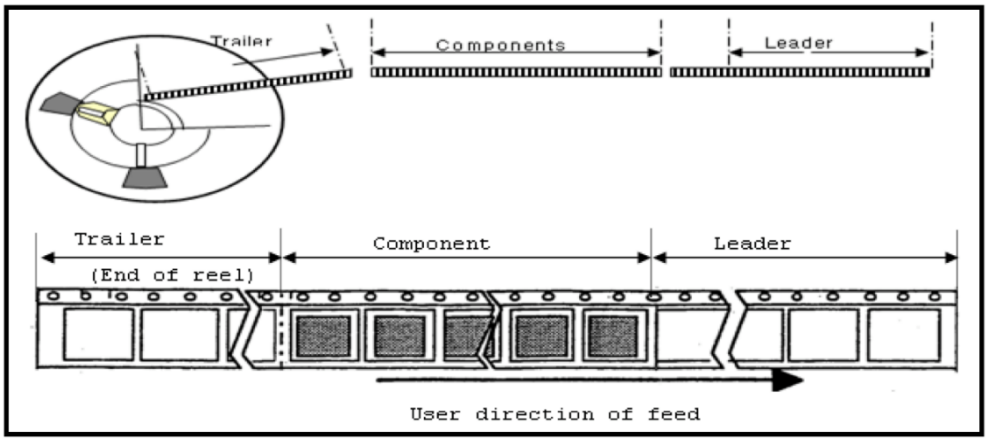


Figure 21: QFN64 Tape and Reel Lead and End Details

Package / Size	Trailer Length	Leader Length	Units / Reel
7 x 7 mm	50 pockets	50 pockets	3,000 units

Table 27: QFN64 Tape and Reel Lead and End Details

8.1.4. QFN64 Tape Direction

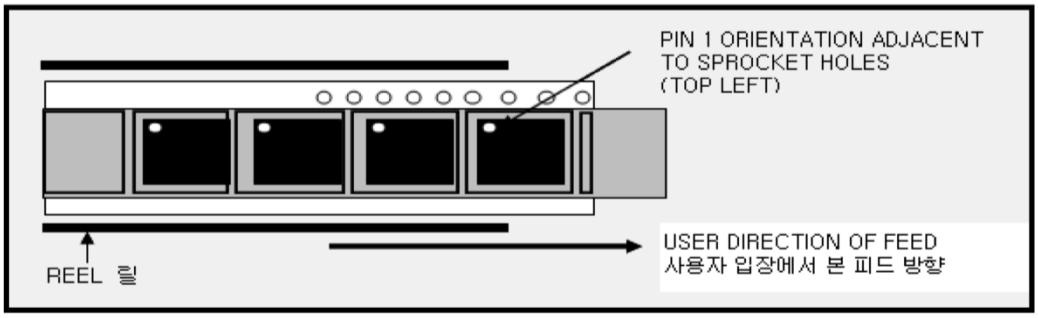


Figure 22: QFN64 Tape and Reel Tape Direction Diagram

Peel Strength Limit	20 ~90 Grams
Peel Strength Angle	165-180°
Tape Pull Speed	Minimum 300 ± 10 mm / minute
Tape Pull Length	Minimum 15 cm

Table 28: QFN64 Tape and Reel Peel Strength Detail

8.2. Timp QFN42 Tape and Reel Details

8.2.1. QFN42 Reel Specifications

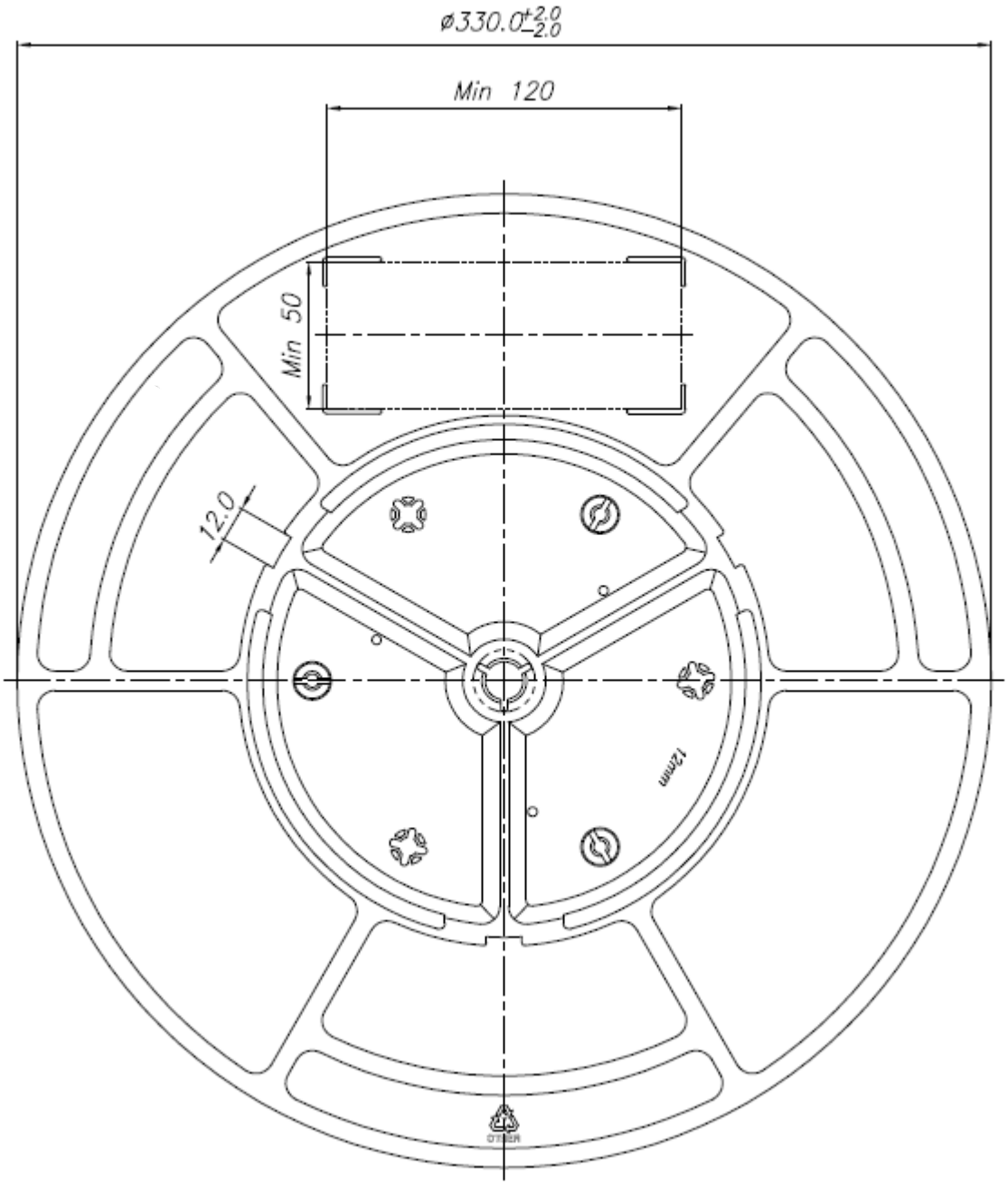


Figure 23: QFN42 Reel Top Diagram

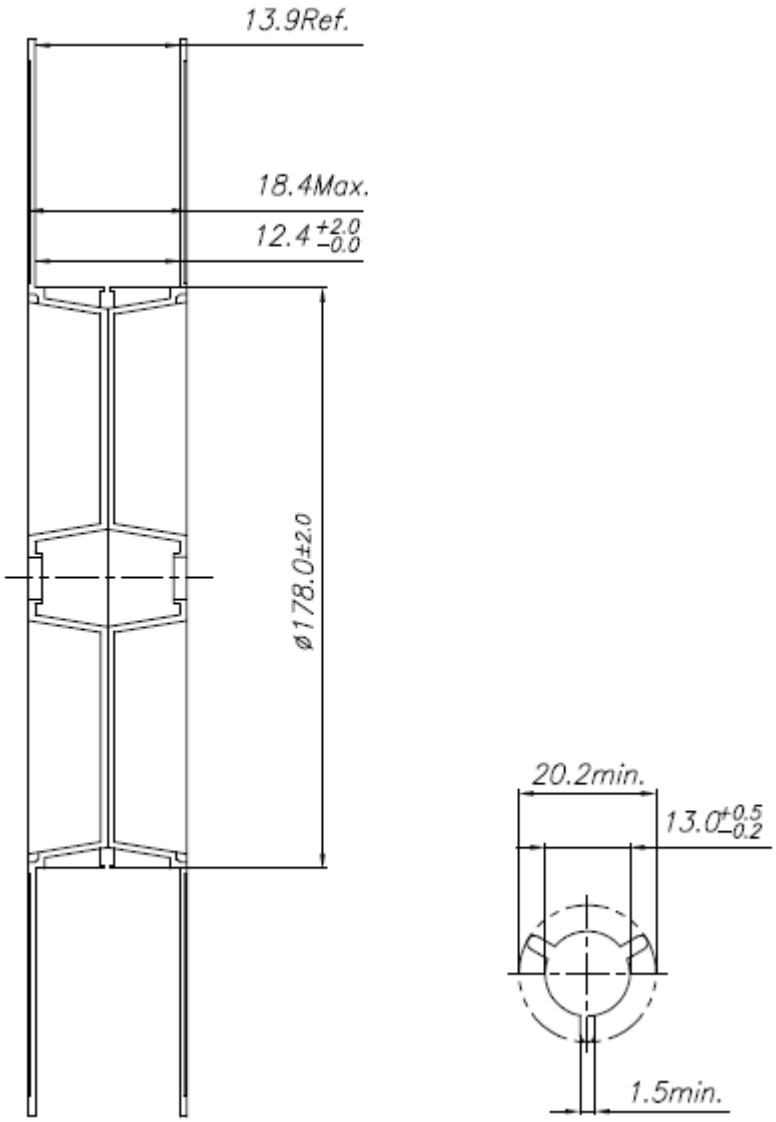


Figure 24: QFN42 Reel Side and Hub Diagram

Outer Width	Carrier Width	Outer Dia.	Inner Dia.	Inner Hub Dia.	Outer Hub Spoke Dia.	Hub Spoke Width
18.4 mm	12.4 mm	330 mm	178 mm	13 mm	20.2 mm	1.5 mm

Table 29: QFN42 Typ. Reel Dimensions

8.2.2. QFN42 Tape and Reel Dimensions

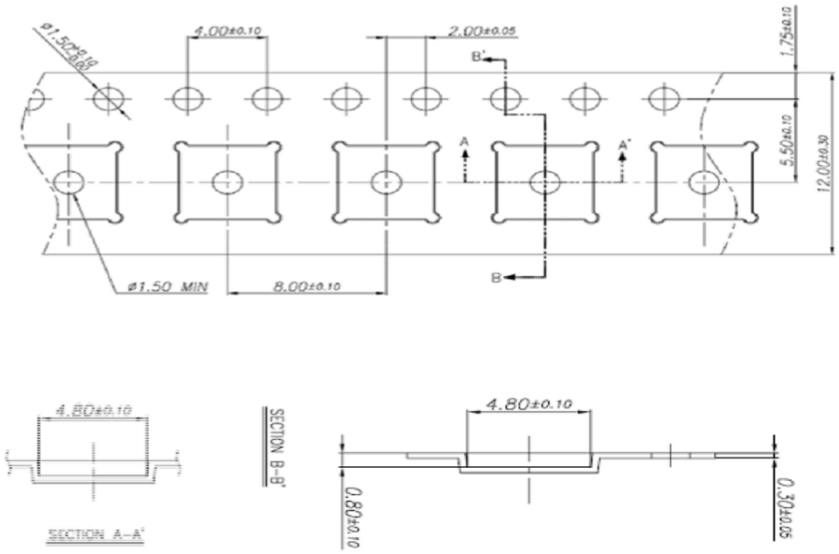


Figure 25: QFN42 Tape and Reel Dimension Drawing

Body Size	Carrier Tape Width	Cover Tape Width	
4.5 x 4.5 mm	12.0 ± 0.3 mm	9.3 ± 0.1 mm	

Table 30: QFN42 Carrier Tape Dimensions

8.2.3. QFN42 Lead and End Details

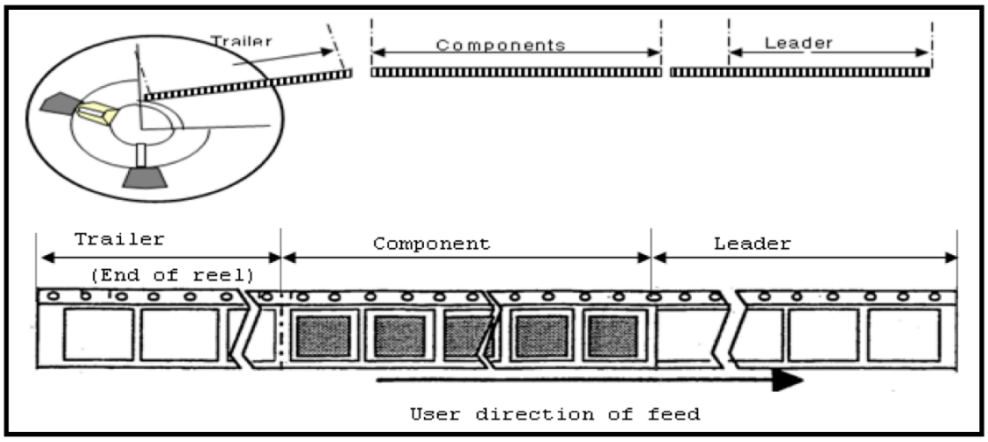


Figure 26: QFN42 Tape and Reel Lead and End Details

Package / Size	Trailer Length	Leader Length	Units / Reel
4.5 x 4.5 mm	Minimum 300 mm	Minimum 500 mm	3,000 units

Table 31: QFN42 Tape and Reel Lead and End Details

8.2.4. QFN42 Tape Direction

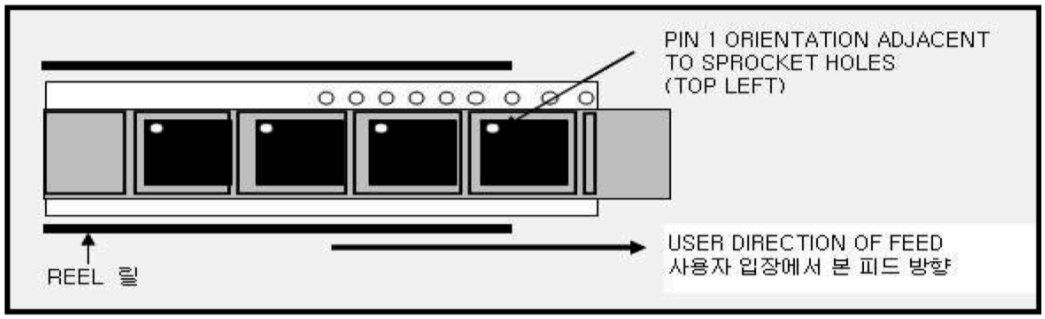


Figure 27: QFN42 Tape and Reel Tape Direction Diagram

Peel Strength Limit	20 ~90 Grams
Peel Strength Angle	165-180°
Tape Pull Speed	Minimum 300 ± 10 mm / minute
Tape Pull Length	Minimum 15 cm

Table 32: QFN42 Tape and Reel Peel Strength Detail

8.3. ESD Precautions

Embossed carrier tape and top cover tape must be anti-static.

8.4. Package and Indicators

Quantity	Identifications for Label on side of Reel	Packing Type
3,000 pcs per reel	• See section Reel Label	Reel is placed in a corrugated carton

Table 33: QFN42 Package and Indicators

8.5. Packing Material Dimensions

The inner reel box holds one reel of up to 3000 parts. The reel will be vacuum sealed in an anti-static bag, packaged in protective packing material, and packed into an inner reel box.

Reel Sealed in Vacuum Pack Anti-static bag

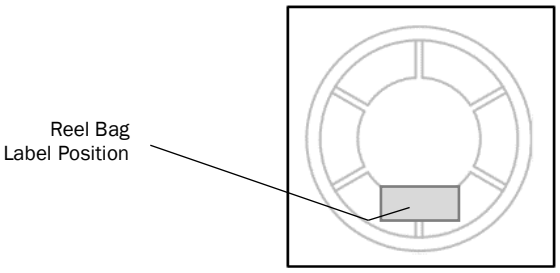


Figure 28: Timp Inner Reel Box

Inner Box (Reel Box) dimensions: 380 x 353 x 50 mm

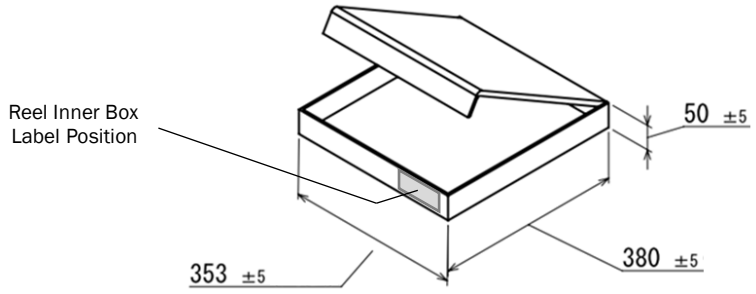


Figure 29: Timp Inner Reel Box

Each outer box contains 6 inner reel boxes.
Outer Box dimensions: 395 x 345 x 390 mm

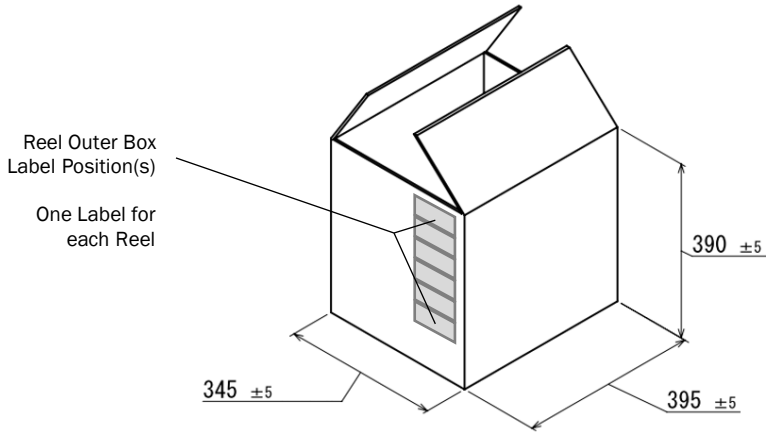


Figure 30: Timp Outer Packing Box

8.6. Reel Label

Reel Labels are adhered in the following locations:

- on the side of the reel,
- on the top of the reel bag,
- on the front right side of the reel inner box, and
- on the front right side of the outer packing box beginning at the top right corner with multiple labels applied below one another. The outer packing box will have a reel sticker for each of the reels contained in the packing box

8.6.1. Reel Label Data

The following table describes the data included on the label

Data Field Name	Description
Customer Name	• Name of the customer that the parts will be shipped to • Variable field length ≤12 characters
Customer P/N	• Internal Part Number for the customer that the parts will be shipped to • Variable length field ≤20 characters
Vendor Name	• Name of Vendor • Fixed length field of 6 characters
Vendor P/N	• Part number used by the Vendor • Fixed length field of 13 characters
Lot NO-1/Sublot-1	• First Lot number and Sublot identifier • Fixed length field of seven characters for the Lot ID. Use "-" as the 7th character for 6-character lot IDs. • Fixed length field of 1 character for Sublot ID
D/C-1	• Date Code for first Lot ID • Fixed length field of four characters. • The first two characters indicate the last two digits of the year the parts were assembled. • The last two characters indicate the week of the year that the parts were assembled.
Qty-1	• Quantity of parts on the reel that come from the first Lot ID • Fixed length field of 5 characters
Lot NO-2/Sublot-2	• Second Lot number and Sublot identifier for reels that contain parts for more than one lot • Fixed length field of 7 characters for the Lot ID. Use "-" as the 7th character for 6-character lot IDs. • Fixed length field of 1 character for Sublot ID
D/C-2	• Date Code for second Lot ID • Fixed length field of 4 characters. • The first two characters indicate the last two digits of the year the parts were assembled. • The last two characters indicate the week of the year that the parts were assembled.
Qty-2	• Quantity of parts on the reel that come from the second Lot ID • Fixed length field of 5 characters

Data Field Name	Description
Serial No	• Identifies the sequence number of the reel within a Lot No/Sublot • Fixed length field of 2 characters • Serial number starts at 1 for the first reel that contains a particular Lot No/Sublot and increments with each subsequent reel
Total Quantity	• Total number of parts contained on the reel. This quantity should be the sum of the individual lot quantities. • Fixed length field of 5 characters
Packing Date	• The date that the reels were packed. • Fixed length field of 10 characters. • The first 4 characters are the 4-digit year, the fifth character is a "-", the sixth and seventh digits are the two-digit month, the eighth character is a "-", and the final two characters are the two-digit day.
Country of Origin	• Indicates the country where the final product was packed. • Fixed length field of 5 characters
N/A	• Stamps indicating specific standards

Table 34: Reel Label Data

8.6.2. Reel Label Barcode Information

- Barcode information:
  - 1D barcode code type: Code 128A
  - Unless otherwise directed by the customer, the barcode concatenates the following information in the following order:
  - [Customer_Name][Customer_P/N][Lot_NO-1/Sublot-1][Serial_No][D/C-1][Total_Quantity]
  - Example: XXXXXXXXNNNNNNNNNNLLLLLLFSSNYYWWQQQQQ
- Data Matrix code information:
  - 2D barcode code type: Data Matrix
  - Unless otherwise directed by the customer, the Data Matrix code concatenates the following information in the following order:
  - [Customer_Name][Customer_P/N][Lot_NO-1/Sublot-1][Serial_No][D/C-1][Total_Quantity]
  - Example: XXXXXXXXNNNNNNNNNNLLLLLLFSSNYYWWQQQQQ

8.6.3. Example Generic Reel Label

9. Explanation of 250us tBuf (I2C) requirement

9.1. Background

The time between successive I2C transactions is 250us. This is longer than normal, the typical I2C spec requires 1.3us. The purpose of this appendix is to explain why the 250us wait time is required.

9.2. Timing Errata

The Gen6 I2C design has a timing errata that can occur when a transaction occurs too quickly after a previous transaction. The issue is described below.

When a transaction completes, a stop condition is generated, then the host will start another transaction by re-sending the start condition again (see simple example below).

Figure 31: Timing Errata Transaction Diagram

In the example above, when the second transaction comes in there is a special timing window where the Gen6 IC can actually lose the flag that signals that the I2C address has been received.

That timing window is shown below. In this image, the previous transaction ended with a stop condition. The next transaction has started with the proper 0x2C address match.

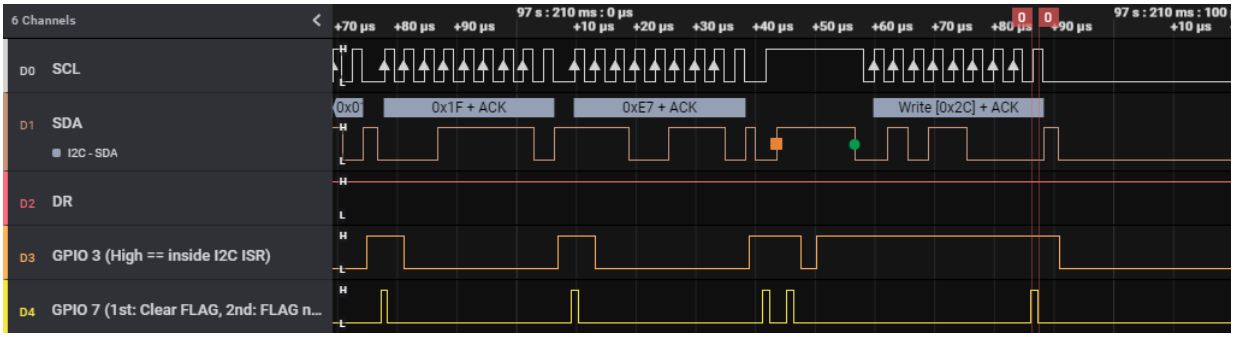


Figure 32: Timing Errata Transaction Waveform

Looking closely at the signals, the yellow signal on the bottom shows when the Gen6 IC clears the STOP condition from the previous transaction. This drawing shows red markers around that period. When the STOP condition is being cleared notice in this case that the timing is exactly after the device has sent the ACK. This is the timing window where if the CPU clears the STOP flag, the ACK and address match will be lost to the system.

The Gen6 IC will hold the I2C bus (clock stretched condition) forever, it will not recover from this case.

The core issue is that the STOP flag was cleared in that small window that caused the flags for the next byte to be cleared as well. Once that flag is lost, the I2C transaction will not be processed properly by the CPU. However, the I2C peripheral has not been properly cleared either to allow it to continue through the I2C transaction. So, the I2C peripheral will be stuck eternally in a clock stretching state and the CPU will never recover it.

Why does this not happen with every transaction? What causes it to happen only sometimes?

There is a special timing that is required to make this issue occur.
First, the interrupts must be disabled (inside the Gen6 CPU) when the STOP condition occurs. If interrupts are disabled when the STOP condition occurs, when interrupts are re-enabled the I2C STOP flag will cause an interrupt to immediately fire. This interrupt will cause the Gen6 CPU to clear the I2C STOP flag. If this STOP flag is clear after the next transaction has started (see diagram above) at just the right moment, the issue will occur.

What causes interrupts to be disabled

Certain I2C writes will cause the Gen6 CPU to write to AFE registers. These writes occur when writing measurement settings. So any time measurement settings (either exact measurement configurations or group configurations) are written, the transaction following that write can be in danger of this issue.

Is a delay required when reading data?

I2C reads can be done in 1 transaction so no delay is required for reading the sensor data.

Is it required to wait between each transaction?

Cirque recommends the 250us wait between each I2C transaction. However, because this issue is very timing dependent and only should occur after certain write commands, it is possible to have fully working communication without a delay between all transactions. In this case it is up to the end application developer to fully test their system and determine if it is an issue or not.

9.3. Required solution

To ensure that this issue never occurs, the host must wait between each I2C transaction long enough to ensure that the Gen6 IC clears the I2C STOP condition before a new ADDRESS MATCH to guarantee that those two events will never occur at the same time within the CPU. To ensure this, a 250us wait time between transactions is required. With a 250us wait time the system is guaranteed to not have this issue occur.

10. Ordering and Contact Information

10.1. Olympus QFN64 Part Number

- Olympus QFN64: 10-02A1A3-XXX

	Category	Mfg.	Pin Count	Package	Family	Additional Identifiers
Sample	10	02	A	1	A3	XXX
Definition	IC	Cirque	64	QFN	Gen6 F2	n/a

10.2. Timp QFN42 Part Number

- Timp QFN42: 10-02F1A3-XXX

	Category	Mfg.	Pin Count	Package	Family	Additional Identifiers
Sample	10	02	F	1	A3	XXX
Definition	IC	Cirque	42	QFN	Gen6 F2	n/a

10.3. Additional Resources and Contact Information

Contact a Cirque sales representative for ordering details and for a complete list of Cirque's OEM products.

Web: http://www.cirque.com
In United States & Canada: (800) GLIDE-75 (454-3375)
Outside US & Canada: (801) 467-1100
Fax: (801) 467-0208

11. Semiconductor Reliability

This section lists the Semiconductor Reliability tests performed on these parts to qualify them for production.

Test item	Test Method
Pre-condition (PC)	JESD22-A113
Temperature Cycle (TC)	JESD22-A104E
Unbiased-Highly Accelerated Stress Test (UnbiasedHAST)	JESD22-A118B
High Temperature Storage test (HTS)	JESD22-A103E
Low Temperature Storage test (LTS)	JESD22-A119A
Solderability	J-STD-002D:2011
ESD	JS-001-2017 Passed Classification 3A (>4000 - < 8000V)
	JESD22-C101F Passed Classification C3, 1500V
Latch-up	JESD78E:2016 Passed Immunity Level A, +/- 100mA I-Test, 1.5 * VDD_{MAX} OVT
Salt Atmosphere	JESD22-A107C:2013
High Temperature Operating Life cycle test	JESD22-A108F
Temperature Humidity with Bias	JESD22-A101D

Table 35: Semiconductor Reliability Test Conditions