

## Laboratory 12

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### Running the Data Cache Simulator tool

*row-major.asm*

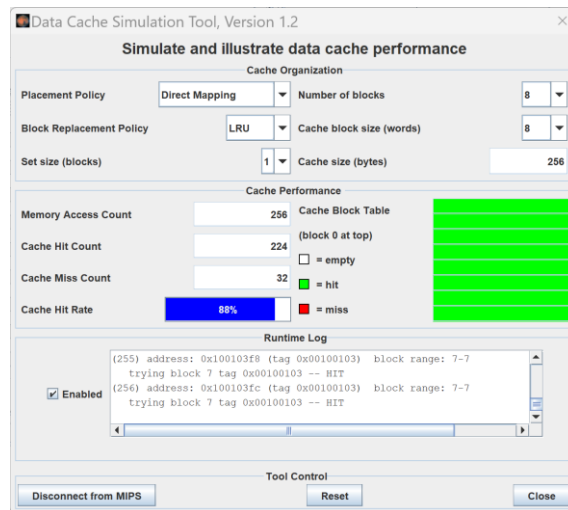
8. What was the final cache hit rate? 75%. With each miss, a block of 4 words are written into the cache. In a row-major traversal, matrix elements are accessed in the same order they are stored in memory. Thus each cache miss is followed by 3 hits as the next 3 elements are found in the same cache block. This is followed by another miss when Direct Mapping maps to the next cache block, and the patterns repeats itself. So 3 of every 4 memory accesses will be resolved in cache.

- Giải thích: Với mỗi block được xét theo hàng, sẽ luôn bị miss phần tử đầu tiên của mỗi block nên tỉ lệ hit sẽ là  $\frac{3}{4} = 0,75$ .

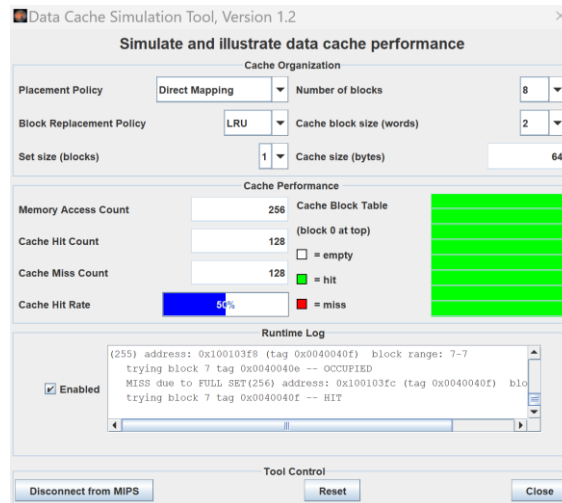
9. Given that explanation, what do you predict the hit rate will be if the block size is increased from 4 words to 8 words? 87,5%. Decreased from 4 words to 2 words? 50%.

10.

- Kích thước block là 8 words:



- Kích thước block là 2 words:

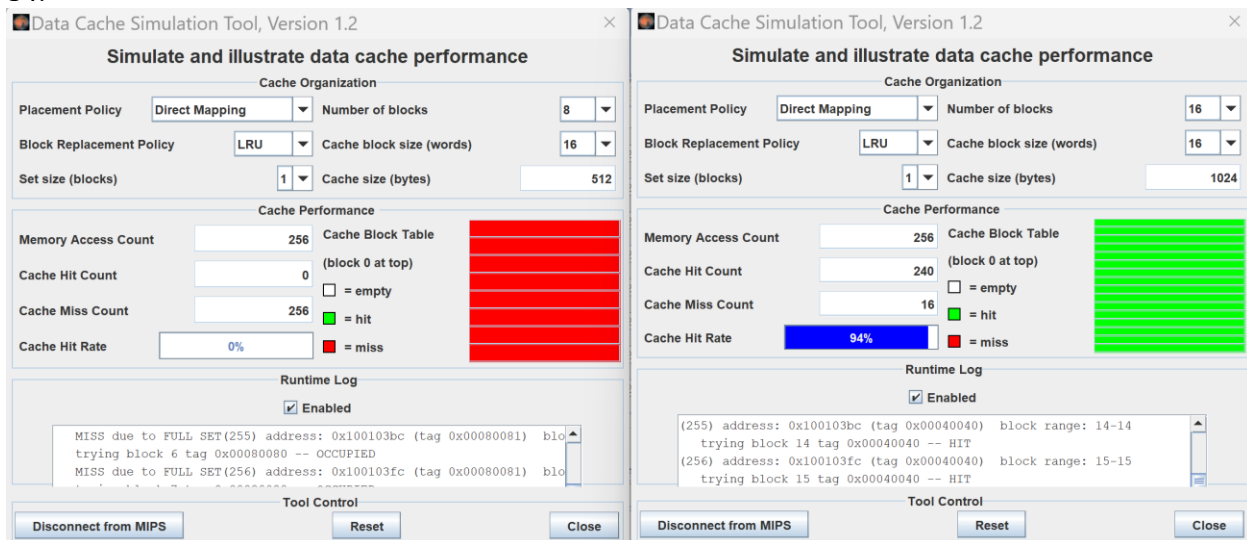


*column-major.asm*

12. What was the cache performance for this program? \_\_\_\_\_0%\_\_\_\_\_. The problem is the memory locations are now accessed not sequentially as before, but each access is 16 words beyond the previous one (circularly). With the settings we've used, no two consecutive memory accesses occur in the same block so every access is a miss.

- Giải thích: do thứ tự duyệt cột dẫn đến việc truy cập các phần tử bộ nhớ là không liên tiếp, nên mỗi lần chương trình truy cập một phần tử mới trong cột, phần tử này sẽ nằm trong một cache line khác nhau, dẫn đến cache miss liên tục.

14.

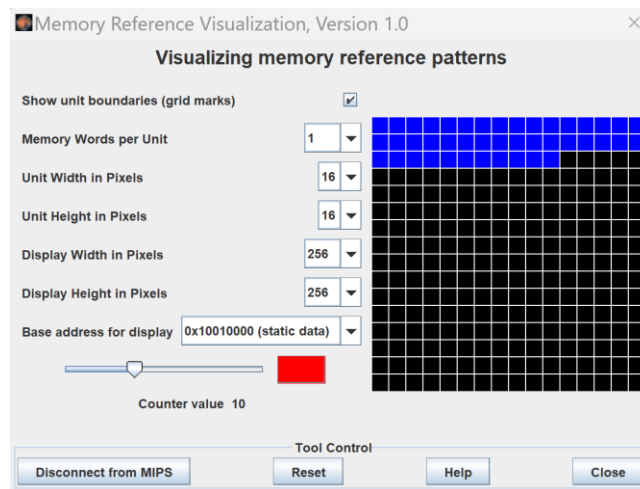


15. Re-run the program. What is the cache performance of the original tool instance? \_\_\_\_\_0%\_\_\_\_\_. Block size 16 didn't help because there was still only one access to each block, the initial miss, before that block was replaced with a new one. What is the cache performance of the second tool instance? \_\_\_\_\_94%\_\_\_\_\_. At this point, the entire matrix will fit into cache and so once a block is read in it is never replaced. Only the first access to a block results in a miss.

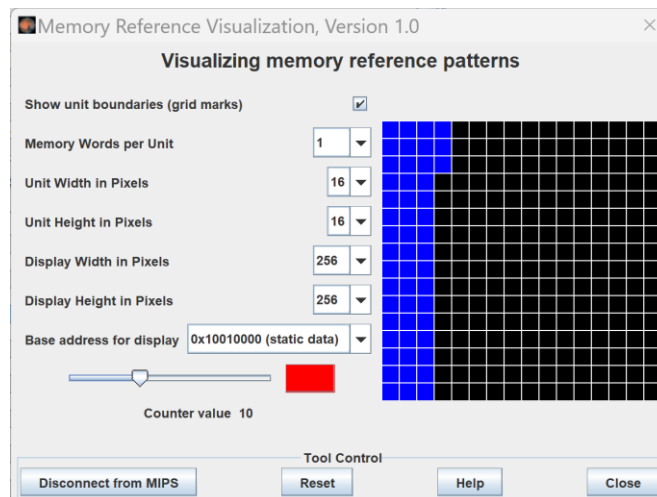
- Giải thích: do mỗi block chứa 16 từ liên tiếp. Điều này có nghĩa là khi một phần tử được nạp vào bộ đệm, toàn bộ 16 từ liên tiếp trong bộ nhớ cũng được nạp vào cùng một block.

## The Memory Reference Visualization tool

*row-major.asm*



*column-major.asm*



*fibonacci.asm*

