Add 3.3 V regulator
Add external GPIO Control – Switch to pulldown at startup.

ATTiny416

File: microcontroller.kicad_sch

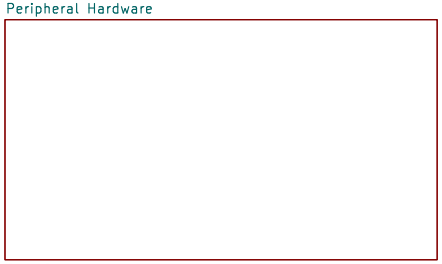
USB to UART Conversion

File: untitled.kicad_sch

Power

File: power.kicad_sch

Peripheral Hardware

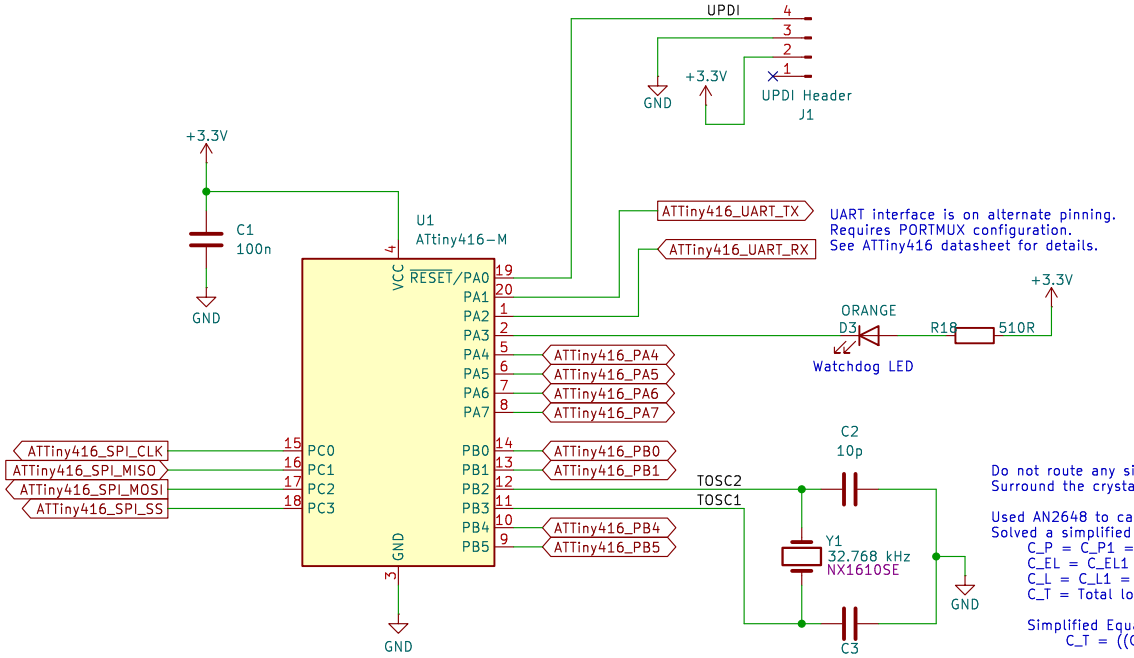


File: Peripheral_HW.kicad_sch

Sheet: /
File: ATTiny_416_Sensor_Board.kicad_sch

Title: ATTiny416 Development Board

Size: A4	Date: 2025-02-09	**Rev: 1**
KiCad E.D.A. 8.0.7		Id: 1/5



Do not route any signals under the crystal signals.
Surround the crystal signals and components with a guard trace.

Used AN2648 to calculate load capacitance.
Solved a simplified version of Equation 3-5 for C_P, assuming:
- C_P = C_P1 = C_P2 = External Load capactor values
- C_EL = C_EL1 = C_EL2 = External parasitic capacitance
- C_L = C_L1 = C_L2 = ATTiny416 internal parasitic capacitance.
- C_T = Total load capacitance (Set with value from selected crystal)

Simplified Equation 3-5:

$$C_T = ((C_L + C_P + C_{EL})^2)/(2C_L + 2C_P + 2C_{EL})$$

Simplified Equation 3-5 solved for C_P:

$$C_P = 2C_T - C_L - C_{EL}$$

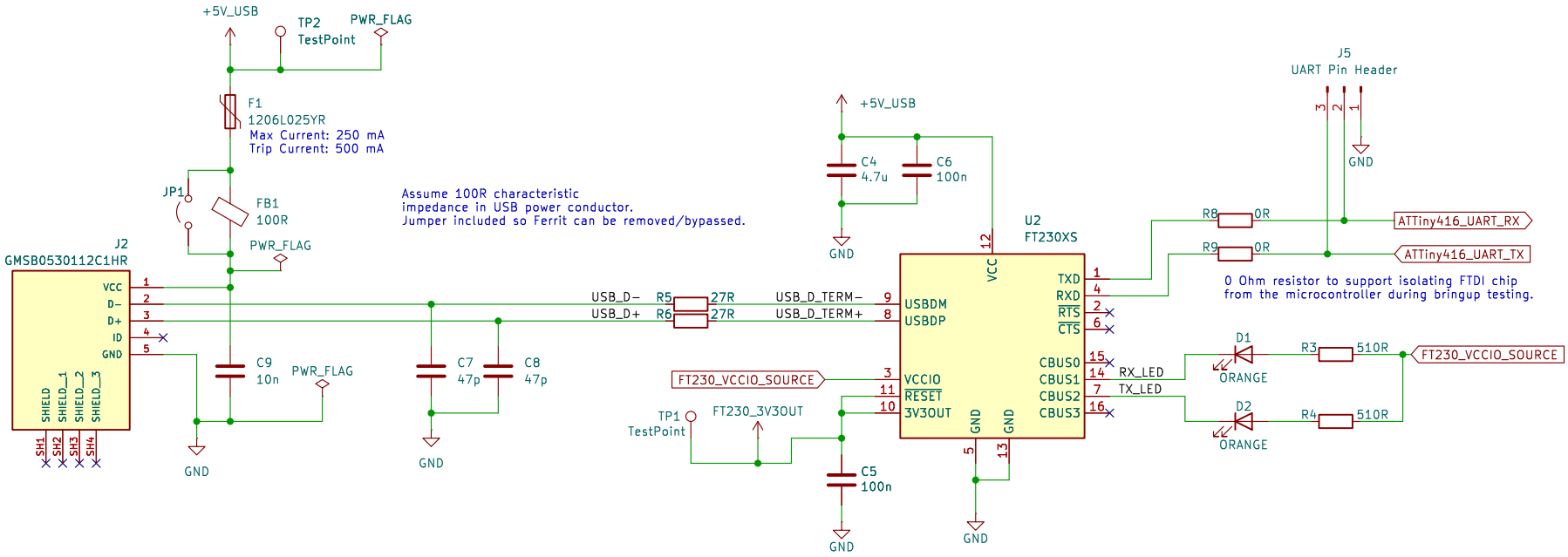
Values & Math:
- C_EL = 5pF (Assumed)
- C_L = 4.5pF (Attiny416 Datasheet, Table 35-14)
- C_T = 9pF (MU01499-32.768K Datasheet)

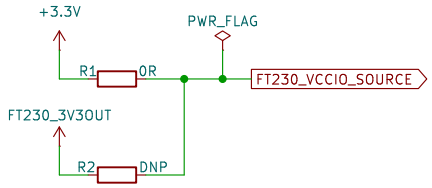
$$C_P = (2 * 9pF) - 4.5pF - 5pF$$
$$C_P = 8.5pF$$

Selected 10, 20, and 15 pF capacitors for experimentation.

WARNING:
This design should be tested to verify the exernal parasitic capacitance in the final configuration using procedures idenfied in AN2648.
Multiple C_P values should be tested to dine the actual C_EL value.

Sheet: /ATTiny416/		
File: microcontroller.kicad_sch		
Title: ATTiny416 Development Board		
Size: A4	Date: 2025-02-09	**Rev: 1**
KiCad E.D.A. 8.0.7		Id: 2/5





Not very clear how to handle connecting the FT230 to a microcontroller that is being powered by a separate 3.3 LDO. While the FT230 supports powering up to 50 mA of external electronics on the 3V3OUT, the design calls for a more capable supply.
It is desirable to have the FT230 output logic highs at the max level of the aforementioned separate 3.3V LDO,

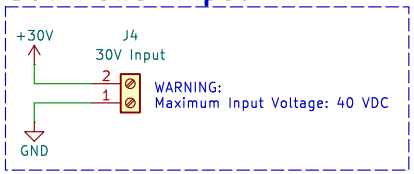
FT232BM Designers Guide shows an example that seems to imply that the all that needs to be done is to connect VCCIO to the external 3.3V rail...
It should be noted that this designer guide is for a different FTDI chip, but assuming the guts are similar enough so that it applies to the FT230.
Attempting to follow the guide, but including s DNP resistor to allow us to power VCCIO using either the external 3.3V supply of rht FT230's 3V3OUT if all else fails.

Sheet: /USB to UART Conversion/
File: untitled.kicad_sch

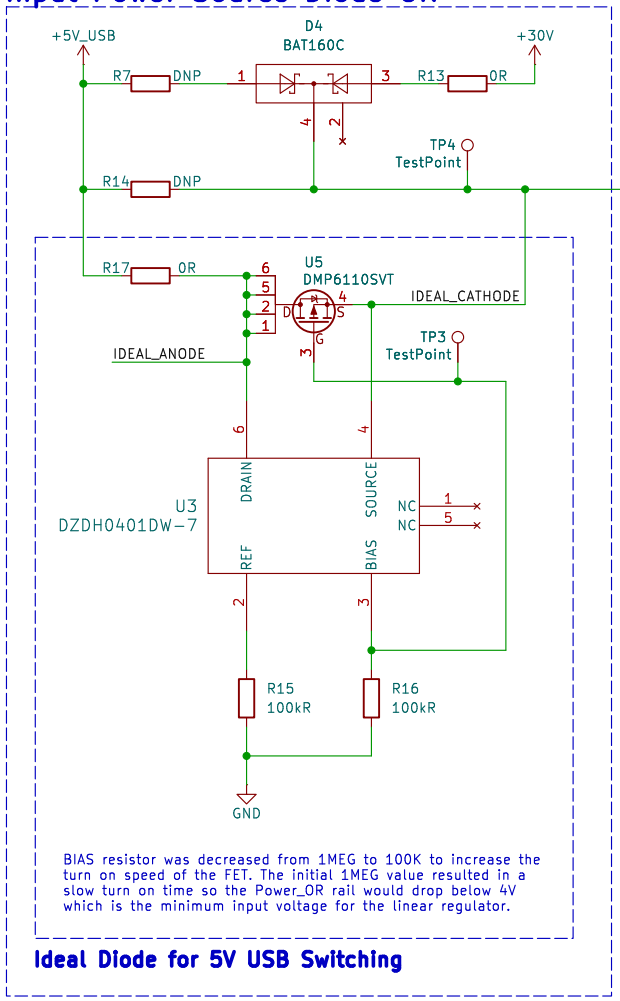
Title: ATTiny416 Development Board

Size: A4	Date: 2025-02-09	**Rev: 1**
KiCad E.D.A. 8.0.7		Id: 3/5

30V Power Input



Input Power Source Diode OR

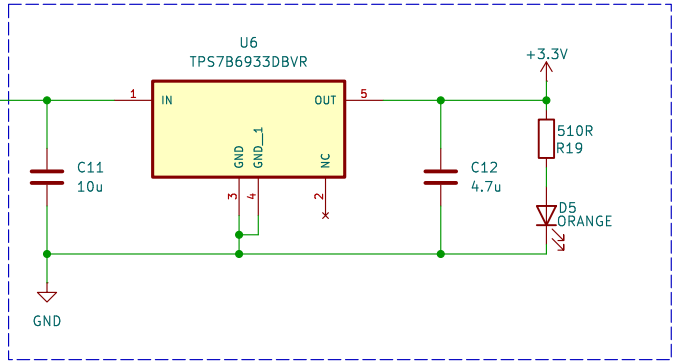


BIAS resistor was decreased from 1MEG to 100K to increase the turn on speed of the FET. The initial 1MEG value resulted in a slow turn on time so the Power_OR rail would drop below 4V which is the minimum input voltage for the linear regulator.

Ideal Diode for 5V USB Switching

PWR_FLAG

3.3V Rail Generation



Required to generate a 3.3VDC power rail capable of delivering 150mA for the uC and other components.

3.3VDC power rail needs to be derived from:
- 5VDC USB power
- 30VDC External input power

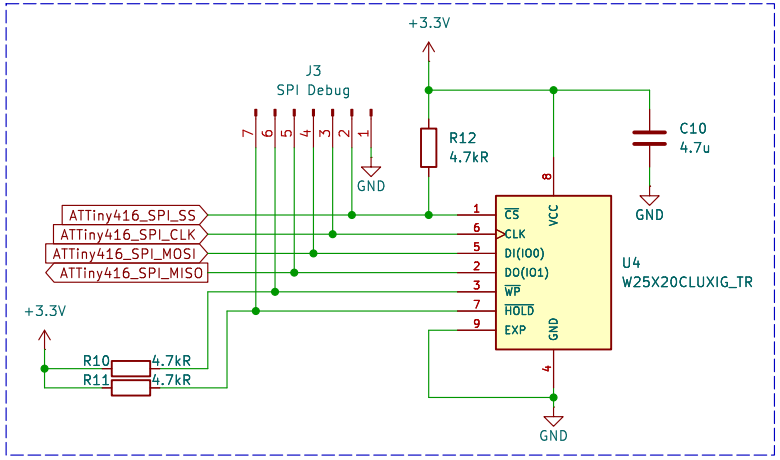
The design requires the power sources to be ORed together so that either supply can power the system.
The selected LDO can regulate with a minimum input voltage of 4.0VDC.
The 30VDC supply can be ORed using a shotky diode as the forward voltage drop on the diode will be well above the min 4.0VDC input.

The USB specification provides a minimum voltage at the device of 4.35VDC.
A shotky diode would create too high of a voltage drop and cannot be used for ORing.
Instead, an Ideal Diode is created using a ORing controller and a P-Channel FET.

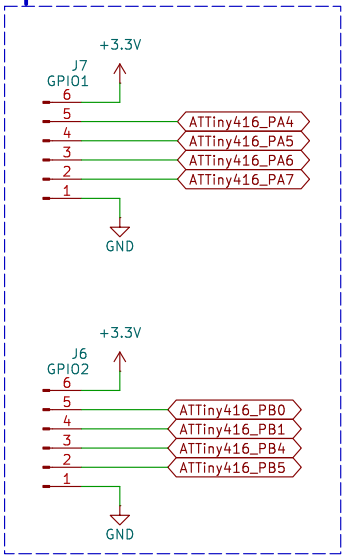
DMP6110SVT R_DS_ON = 130 mOhms
When drawing 150mA, the voltage drop will be V = IR = (.15)(.130) = .02 VDC.
Therfore, the LDO will receive ~4.33 VDC, well above the 4.0VDC minimum.

Sheet: /Power/		
File: power.kicad_sch		
Title: ATTiny416 Development Board		
Size: A4	Date: 2025-02-09	**Rev: 1**
KiCad E.D.A. 8.0.7		Id: 4/5

SPI Flash



Spare Pin Headers



Sheet: /Peripheral Hardware/
File: Peripheral_HW.kicad_sch

Title: ATTiny416 Development Board

Size: A4	Date: 2025-02-09	**Rev: 1**
KiCad E.D.A. 8.0.7		Id: 5/5