BG77 Reference Design

LPWA Module Series

Version: 1.2

Date: 2022-04-16

Status: Released

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About the Document

Revision History

Version	Date	Author	Description
1.0	2019-11-11	Ward WANG/ Newgate HUA	Initial
1.1	2021-06-21	Army RONG/ Lex LI	1. Updated pin 29 from RESERVED to GNSS_LAN_EN. 2. Updated the design of PON_TRIG interface (Sheet 7). 3. Updated the level-shifting circuit design of GNSS UART, added that design of debug UART (Sheet 7). 4. Added eSIM and analog switch designs for 1.8 V only (U)SIM interface (Sheet 12). 5. Added the (U)SIM interface level-shifting circuit design (Sheet 13).
1.2	2022-04-16	Lex LI/ Karl WANG	1. Deleted the power-up, power-down and reset timings which can be found in the hardware design manual. 2. Added the high-speed mode of USB interface, and completed the list of functions supported by USB interface (Sheet 3). 3. Updated the note about PON_TRIG (Sheet 3). 4. Updated VBAT designs in standard and battery power supply solutions (Sheet 4 and Sheet 5).

Contents

1 Reference Design

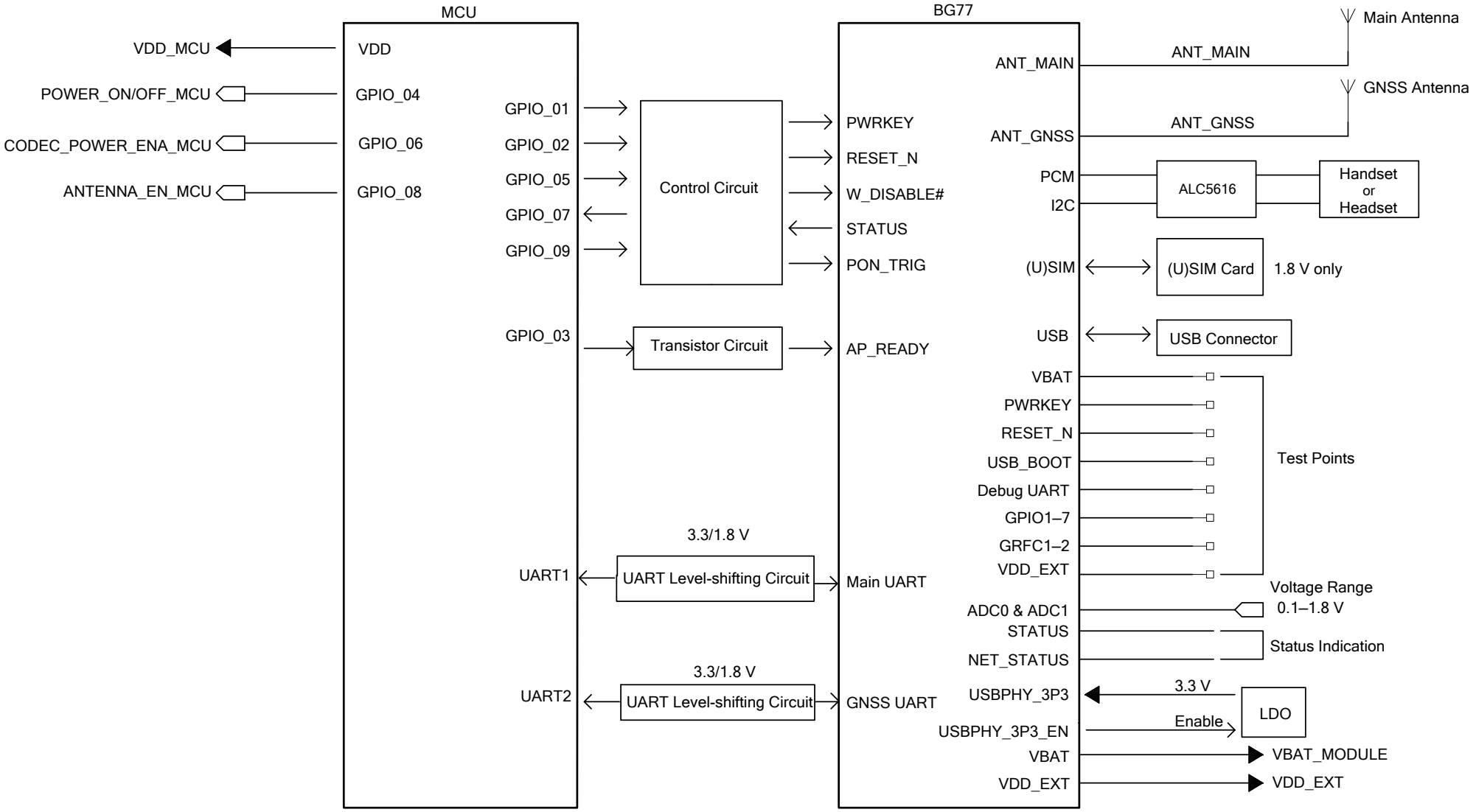
1.1. Introduction

This document provides reference designs of Quectel BG77 module, including block diagrams, power supply, UART, (U)SIM and more interface designs.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



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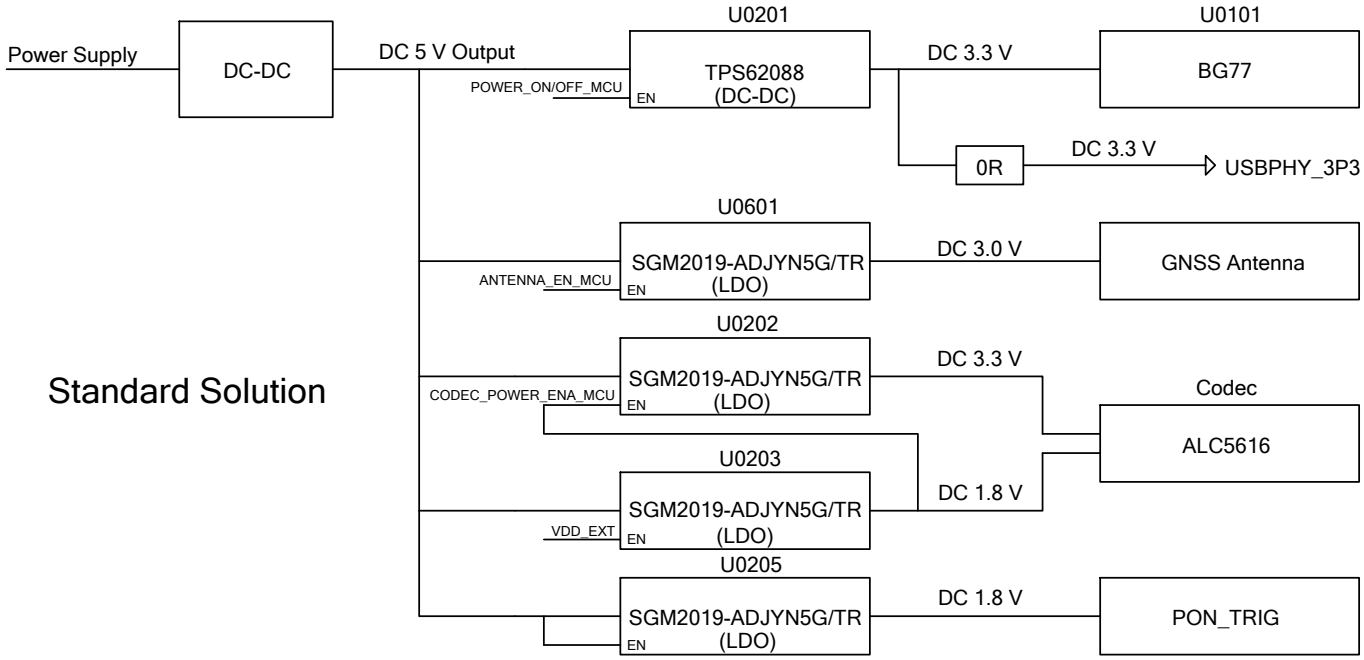
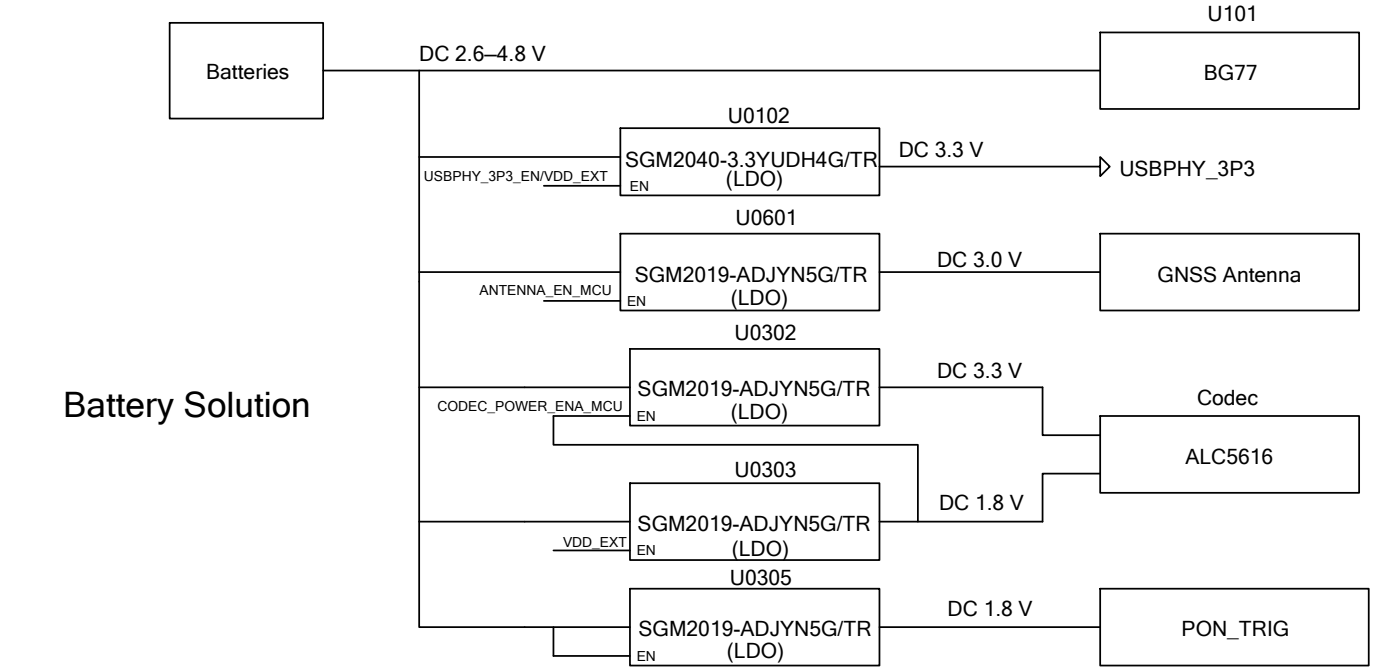
Power Supply Block Diagram



Standard Solution



Battery Solution

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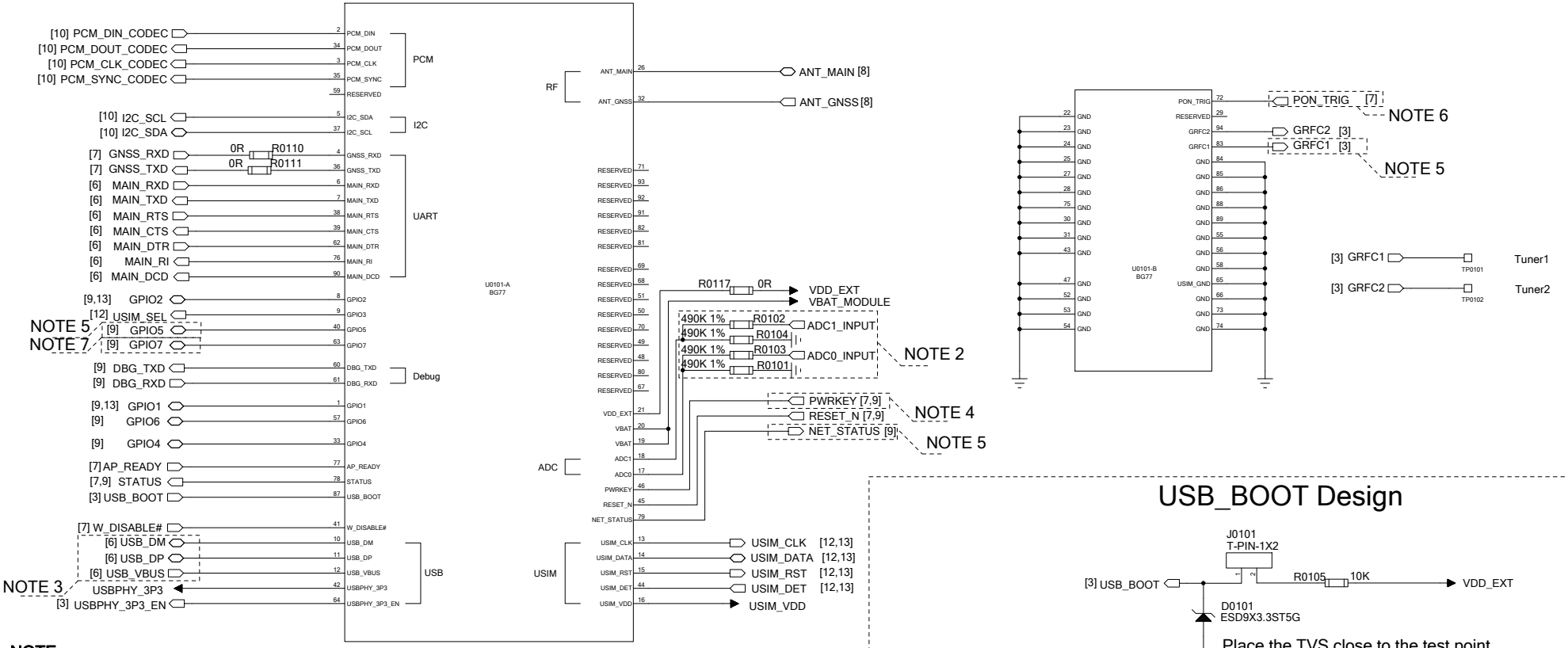
Module Interfaces Design



NOTE:

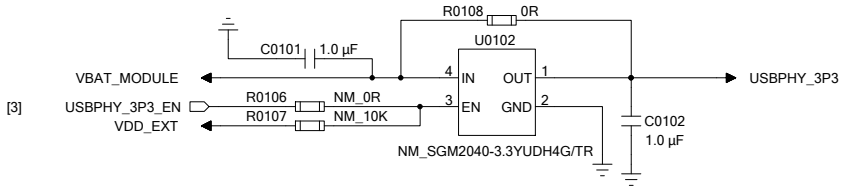
1. Keep all RESERVED and unused pins unconnected, and all GND pins should be connected to ground.
2. ADC pins can not be directly connected to the power supply and the input voltage must not exceed1.8 V. It is recommended to use resistor divider circuit for ADC application, and the divider resistor accuracy should be no less than 1 %.
3. BG77 can only be used as a slave device and supports low speed, full speed and high speed modes. The USB interface is primarily used for GNSS NMEA sentences output, software debugging and firmware upgrade. The input voltage range of USB_VBUS is 1.3–1.8 V.
4. PWRKEY should never be pulled down to GND permanently.
5. GPIO5, NET_STATUS and GRFC1 are BOOT_CONFIG pins. Never pull them up before startup, otherwise the module cannot power on normally.
6. When PON_TRIG detects a rising edge and keeps at high level for at least 30 ms, the module will wake up from PSM (Power Saving Mode). PON_TRIG is pulled down by default.
7. To meet specific requirements for power-down protection, the module can support fast shutdown over GPIO7 through software configuration. When GPIO7 (pin 63, GPIO by default) is set to a fast shutdown pin, it is pulled up by default. When the pin detects a falling edge, the module powers off within 100 ms without damaging the file system, but the writing data may be lost.

USB_BOOT Design

NOTE:

Pulling up USB_BOOT to VDD_EXT before startup, the module will be forced into emergency download mode when it is powered on.

Power Supply for USB PHY Circuit



	R0108	U0102 R0106 R0107
Standard Solution	Mount	NM
Battery Solution	NM	Mount

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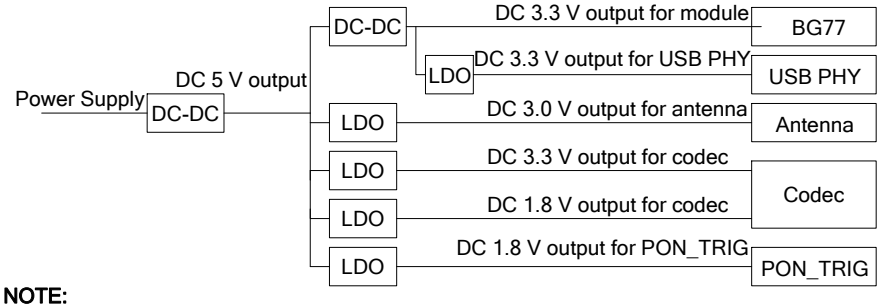
Power Supply Design (Standard)

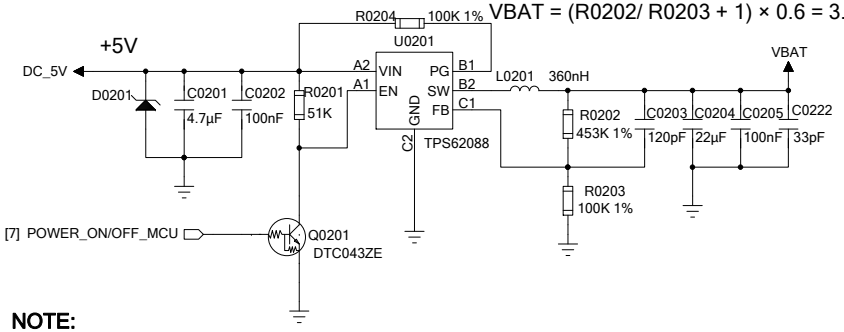
DC-DC Application



NOTE:

1. You can select either the standard power supply design or the battery power supply design according to your specific application demands.
2. This solution can be used when the input voltage is above 7 V. First, use a DC-DC converter to convert the high input voltage into a 5 V output, and then use LDOs and a DC-DC converter to generate 3.3 V, 3.0 V and 1.8 V typical voltages.

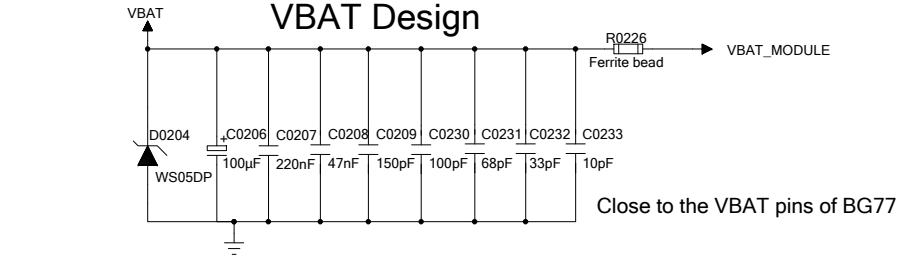
DC-DC Design



NOTE:

The maximum input supply voltage of U0201 is 5.5 V.

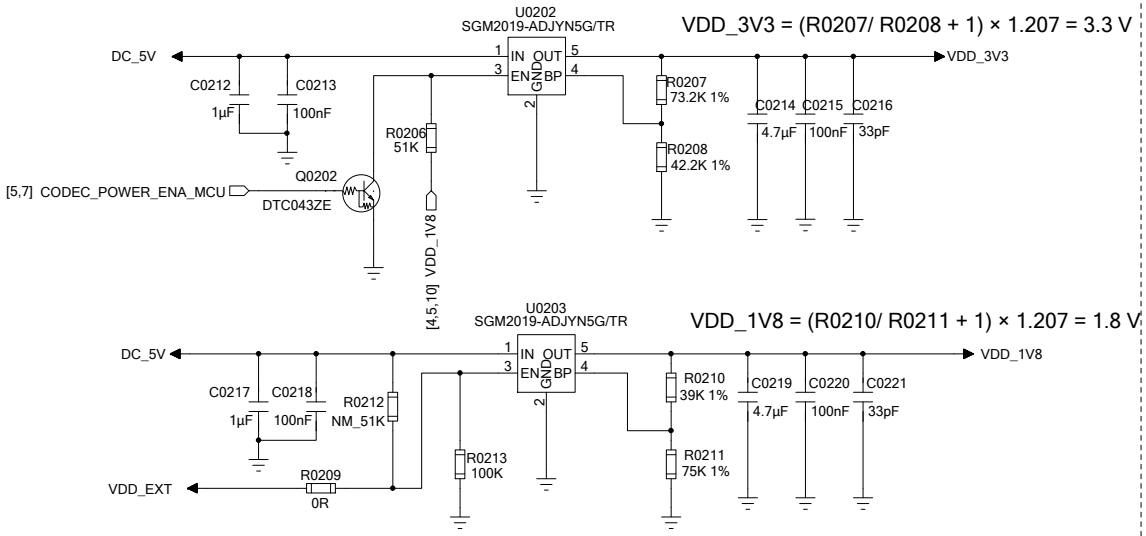
VBAT Design



NOTE:

Select a ferrite bead for R0226, and place it as close to VBAT_MODULE as possible. R0226 requirements:
(1) Current Rating ≥ 600 mA; (2) ≥ 800 Ω impedance @ 700-960 MHz.
(3) Low DC resistance to avoid voltage drop during instantaneous high power consumption.

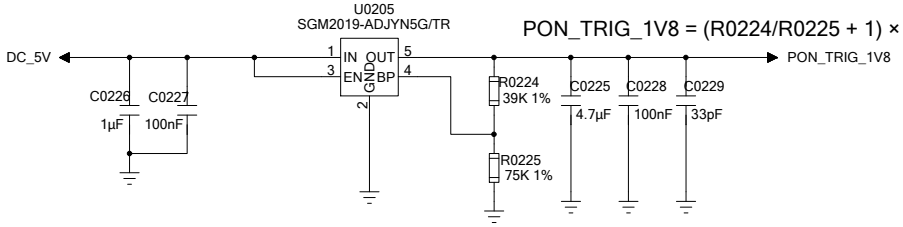
Audio Codec Power Supply



NOTE:

1. CODEC_POWER_ENA_MCU must be at low level to ensure the normal output voltage of VDD_3V3. If CODEC_POWER_ENA_MCU is at high level, VDD_3V3 power supply will be switched off.
2. The following power-on/off sequences should be followed to ensure the audio codec works normally.
   Power-on sequence: power on VDD_1V8 first, and then VDD_3V3.
   Power-off sequence: power off VDD_3V3 first, and then VDD_1V8.

PON_TRIG Power Supply



NOTE:

PON_TRIG is powered by an external LDO.

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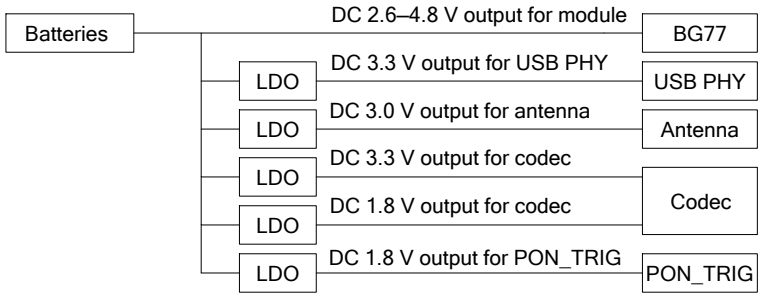
Power Supply Design (Battery)

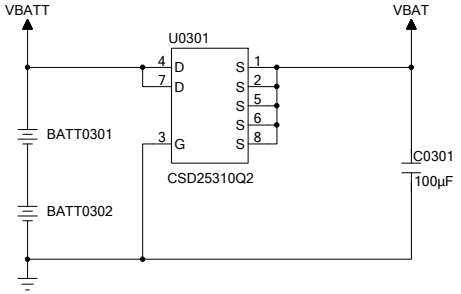
Battery Application



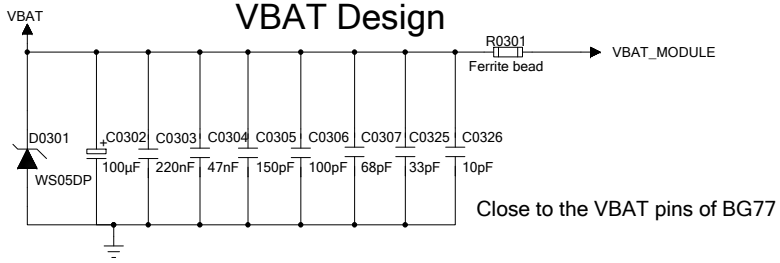
NOTE:

1. You can select either the standard power supply design or the battery power supply design according to your specific application demands.
2. The output voltage of batteries must be 2.6–4.8 V.

Battery Polarity Protection Design



VBAT Design

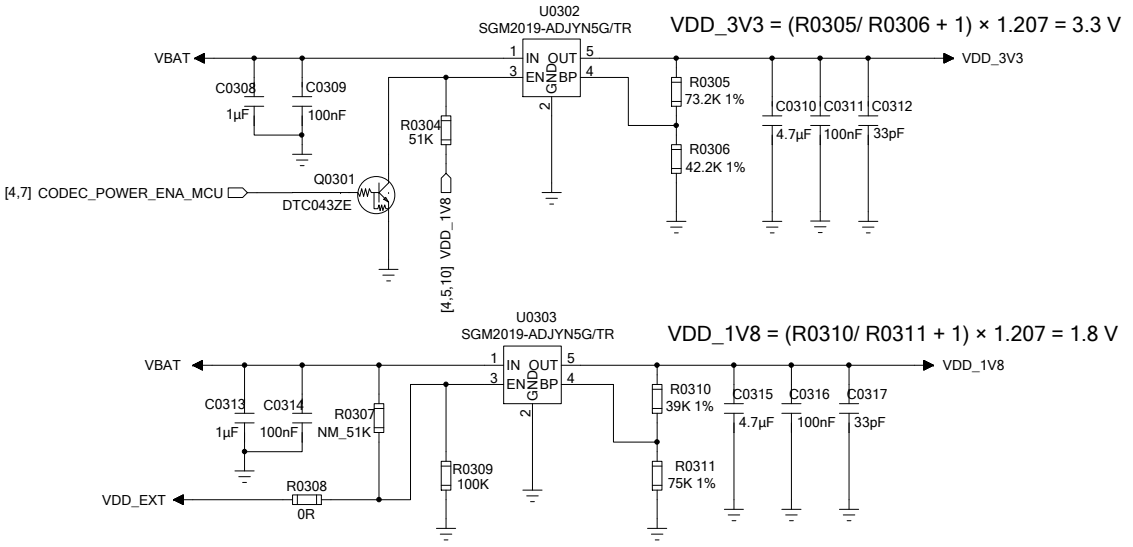


Close to the VBAT pins of BG77

NOTE:

Select a ferrite bead for R0301, and place it as close to VBAT as possible. R0301 requirements :
(1) Current Rating ≥ 600 mA; (2) ≥ 800 Ω impedance @ 700-960 MHz.
(3) Low DC resistance, to avoid voltage drop during instantaneous high power consumption.

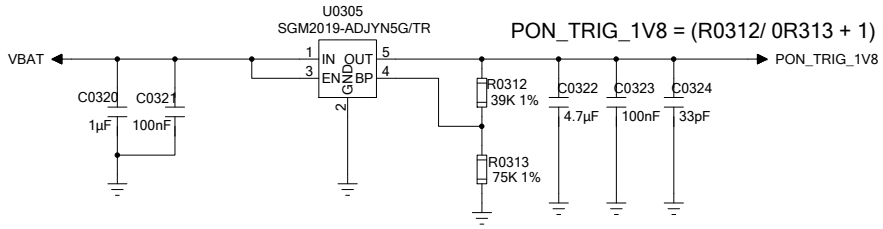
Audio Codec Power Supply



NOTE:

1. CODEC_POWER_ENA_MCU must be at low level to ensure the normal output voltage of VDD_3V3. If CODEC_POWER_ENA_MCU is at high level, VDD_3V3 power supply will be switched off.
2. The following power-on/off sequences should be followed to ensure the audio codec works normally.
   Power-on sequence: power on VDD_1V8 first, and then VDD_3V3.
   Power-off sequence: power off VDD_3V3 first, and then VDD_1V8.

PON_TRIG Power Supply



NOTE:

PON_TRIG is powered by an external LDO.

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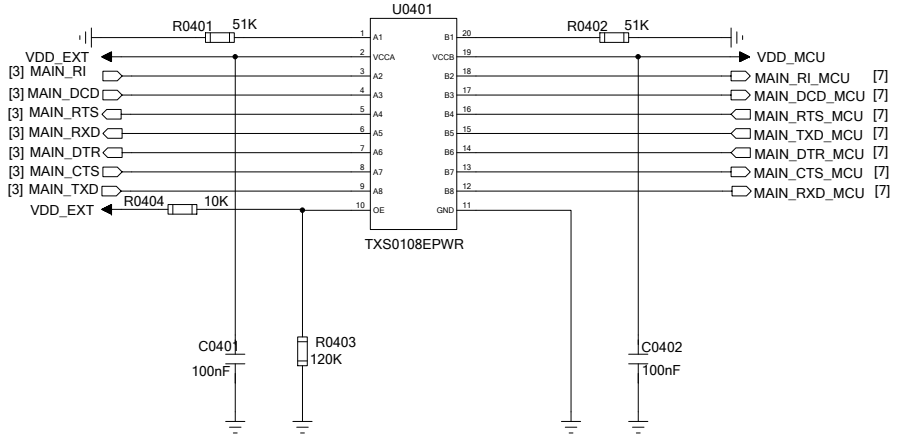
UART & USB Interfaces Design

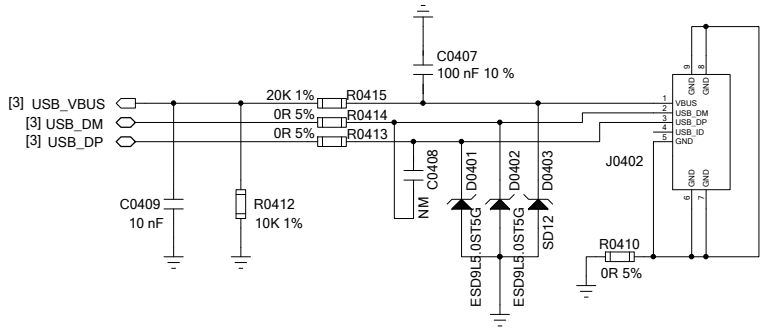
UART Level-shifting Circuit



NOTE:

1. It is recommended to use a voltage-level translator TXS0108EPWR between BG77 and MCU.
2. VCCA should not exceed VCCB. For more information, see the datasheet from Texas Instruments.

USB Interface Design



NOTE:

1. The junction capacitance of the ESD protection devices should be less than 2 pF.
2. It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.

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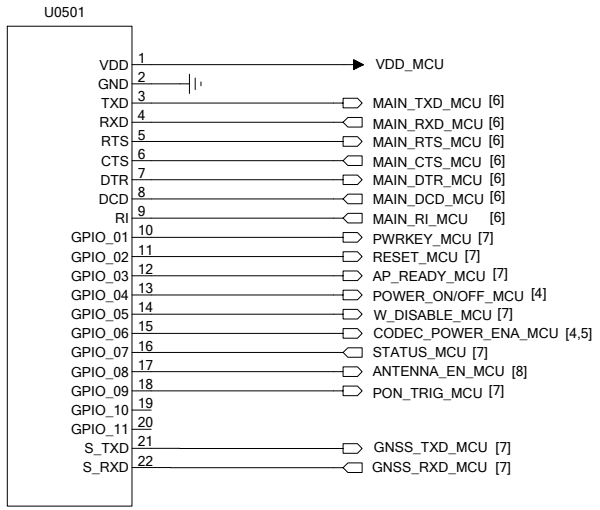
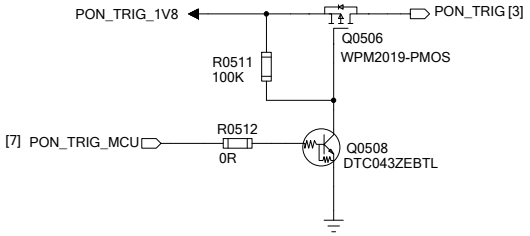
MCU Interfaces Design

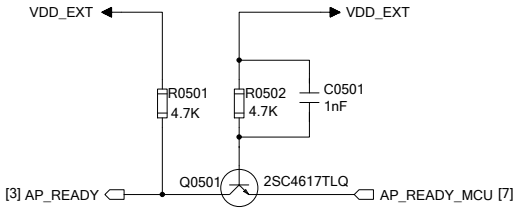


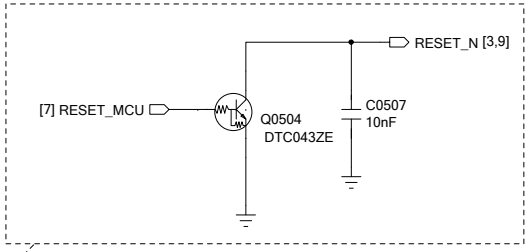
NOTE:

1. U0501 represents your MCU.
2. Pay attention to the UART interface connection of RTS/CTS.
3. When BG77 module enters PSM, set MCU's UART interface into the high-impedance mode.

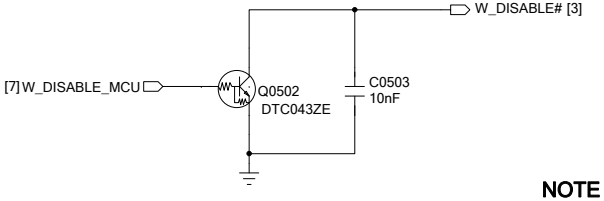
PON_TRIG Design

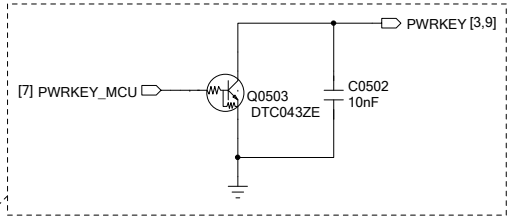




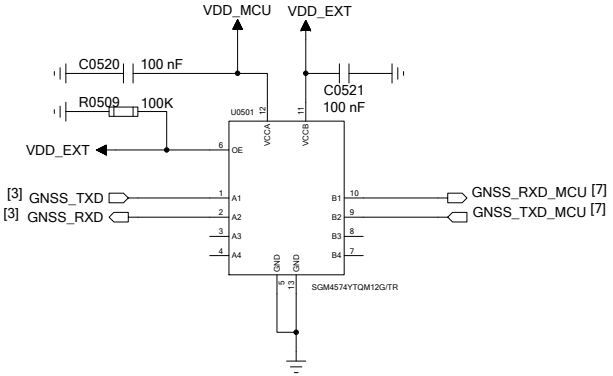


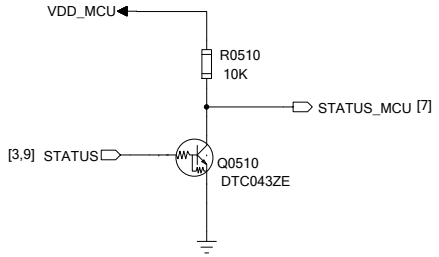
NOTE 1





NOTE 2





State	STATUS	STATUS_MCU
Power-off	0	1
Power-on	1	0

NOTE:

1. The module can be reset by driving RESET_N low for 2–3.8 s.
2. Driving PWRKEY low for 500–1000 ms, the module will be turned on.
   Driving PWRKEY low for 650–1500 ms, the module will be turned off.
   Never pull down PWRKEY to GND permanently.

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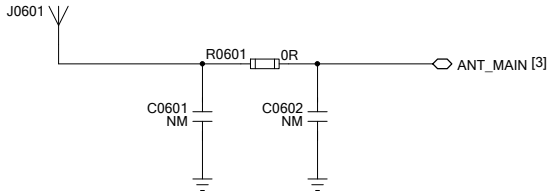
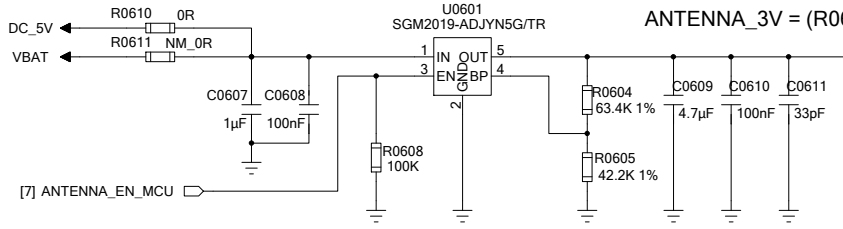
Antenna Interfaces Design

Main Antenna Interface



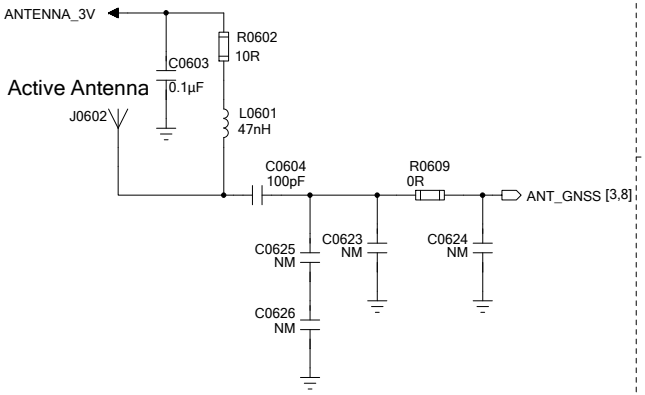
Antenna Power Supply



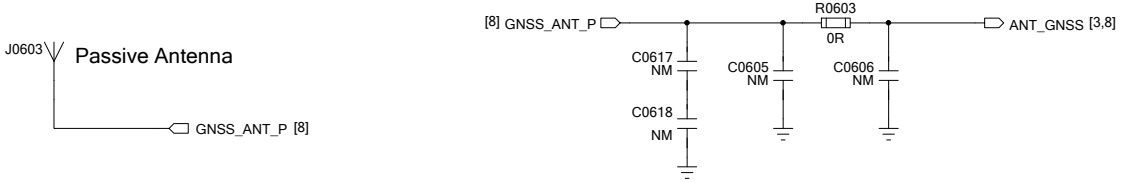
	R0610	R0611
Standard solution	Mount	NM
Battery solution	NM	Mount

GNSS Antenna Interface

Active Antenna Design

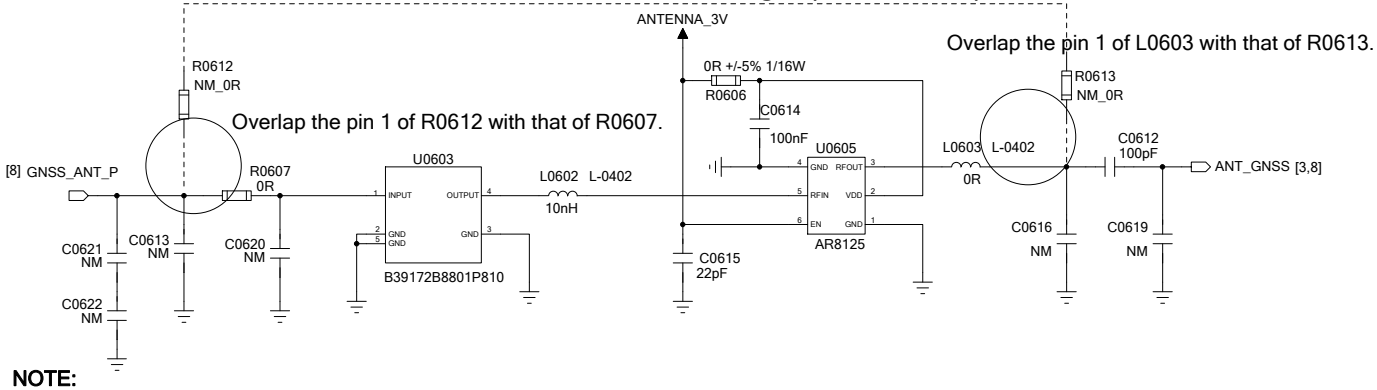


Passive Antenna Design (Solution 1)



NOTE:
This solution is ideal for compact-sized applications where the cable insertion loss from the module to the antenna is small.

Passive Antenna Design (Solution 2)



NOTE:
This solution is ideal for applications where the cable insertion loss from the module to the antenna is large and external LNA and SAW are needed.

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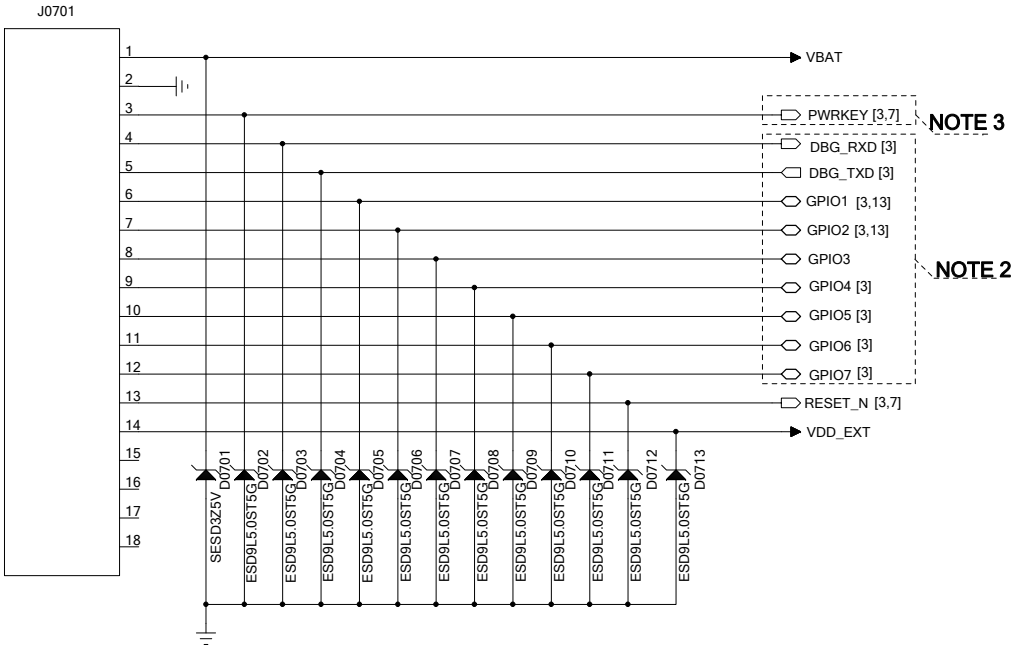
Test Points and Indicators

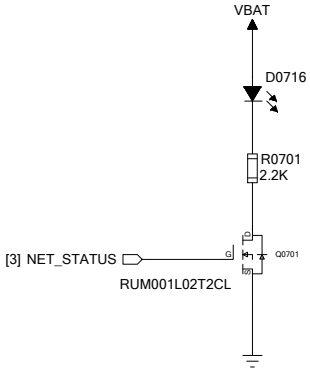
Reserved Test Points

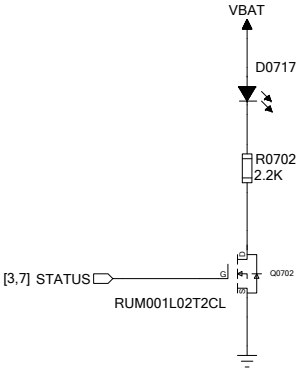


NOTE:

1. It is recommended to reserve the test points for debug UART interface for future software debugging.
2. The voltage level of debug UART interface and GPIO interfaces is 1.8 V.
   Do not connect them directly to a 3.3 V level.
3. PWRKEY should never be pulled down to GND permanently.

Indicators





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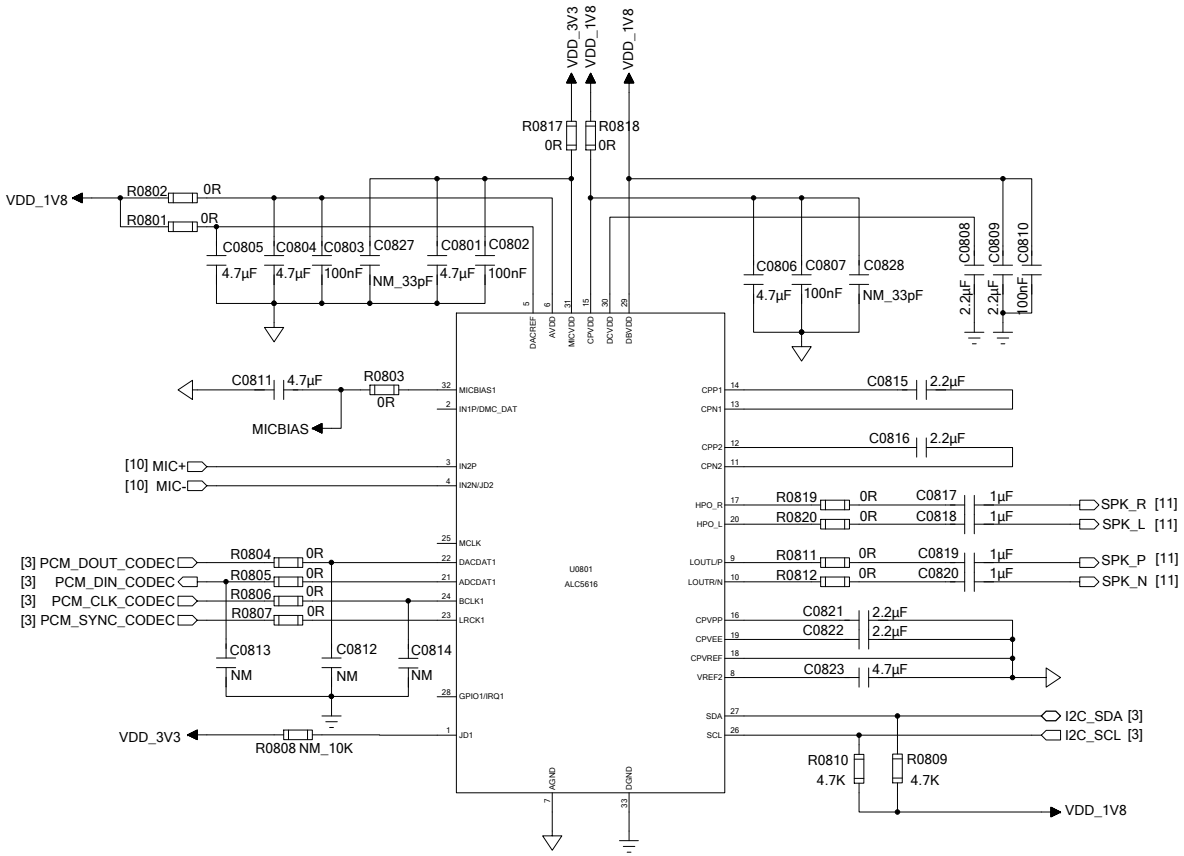
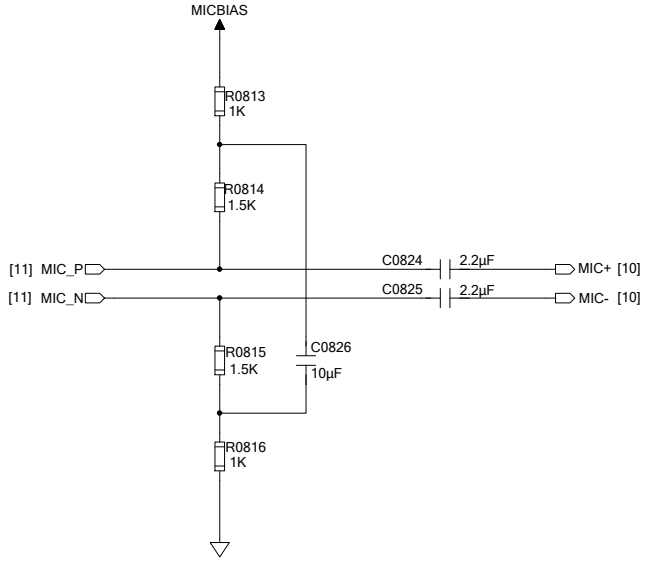
Audio Codec Design





NOTE:

1. To ensure that ALC5616 works normally, follow the power-on and power-off sequences of its power supply.
   Power-on sequence: power on DBVDD/AVDD/DACREF/CPVDD first, and then MICVDD.
   Power-off sequence: power off MICVDD first, and then DBVDD/AVDD/DACREF/CPVDD.
   For more details, see ALC5616 datasheet.
2. BG77 module will automatically initialize the codec via I2C interface after the module is turned on successfully, so all power supplies for the codec need to be switched on before that.

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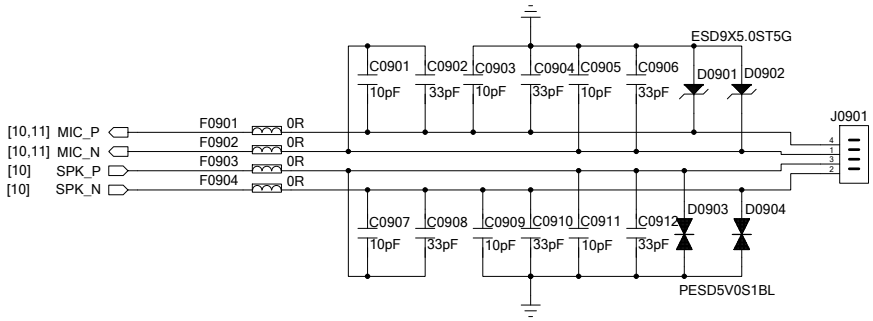
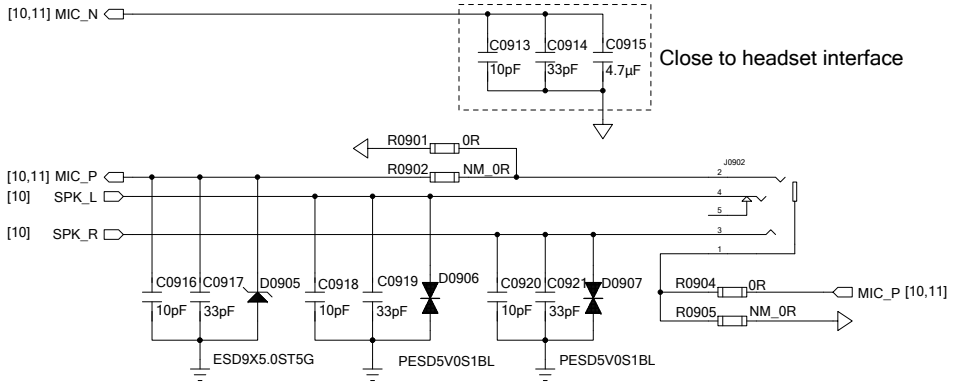
Audio Interface Design

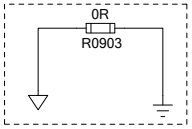
Handset Application



Headset Application



Separate analog ground and digital ground



	CTIA	OMTP
R0902/R0905	NM	Mount
R0901/R0904	Mount	NM

NOTE:

1. The analog output only drives headset and handset. For larger-power loads such as loudspeakers, an audio power amplifier needs to be added in the design.
2. The maximum capacitive loading for loudspeaker is 330 pF and that for microphone is 250 pF.
3. In handset application, both the microphone and loudspeaker signal traces need to be routed as differential pairs.
4. In headset application, the microphone signal traces need to be routed as differential pairs.
5. All microphone and loudspeaker signal traces should be routed with ground surrounded and far away from noise signals such as clock and DC-DC signals, etc.
6. The 0 Ω resistor (R0903), which separates analog ground and digital ground, suppresses loop current and reduces noise interference.

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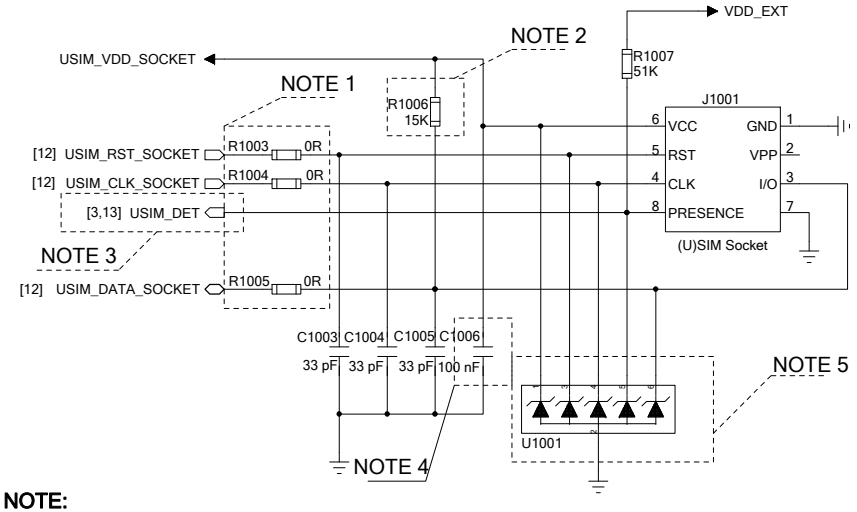
(U)SIM Interface Design (1.8 V Only)

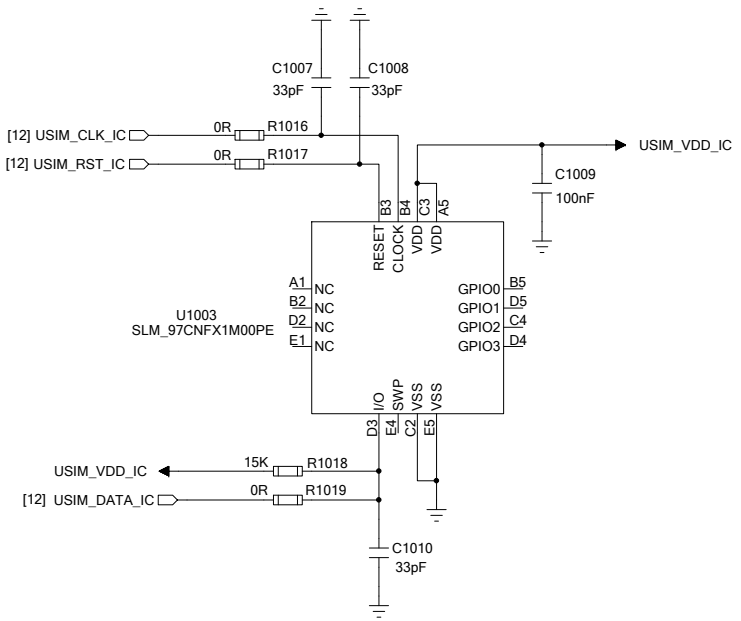
(U)SIM Card Socket Design



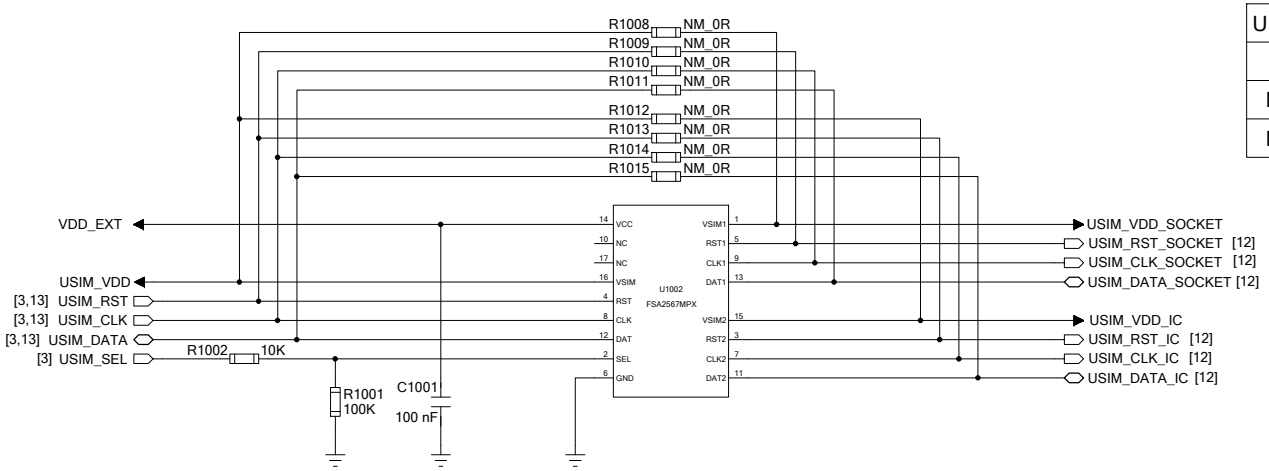
NOTE:

1. R1003–R1005 are applied to facilitate debugging. It is recommended to reserve the series resistors for (U)SIM signals of the module.
2. The pull-up resistor (R1006) on USIM_DATA trace can improve anti-jamming capability.
3. BG77 supports (U)SIM card hot-plugging, which can be implemented through USIM_DET pin.
4. The value of C1006 should be less than 1 μF.
5. The parasitic capacitance of the TVS array should not exceed 15 pF.

eSIM Design (1.8 V Only)



Analog Switch for (U)SIM Interface



U1002	R1008–R1011	R1012–R1015	
M	NM	NM	Switch + Socket/eSIM IC
NM	M	NM	Single Socket
NM	NM	M	Single eSIM IC

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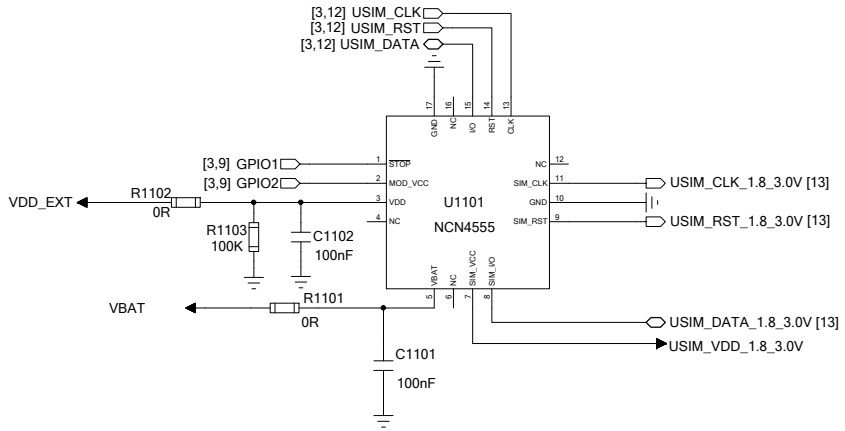
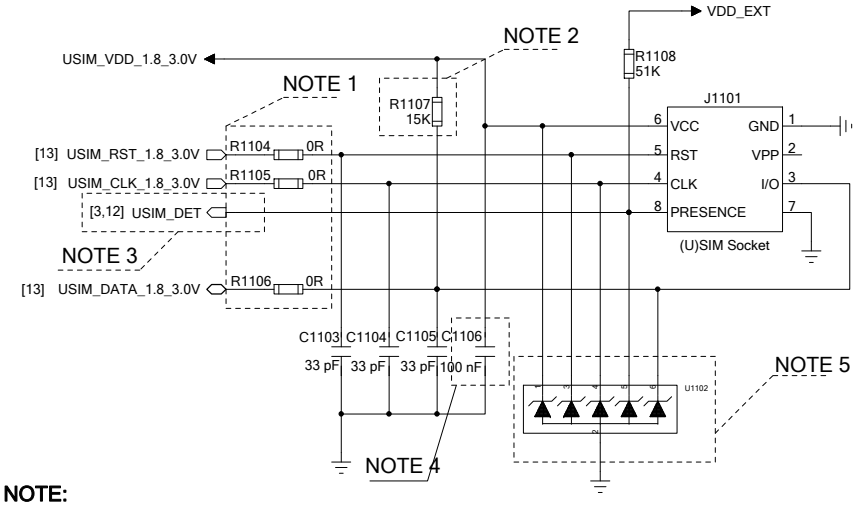
(U)SIM Interface Level-shifting Circuit Design (1.8/3.0 V)

(U)SIM Interface Level-shifting Circuit Design



STOP#	MOD_VCC	Description
Low	Low/High	Shutdown mode
High	Low	SIM_VCC = 1.8 V. 1.8 V (U)SIM card is supported (default).
High	High	SIM_VCC = 3.0 V. 3.0 V (U)SIM card is supported.

(U)SIM Card Socket Design



NOTE:

1. R1104–R1106 are applied to facilitate debugging. It is recommended to reserve the series resistors for (U)SIM signals of the module.
2. The pull-up resistor (R1107) on USIM_DATA trace can improve anti-jamming capability.
3. BG77 supports (U)SIM card hot-plugging, which can be implemented through USIM_DET pin.
4. The value of C1106 should be less than 1 μF.
5. The parasitic capacitance of the TVS array should not exceed 15 pF.

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