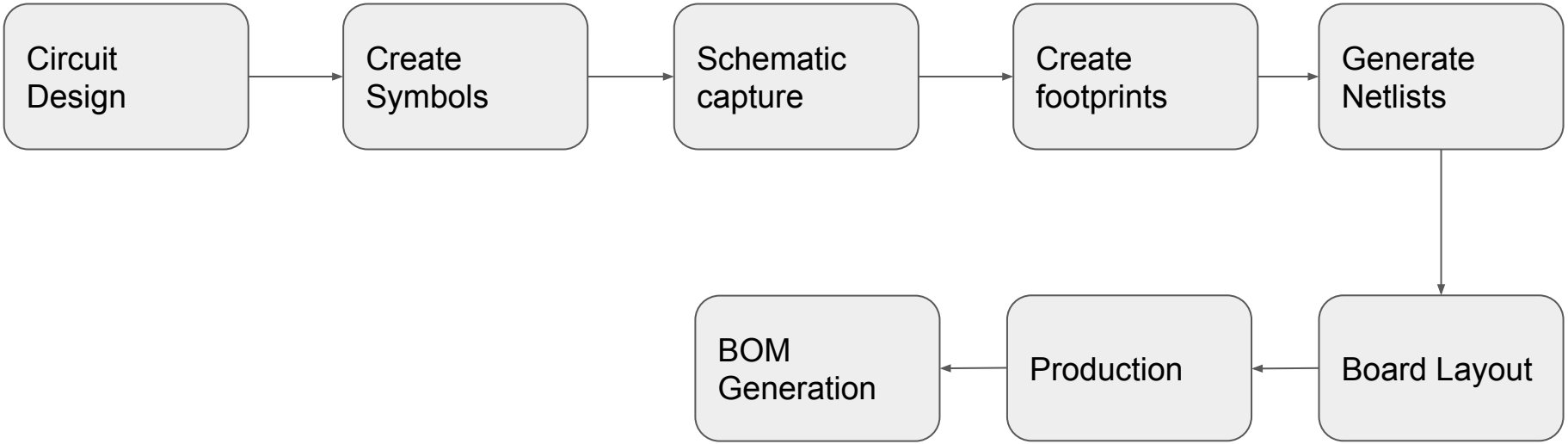
PCB Design Crash Course in KiCAD

Process


Circuit Design
Create Symbols
Schematic capture
Create footprints
Generate Netlists
Board Layout
Production
BOM Generation

What are PCBs and how are they made?

- Electrical connection and mechanical support
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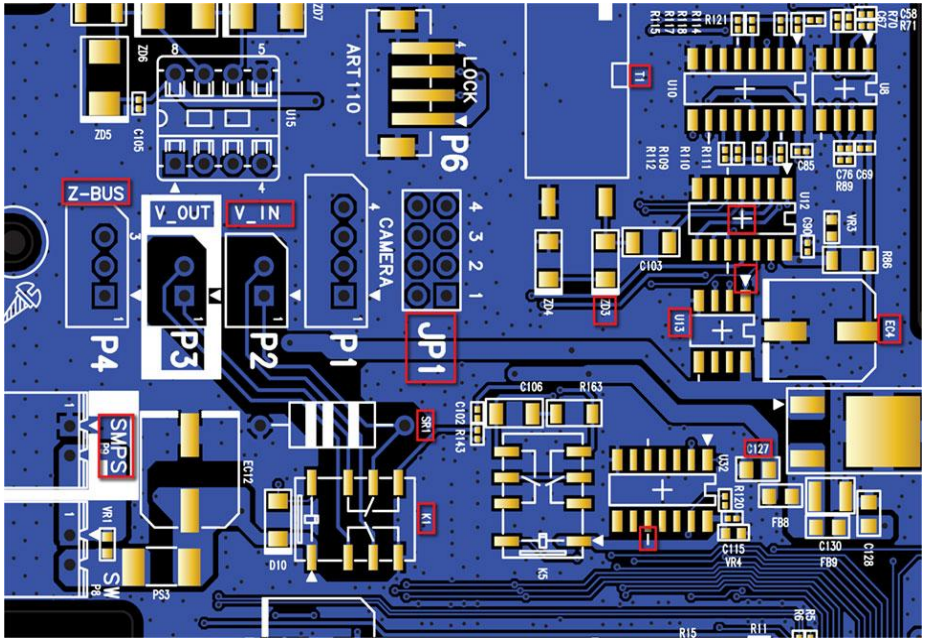


Layers

- Silkscreen
- Soldermask
- Copper
- Substrate
- Copper
- Soldermask
- Silkscreen

Part 1: Effective circuit design

Consider:

- Digital sections - e.g NAND GATE, NOR GATES etc
- Analog sections - think RF
- Mixed signal sections - ADC, DACs etc
- High speed signals - (*mainly digital, USB, ethernet, PCIe)*

- Group into respective sections - (trick: fully connected wires make it easier to debug a schematic) (tv schematic)
- Multi-sheet schematics - use global/hierarchical connectors
- Application notes
- Screw sizes, test-points etc

Few schematic tips

- Use symbols you are familiar with - IEEE symbols vs IEC - all softwares provide all - a matter of preference
- No crossing wires - unless no other option - if crossed, dot indicates connected, no dot - not connected
- Use full length wires
- Block diagram from hardware design
- Think design flow - left-right
- Don’t play Tetris with a schematic
- Application notes - truth tables, expected ripple, config tables etc
- Name your nets - it’ll save you during debugging
- Watch your capacitors - polarized - non-polarized

Let’s do it!

Part 2: Creating symbols and footprints, Routing and Basic signal integrity

Part 2.1: Creating symbols and footprints

- Sometimes symbols and footprints you need are not available
- Options - download online - SnapEDA
- Create your own - some modules are overly custom
- OLED screen 0.96”

Let’s create one!

Part 2.2: Routing and basic signal integrity

What is signal integrity?

- The challenges posed by ensuring that wires carry correct, uncorrupted values

Most important things to consider

1. Clearances
2. Trace geometry
3. Via sizes
4. Impedance

Trace width

-Determine the width you need. Depends on whether impedance control is needed

-Impedance depends on

a. Dielectric material
b. Thickness of dielectric

-Chose width that does not violate design rules

-Impedance matching(can be researched)

How do you choose trace width

-Choose width based on

a. Hitting impedance target
b. Ensure you carry enough current-polygons are preferred at high current above 1A - KICAD tool to calculate this
c. Trace density - densely packed board? Use thinner traces (No-brainer)

Trace units

-Mils - very common

-mm - also common

- Wider width lowers DC resistance,
- prevents DC power loss
- Prevent heating of the trace

Trace angles

- Routing myth - 90 deg angles create a lot of noise - **Exception** - Frequencies of 10GHz and above
- Preferred angles - 45 deg

Trace angles for SMT

- For SMT, when the incoming trace is widget at the pad, the SMT entry should be straight into the pad

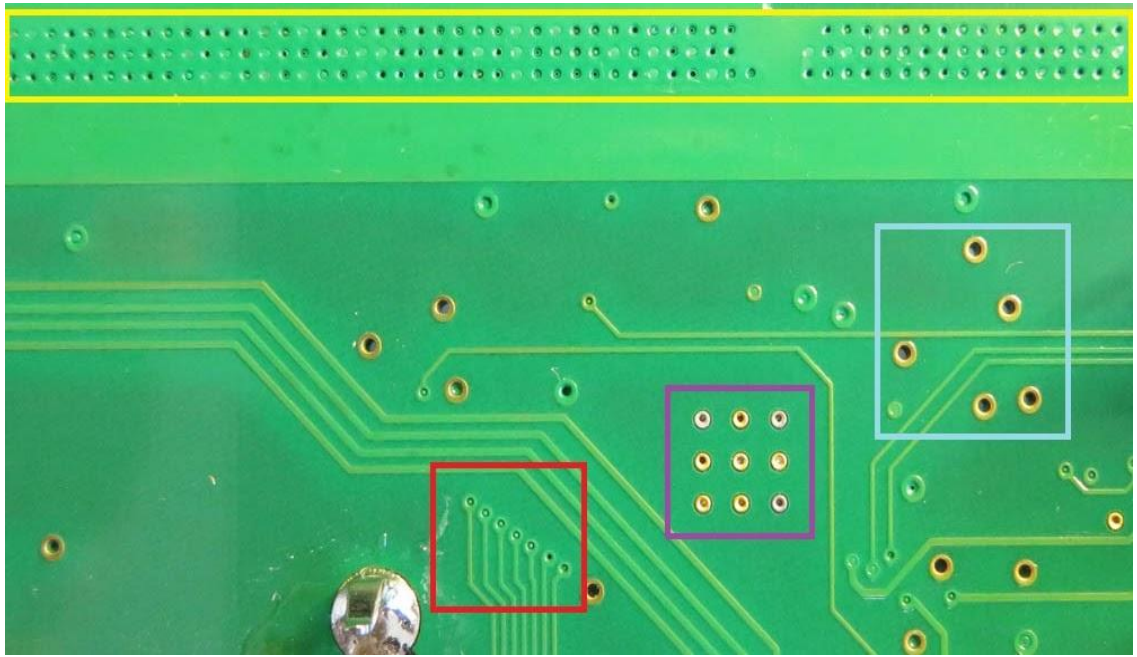
Standard way to route SMT:

a. Straight entry
b. Corner SMT entry

- If a design rule e.g Impedance needs a thicker trace, you can route a very short section into the pad that is thinner, while leaving the reas of the trace thick

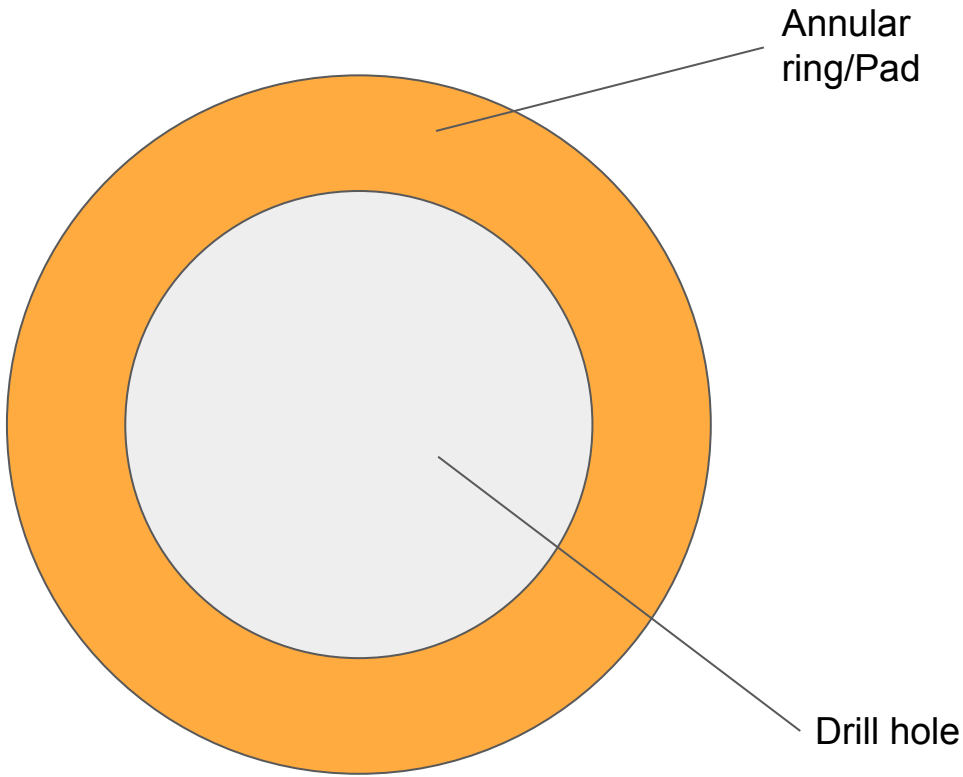
Polygons - copper pours

1. Used for ground and power nets to reduce the inductance- Conductor physics
2. Heat dissipation - Thermal tenting - most commonly seen on voltage regulators, CPUs etc
3. Impedance control for HF signals - for example decoupling capacitors that need to remove noise from the power supply line
4. A polygon can carry more current than a trace



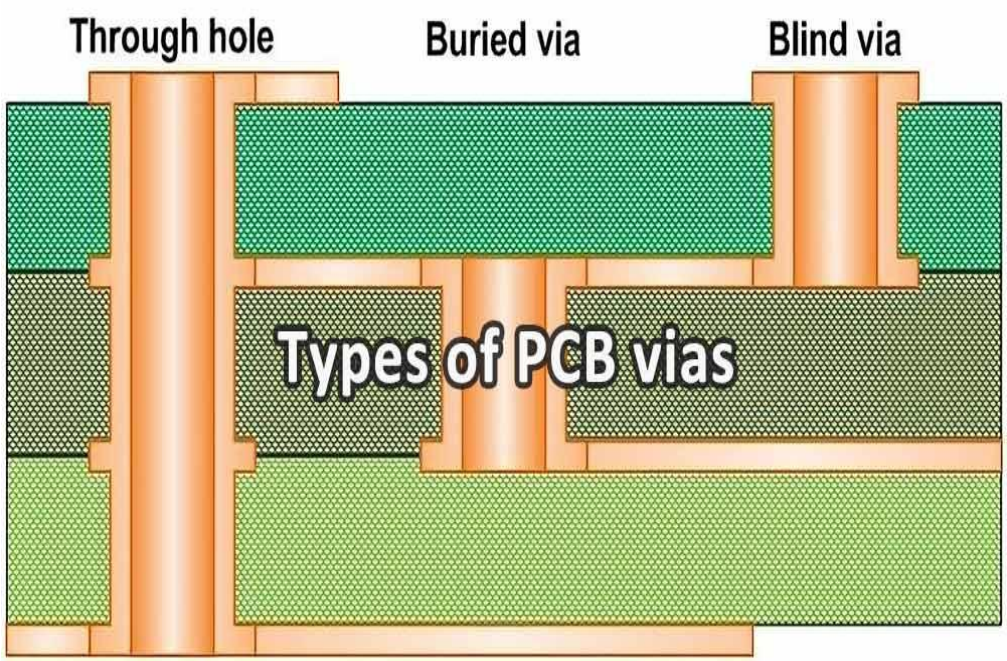
Vias

- Via -> Through
- Holes
- Set up via sizes during the design rule stage

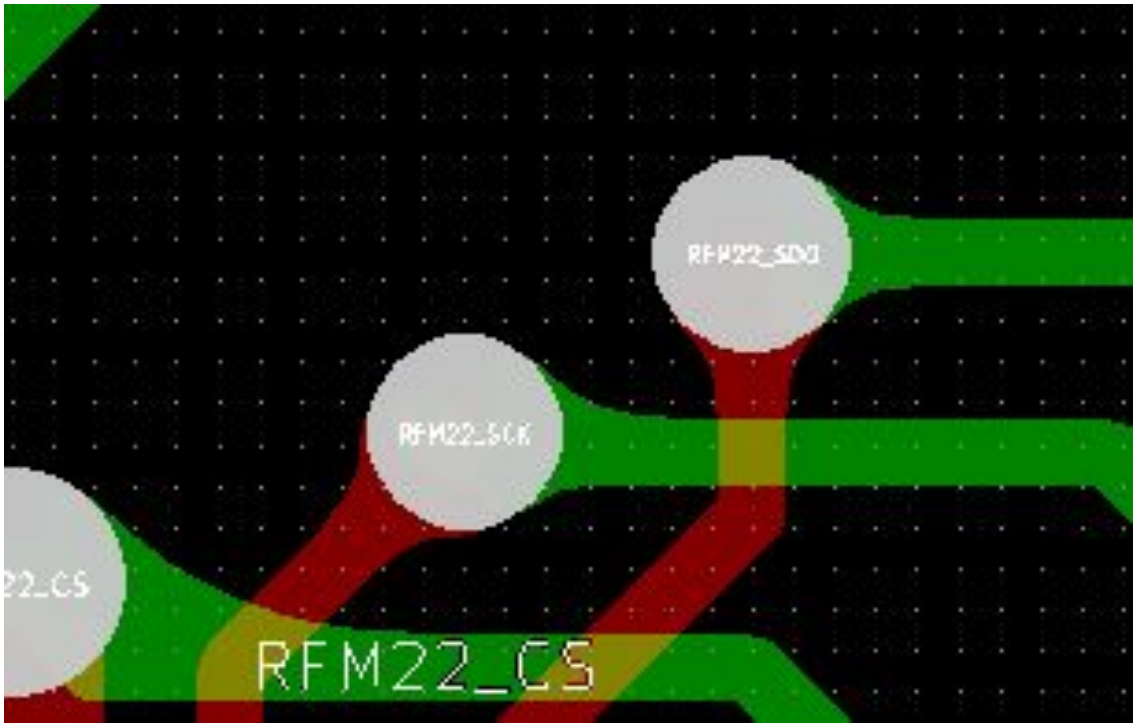


Via types

- Blind- top + internal layer
- Buried - Internal layers
- Through - top and bottom
- Micro - High layer boards



Teardrops



- Adding extra-copper around vias
- Usage - improve reliability of the via during manufacturing
- In case the drill bit does not hit the exact point

Component placement and arrangement

Tips

1. Place decoupling capacitors close to the IC
2. Place crystals close to the IC - never route a clock signal under any component
3. Use datasheets for IC layout
4. Avoid routing traces under inductive and capacitive components
5. Place analog and digital sections AWAY! from each other
6. Place ground vias and power vias in pairs - current return path
7. Avoid parallel paths to reduce cross-talk
8. Silkscreen - guide when soldering and for users - use it to label components
9. Watch component height

Let’s do it!

Part 3: High Speed Routing and Electromagnetic Interference (EMI) techniques

1. USB
2. I2C
3. UART
4. SPI

Part 4: PCB manufacturing

- Important files

a. Fabrication files

b. BOM

c. Drill files

- Fiducials
- PCB Assembly
- Turn keying
- Soldering