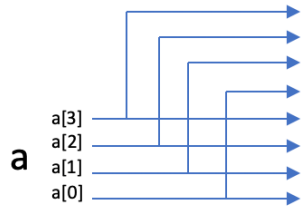
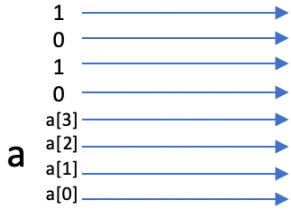
Bit Concatenation in SystemVerilog

```
logic[3:0] a;

// Assume a had the value 0001 on its wires
// Then {a, a} would be 00010001
```




```
// And, {4'b1010, a} would be 10100001
```




```
// If a was 0001 then:
//            {a[1:0], a[1:0], 4'b1010} would be 01011010
```

Sign Extension in SystemVerilog

Just concatenate the MSB of the signal onto the left to make a copy of it.

```
logic[3:0] a;

// {a[3], a} will be:
```

FINAL NOTE: you are creating new bundles of wires as you do this, NOT copying 1's and 0's…