

Two-Stage Operational Amplifier

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1 Introduction

Our goal is to design a two stage operational amplifier with the following topology:

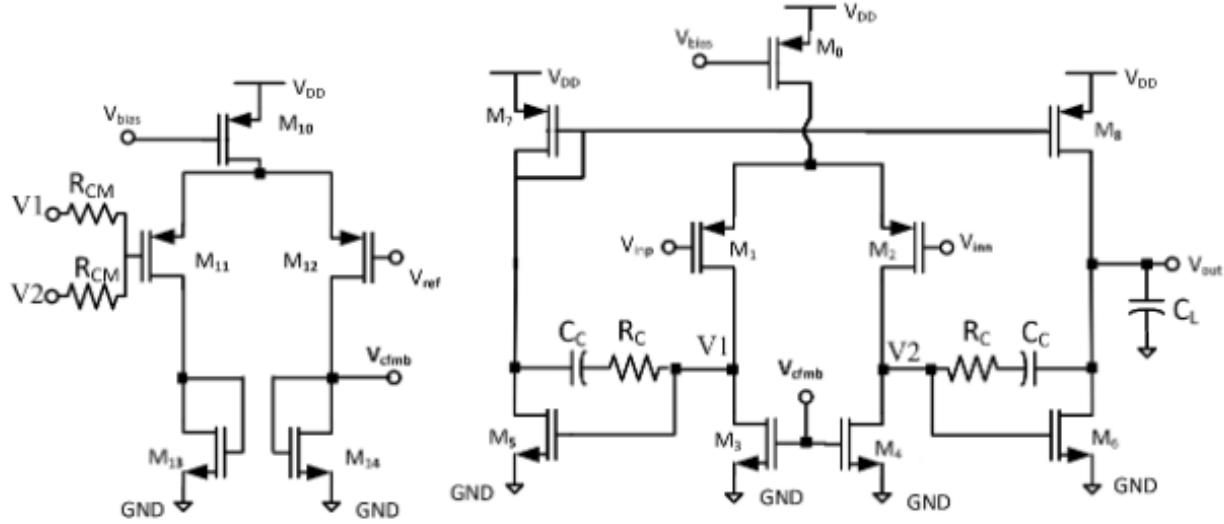


Figure 1: Operational Amplifier Design Schematic

that could achieve the following performance specifications and design constraints:

Specification	Value
V_{DD}	1.0 V
GND	0 V
Load capacitance C_L	2 pF
Nominal input common-mode (DC level)	$V_{DD}/2$
Nominal output common-mode (DC level)	$V_{DD}/2$
Two-stage power consumption	$\leq 0.4 \text{ mW}$
CMFB circuit power	$\leq 40 \mu\text{W}$
Differential output swing	$\geq 0.75 \text{ V}$
Low-frequency differential gain	$\geq 46 \text{ dB}$
Small-signal unity-gain frequency	$\geq 600 \text{ MHz}$
Phase margin	$60^\circ \leq \text{PM} \leq 90^\circ$
Slew rate	$\geq 20 \text{ V}/\mu\text{s}$

while also adhering to the following design constraints:

Constraint	Limit
Maximum transistor length	$5 \times L_{\min}$
Maximum width per multiplier	4 μm
Maximum multiplier of transistors	50

2 Methodology

We have a two stage amplifier so we should design our op amp in two stages. Considering the power budget, we design for around $100 \mu\text{A}$ in each branch. We want a swing of 750 mV in the second stage and likely a gain of around 10-15. Then, the first stage should have a swing of around 75 mV and a single ended gain around 15-20. To aid in the design process, we plot $I_d - V_{ds}$ curves of reference devices. Here we plot the curves for $W_{ref} = 1440 \text{ n}$ ($12 \times W_{min} = 12 \times 120 \text{ n}$ for a highly composite multiple of the minimum width). Clockwise from top left: nmos_svt, pmos_svt, nmos_lvt, pmos_lvt.

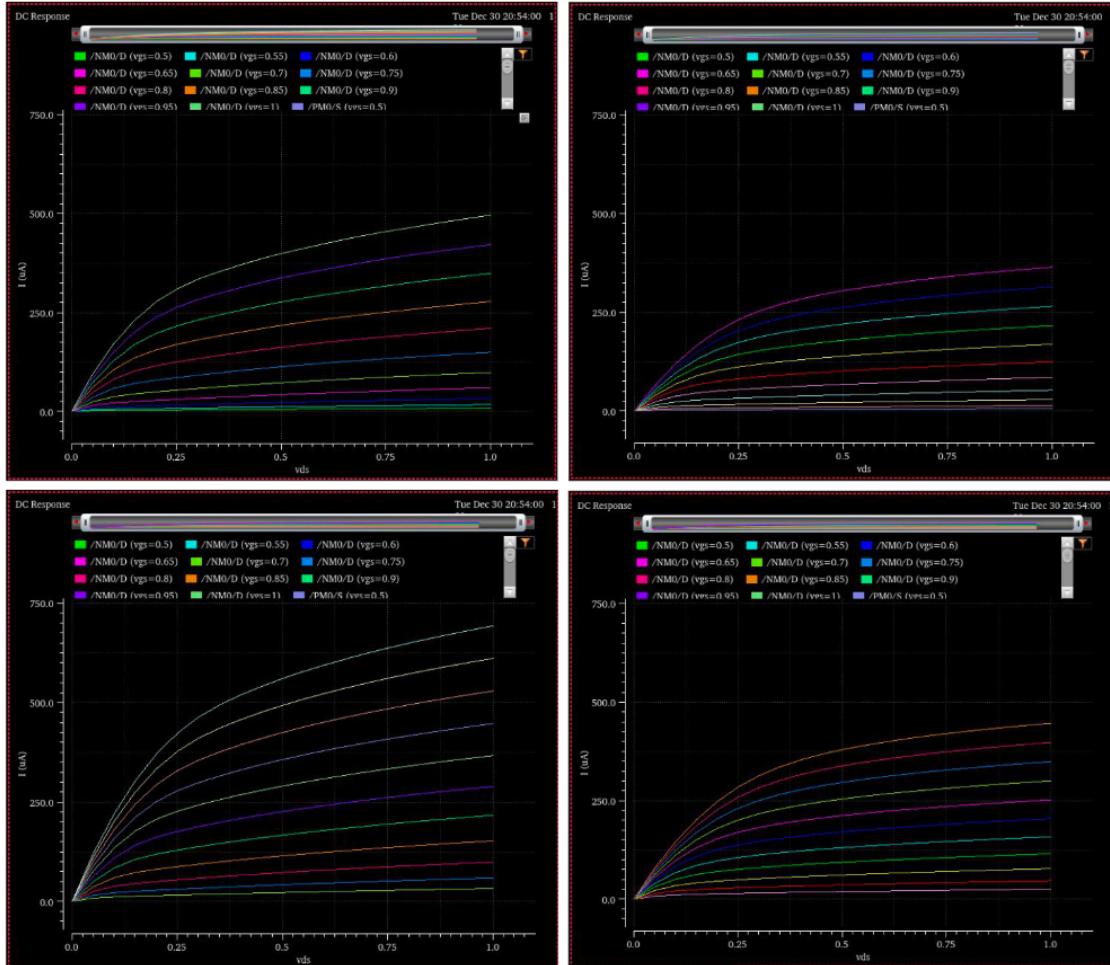
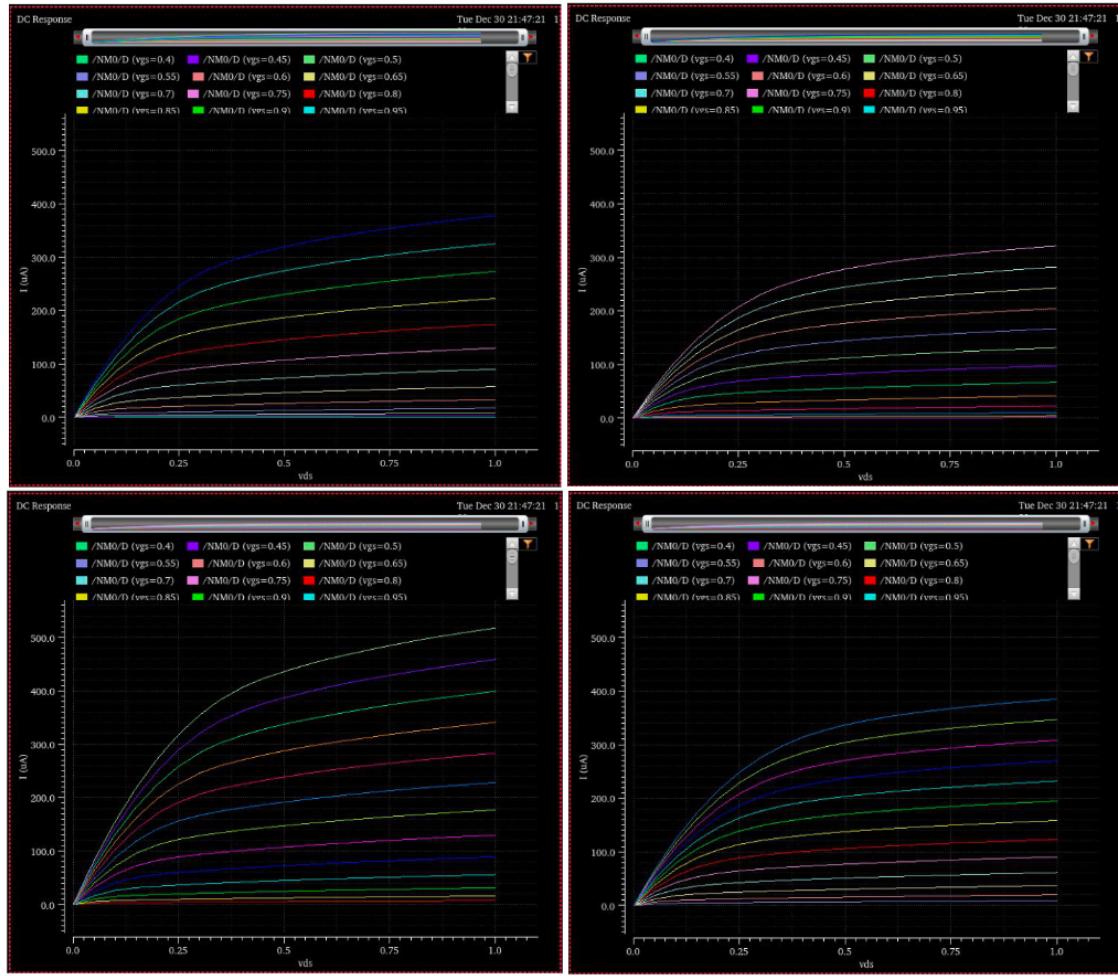
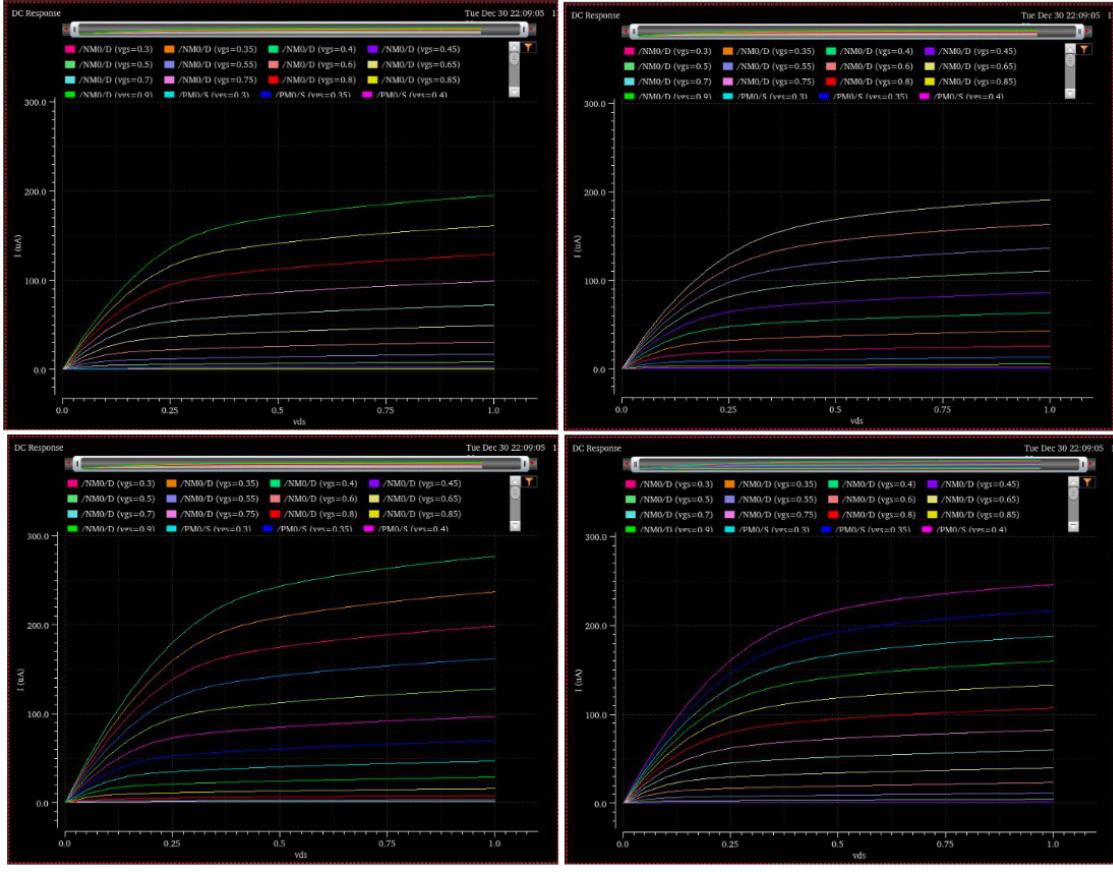


Figure 2: $L = L_{\min} = 45 \text{ n}$

Figure 3: $L = 2 \times L_{min} = 90 \text{ n}$

Figure 4: $L = 4 \times L_{min} = 180$ n

2.1 Stage One

First, starting with W_{ref} and L_{min} , we see $M0$ is in subthreshold because there is not enough headroom ($V_{ov0} + V_{ov12} + V_{ov34} = V_{dd} - V_{swing}$). We design for $V_{ov0} = 100$ mV using $V_{bias} = 0.5$ V to allow adequate headroom. V_{ov34} depends on V_{gs6} so we need to find the proper voltage to make $V_{ds6,min} = 125$ mV and $I_{ds} = 100 \mu\text{A}$ by looking at the $I_{ds} - V_{ds}$ plots. This ended up being approximately 500 mV so we set $V_{ref} = 500$ mV to start with (see Common Mode Feedback Circuit for explanation).

Using low threshold devices for all transistors and increasing the lengths of $M1, 2$ and $M3, 4$ to $5 \times L_{min} = 225$ n puts all the devices in saturation. To utilize the $200 \mu\text{A}$ allotted to the first stage, we scale all of the devices by 18. The calculated differential gain is $g_{m1,2}(r_{outN} || r_{outP}) = 1.9m(15k || 19k) \approx 30$ and we can graph the outputs to confirm if our swing is adequate (around 15 gain and 150 mV swing).

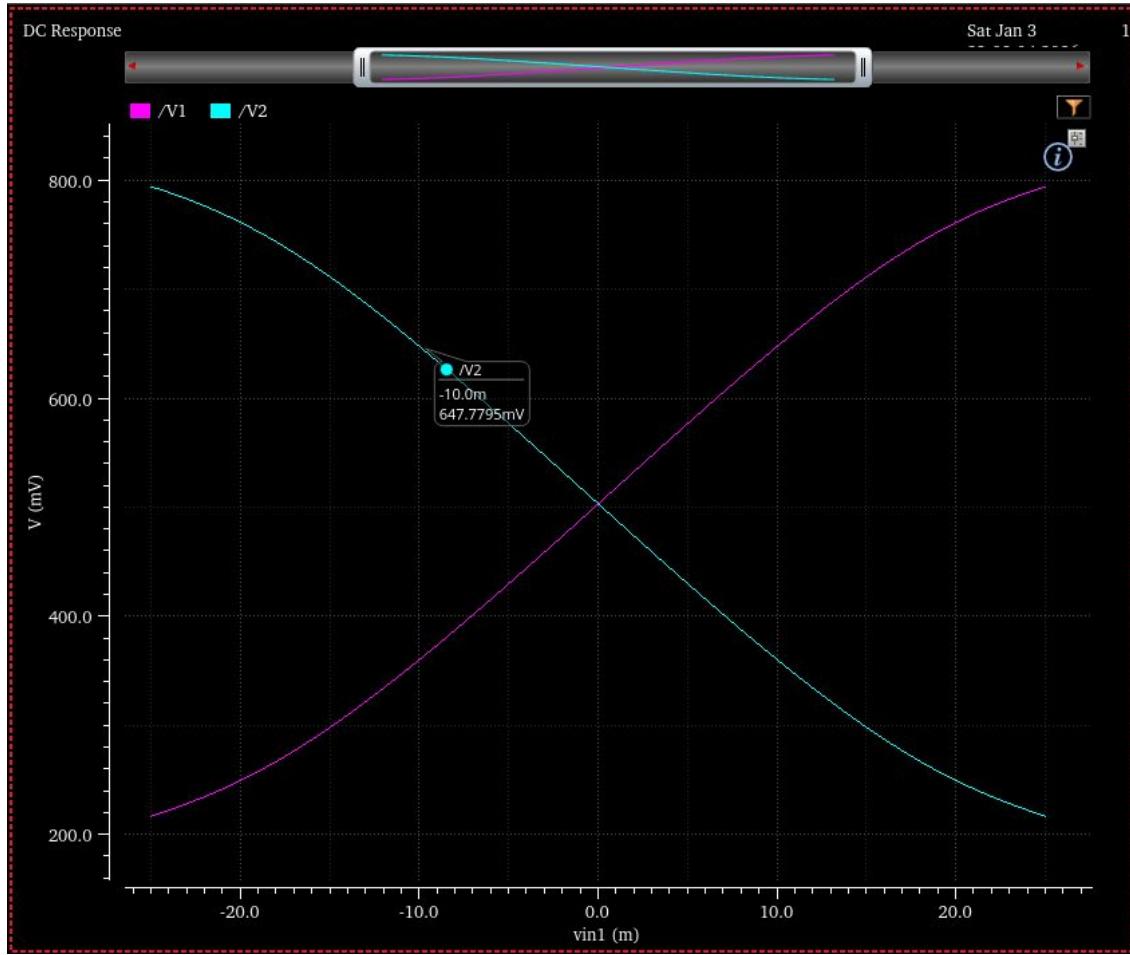


Figure 5: Stage 1 Differential Outputs

2.1.1 Common-Mode Feedback Circuit

The common-mode feedback circuit sets the common mode of the output to a particular value V_{ref} . For a normal differential amplifier, there is no restriction the common mode of the output. The way the CMFB circuit remedies this is by raising or lowering V_{cmfb} to counter the normal behavior of the circuit. If the sensed common mode (average of V_1 and V_2) is too high, then V_{cmfb} is increased which causes the output NMOS to pull the common mode down. If the sensed common mode is too low, then v_{cmfb} is decreased which causes the output PMOS to pull the common mode up.

This means our V_{ref} should be around 0.52 V (it may need some adjusting after second stage is designed). To make the common mode feedback circuit all in saturation it required changing $M11, 12, 13, 14$ to have lengths of $4 \times L_{min} = 180$ n.

2.2 Stage Two

We consider the common mode of the first stage output is around 520 mV to make our test bench and do a similar process for the second stage. Scaling the devices by 3 uti-

lizes around $100 \mu\text{A}$ in the left and the right branches as intended. The calculated gain is $g_{m6}(r_{outN}||r_{outP}) = 890u(27k||27k) \approx 24$ and we can graph the output to confirm if our swing is adequate (the gain actually seems closer to 15 and 150 mV swing).

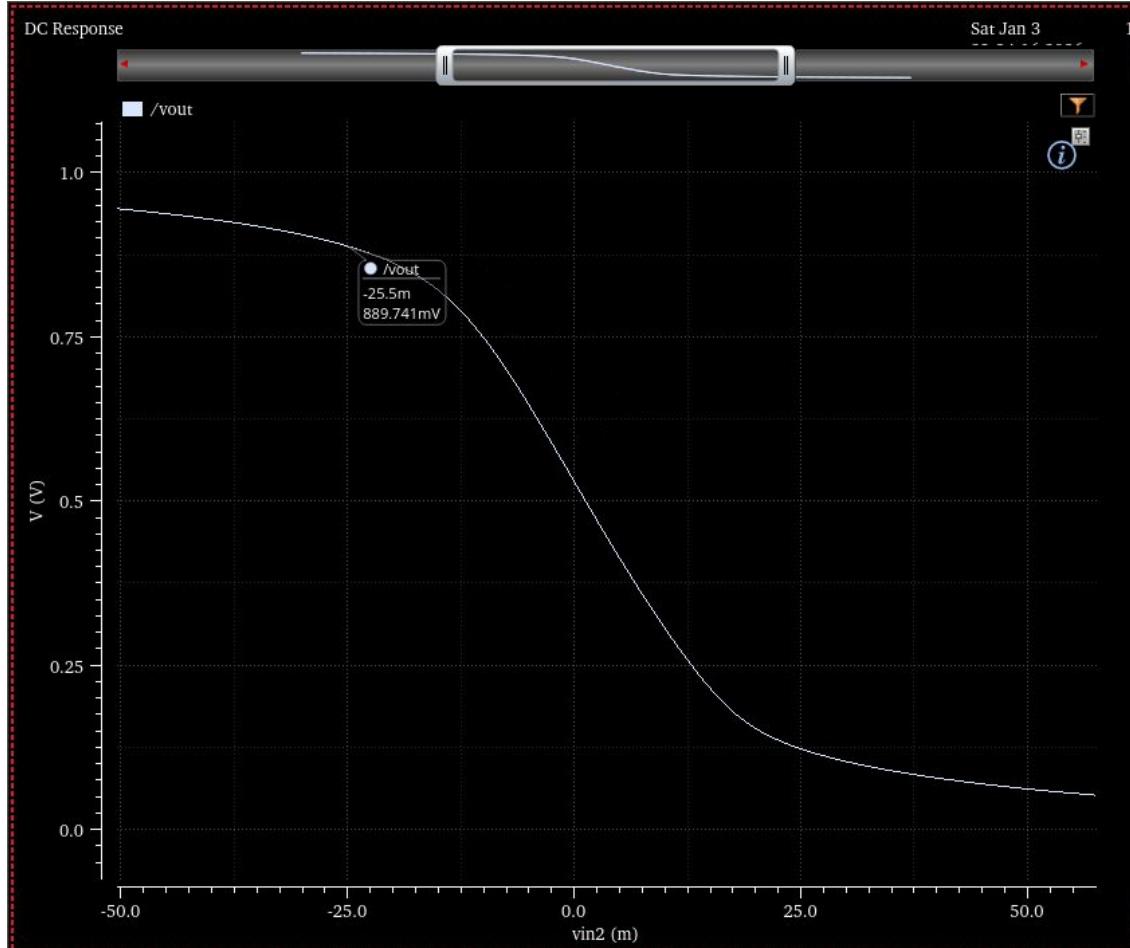


Figure 6: Stage 2 Output

Putting the two stages together, the common mode of the put is shifted above 0.5 V by about 10 mV. We sweep V_{ref} until it equals the common mode of the first stages output which was at 0.535 V. We find we can maintain a gain > 203 within a swing of 750 mV

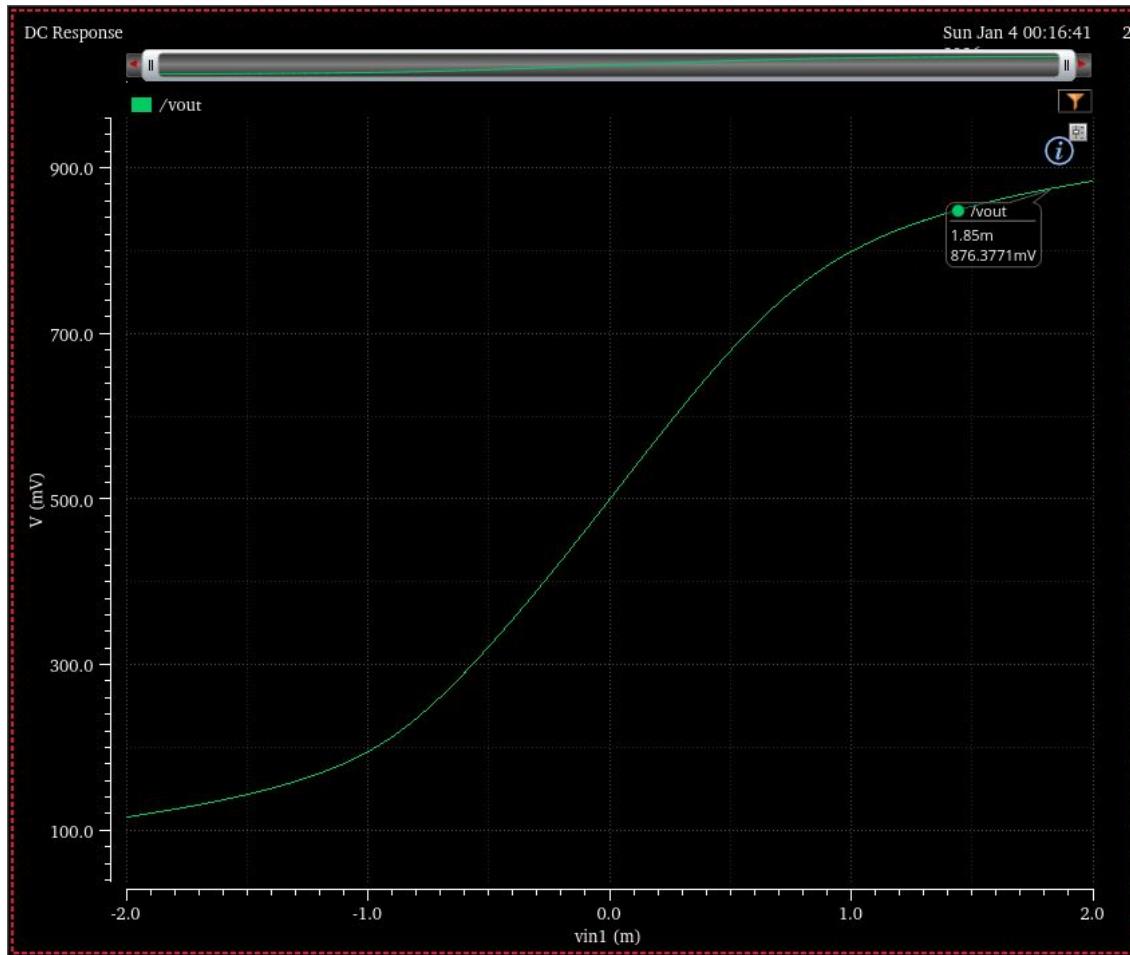
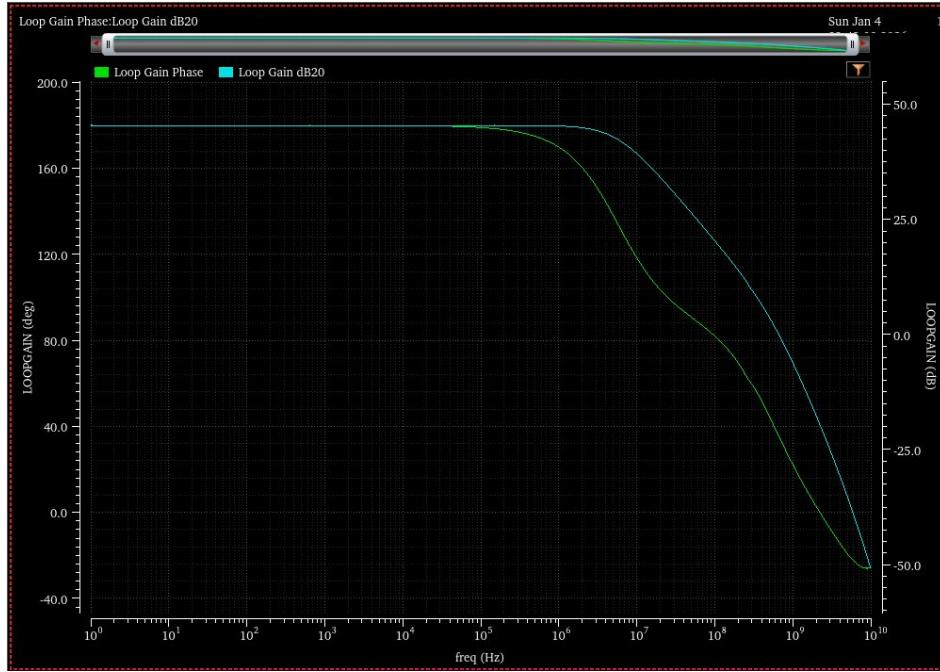


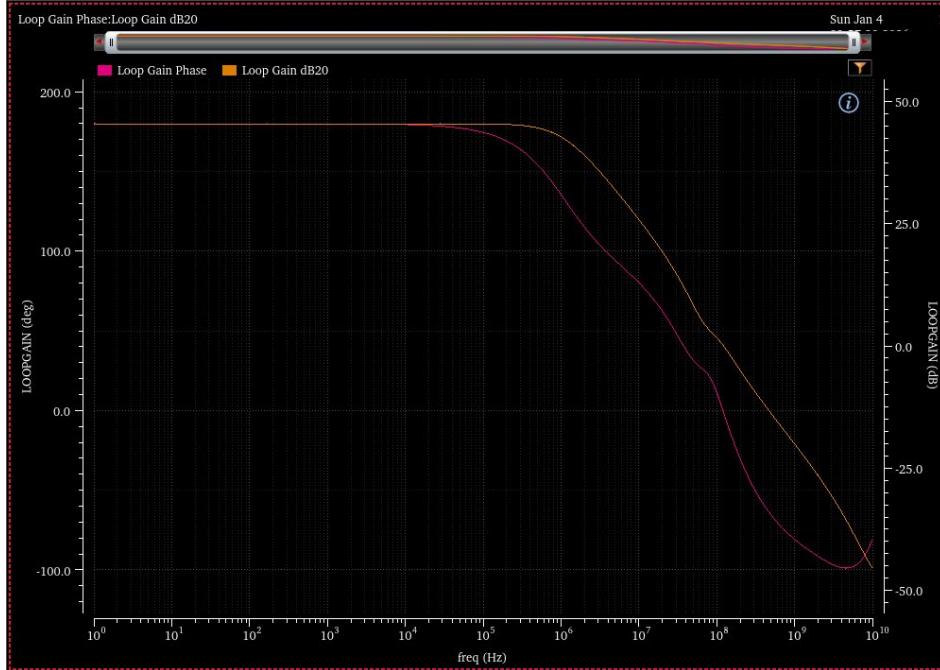
Figure 7: Full Op Amp Output

2.3 Compensation

Conducting a stability analysis of the open loop response, we see the low frequency gain is 46.15 dB and unity gain frequency is 662 MHz with phase margin of 35°. The dominant pole is at around 6 MHz.

Figure 8: $C_c = 0, R_c = 0$

The phase margin is 60° at around 300 MHz so draw a -20 dB/dec line starting at 300 MHz and 0 dB until it hits the gain plot at around 1 MHz. We adjust C_c until the pole shifts to that 1 MHz. This ended up being 1 pF.

Figure 9: $C_c = 1p, R_c = 0$

We find the point where the phase margin is 45° (250 MHz) and then set $R_c = 1/(\omega \times C_c) = 40k$. We achieve UGF = 600 MHz, but only PM = 47.5° . The phase margin being so low means our op amp is may not be stable enough.

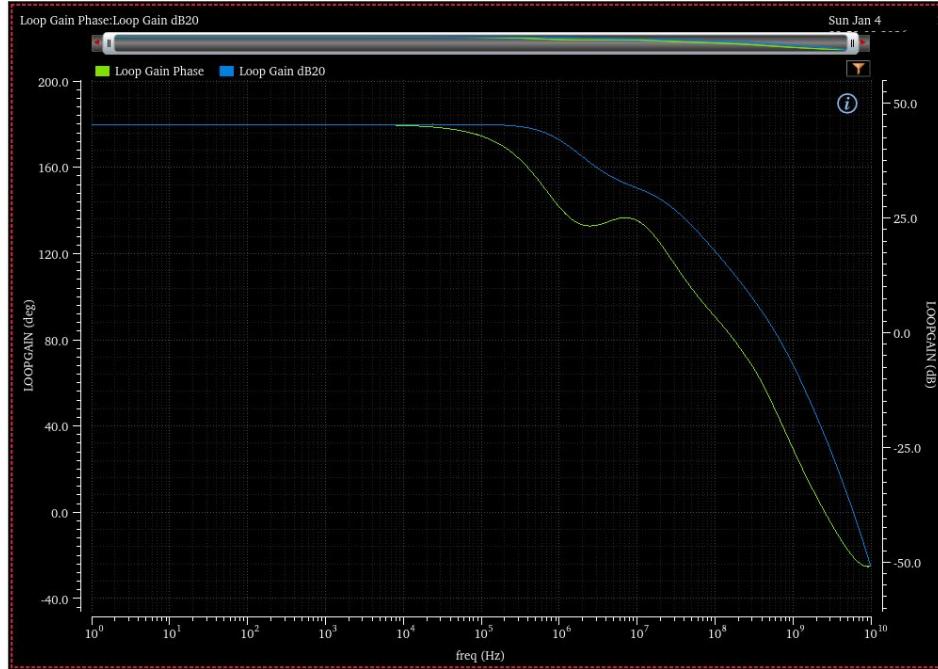


Figure 10: $C_c = 1p, R_c = 40k$

3 Results

Specification	Target	Achieved
Nominal output common-mode (DC level)	$V_{DD}/2$	0.5 V
Two-stage power consumption	≤ 0.4 mW	399.5 mW
CMFB circuit power	≤ 40 μ W	31.4 μ W
Differential output swing	≥ 0.75 V	0.78 V
Low-frequency differential gain	≥ 46 dB	46.15 dB
Small-signal unity-gain frequency	≥ 600 MHz	600 MHz
Phase margin	$60^\circ \leq PM \leq 90^\circ$	47.5°
Slew rate	≥ 20 V/ μ s	5.5 V/ μ s rising, 9.6 V/ μ s falling

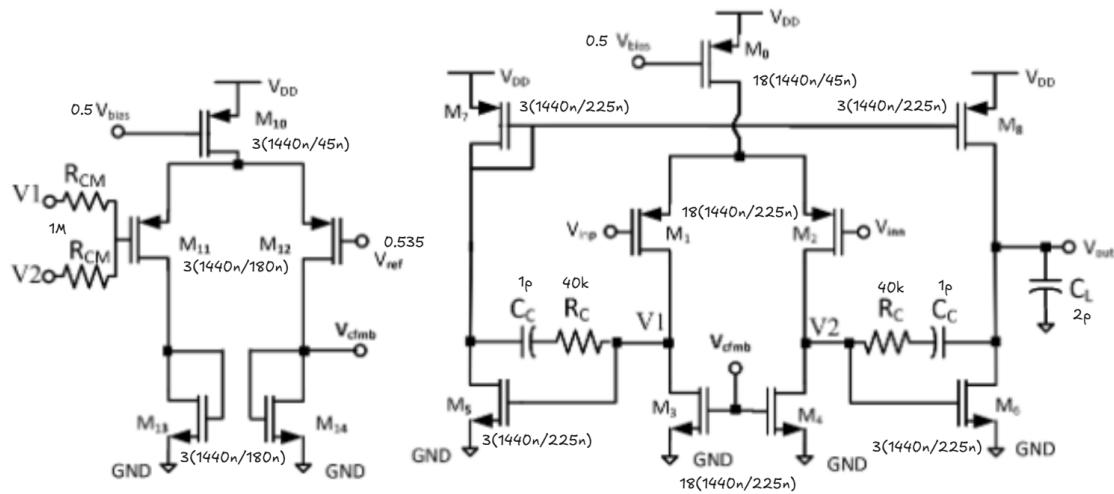


Figure 11: Device Sizings

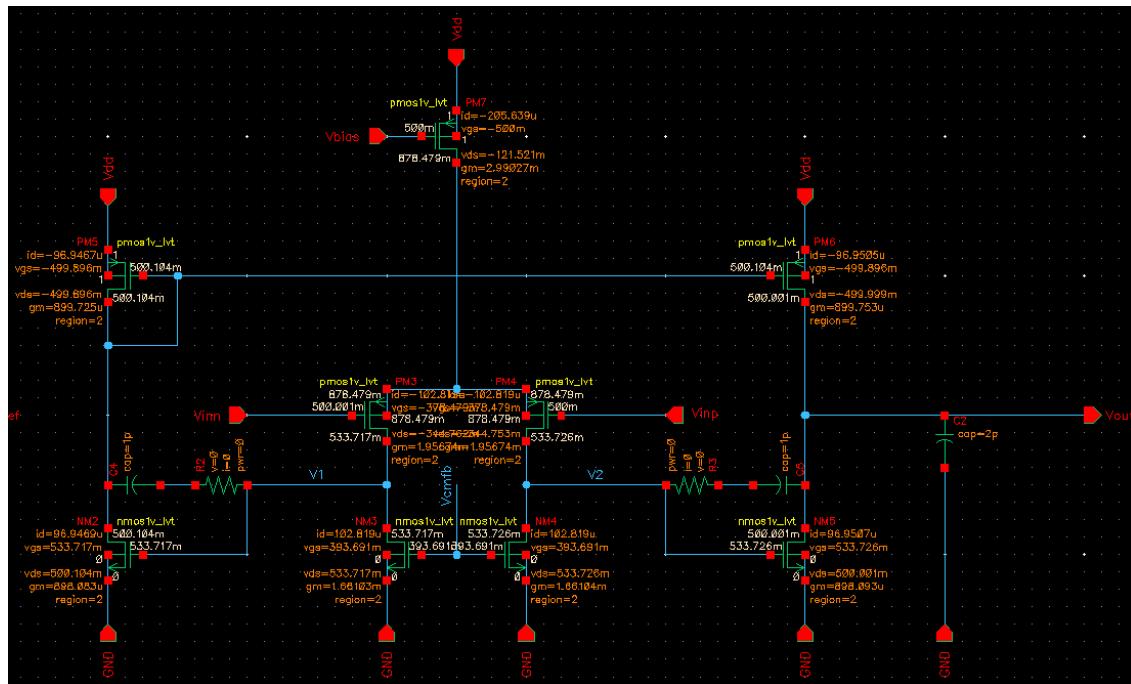


Figure 12: Op Amp DC Operating Points

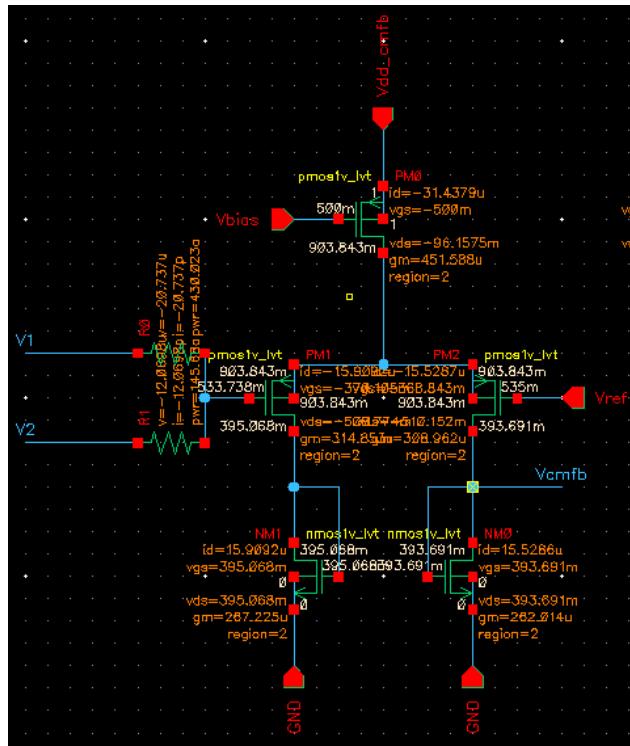


Figure 13: CMFB DC Operating Points

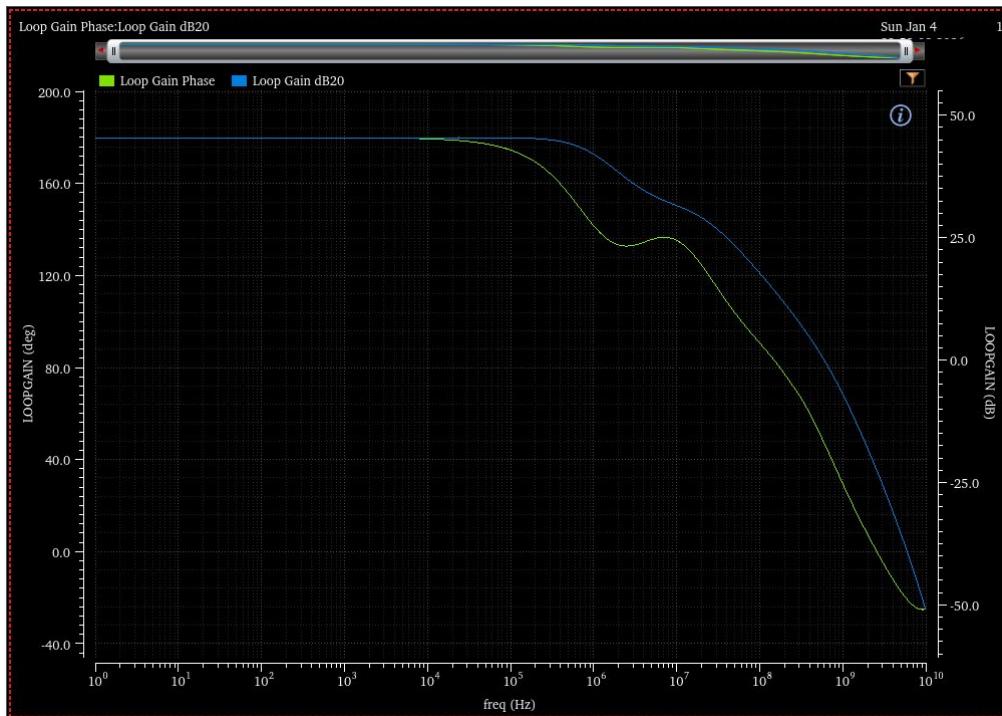


Figure 14: Open Loop Response (Low Freq Gain = 46.15 dB, UGF = 600 MHz, PM = 47.5°)

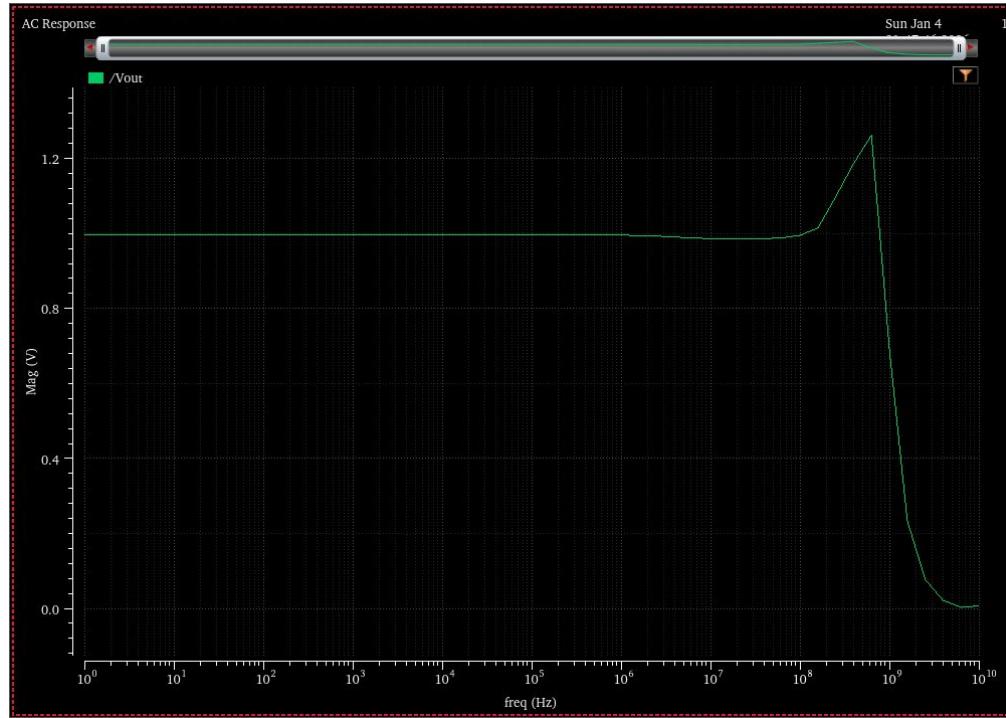


Figure 15: Closed Loop Response (3 dB point = 983 MHz)

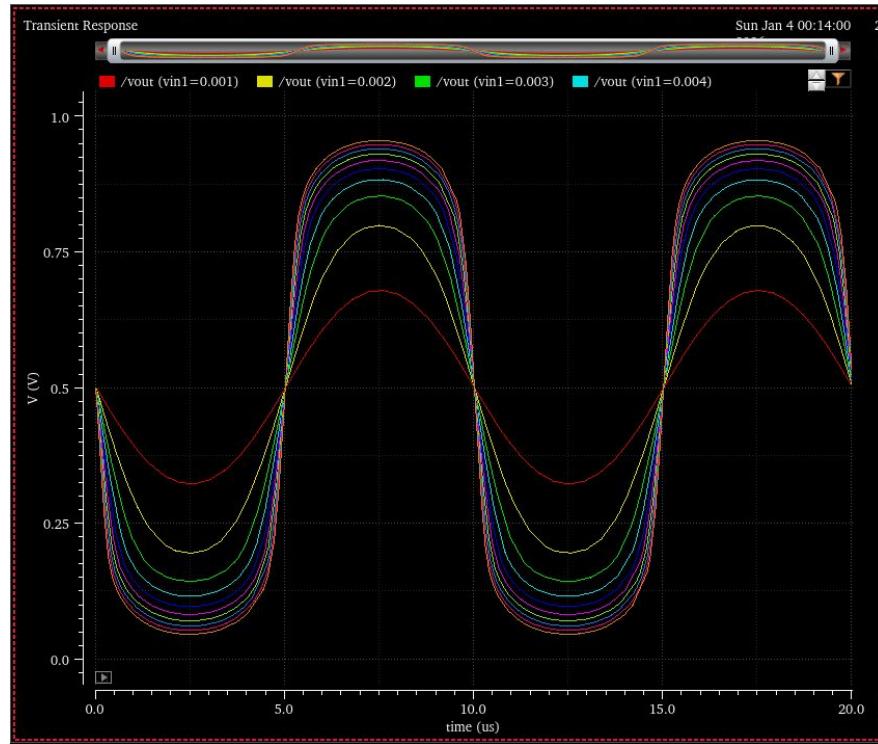


Figure 16: Output Distortion Sweep (1m:1m:10m)

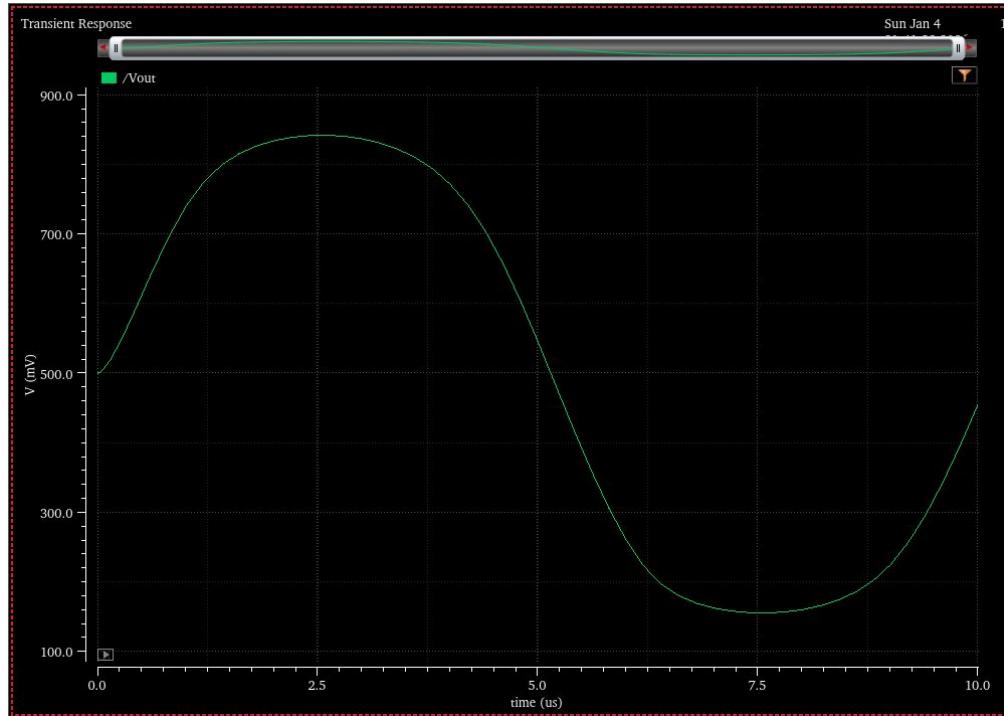


Figure 17: Maximum Undistorted Output ($V_{in} = 2.7 \text{ mV}$)

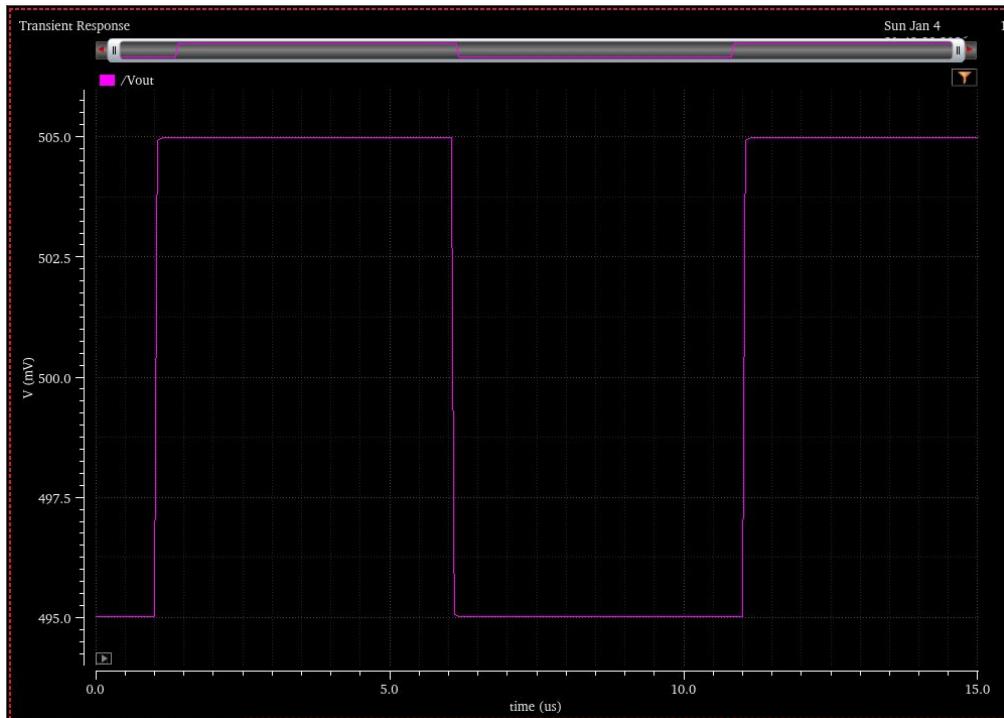


Figure 18: 10 mV Step Response (10%-90% time = $0.0803\mu\text{s}$, 90%-10% time = $0.0801 \mu\text{s}$)

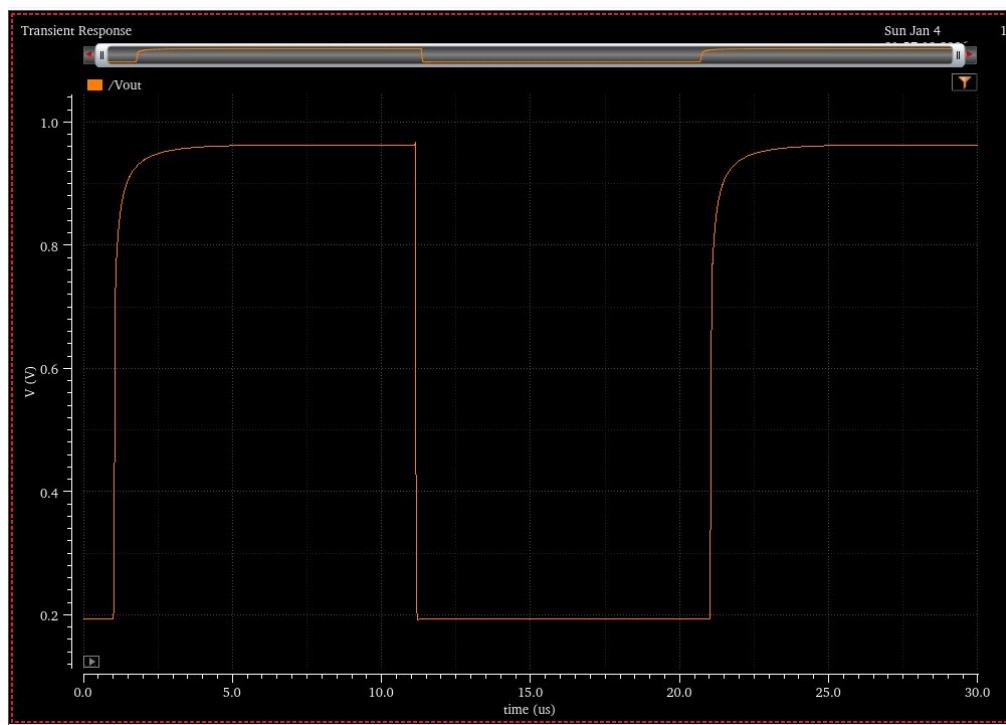


Figure 19: 1 V Step Response (Rising Slew Rate = $9.6 \text{ V}/\mu\text{s}$, Falling Slew Rate = $5.5 \text{ V}/\mu\text{s}$)