

**RapidSmith 2**

**A Library for Low-level Manipulation   
of Vivado Designs at the Cell/BEL Level**

**Technical Report and Documentation**

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# Introduction

## What is RapidSmith 2?

The original BYU RapidSmith project began in 2010 with the goal to develop a set of tools and APIs written in Java which would provide academics with an *easy-to-use* platform to try out experimental CAD ideas and algorithms on modern Xilinx FPGAs. RapidSmith 2 (abbreviated RS2 hereafter) represents a major addition to RapidSmith. Using RS2 you can write custom CAD tools which will:

* export designs from Vivado
* perform analyses on those designs
* make modifications to those designs
* import those designs back into Vivado for further processing or bitstream generation

In addition, you need not start with a Vivado design – you can create a new design from scratch in RS2 and then import it into Vivado.

So, clearly a major addition with RS2 is the ability to work with Vivado. However, the other major new capability which RS2 adds over RapidSmith is that it changes RapidSmith’s design representation from the Instances and Sites of ISE’s XDL language to the Cells and BELs of Vivado. This is a significant change as it exposes the actual design and device in a way that RapidSmith never did, opening up a world of new CAD research opportunities which were difficult to perform using Rapidsmith.

## Who Should Use RS2?

RS2 is aimed at anyone desiring to do FPGA CAD research on real Xilinx devices. It is written in Java. It also depends on some understanding of Xilinx FPGAs, Vivado, and TCL. However, the goal is that this documentation provides sufficient background and detail to help bring developers up to speed on the needed topics.

RS2 by no means is a Xilinx Vivado replacement and **cannot** be used without a valid and current license to a Xilinx tools installation (RS2 cannot generate bitstreams for a design, for example).

## Why RS2?

The Xilinx-provided TCL interface into Vivado, in theory, provides all that is needed to create any kind of CAD tool desired to augment the capabilities provided by Vivado. In practice there are a number of problems with that. First, TCL is slow, far too slow to execute a router for example. Also the Xilinx TCL interface does not manage memory well. In our experience, long running scripts eventually cause the system to run out of memory (this has been unofficially confirmed by reading between the lines of the responses we have received to bug reports we have filed). Brad White’s MS work also determined that not 100% of the device information required to do arbitrary CAD manipulations is available through TCL. As a result, additional tools (and some small amount of manual work) are required to provide the user (and CAD tools they might like to write) with all the physical details on Xilinx parts (simply put, some information is not available through the TCL interface). Finally, the ability to export and import designs to/from Vivado and operate on them outside Vivado using a modern high-level language such as Java is a hugely useful capability.

RS2 (in conjunction with Tincr which is described in a later section of this document) takes care of all of the generation of the FPGA part information that is required by CAD tools. It also takes care of exporting/importing designs from and to Vivado along with a myriad number of fairly arcane details associated with that process. In addition, RS2 creates special device files from the XDLRC files produced by Tincr and provides a nice API into those physical device details. All of this enables researchers to have more time to focus on what matters most: their research of new ideas and algorithms.

## Which Xilinx Parts does RS2 Support?

As of the writing of this document, Virtex 7 has been tested the most and is currently supported in all forms and applications. In addition, an Ultrascale device file was created and demonstrated as a part of Brad White’s MS work to show that it is possible. At some point, Ultrascale should be fully supported[[1]](#footnote-1).

As will be seen later, to generate additional device files for additional parts *within a supported family* is relatively straightforward and can be done by any user. As will also be seen later, new families can also be supported but this requires a bit more work. As time goes on the process will become simpler – that is one of the goals for RS2 moving forward.

## How is RS2 Different than VPR and VTR?

[VPR (Versatile Place and Route)](http://www.eecg.utoronto.ca/vpr/) has been an FPGA research tool for several years and has led to hundreds of publications on new FPGA CAD research. It has been a significant contribution to the FPGA research community and has grown to be a complete FPGA CAD flow for research-based FPGAs.

The main difference between RapidSmith/RS2 and VPR is that the RapidSmith tools aim to provide the ability to target commercial Xilinx FPGAs, providing the ability to exit and re-enter the standard Xilinx flow at any point. All features of commercial FPGAs which are accessible via XDL and Vivado’s TCL are available in RapidSmith and RS2.  VPR currently is limited to FPGA features which can be described using VPR's architectural description facilities.

## Why Java?

We have found Java to be an excellent rapid prototyping platform for FPGA CAD tools. The Java libraries are rich with data structures useful for such applications and Java eliminates the need to clean up objects in memory. This eliminates the time needed to debug such things, leaving more time for the researcher to focus on the real research at hand. Our experience over the past decade is that for student research projects, the lack of memory management problems (dangling pointers, memory leaks, …) and the associated errors has greatly improved our student productivity and led to far more stable CAD tools.

# Vivado, RS2, and Tincr

## RapidSmith vs. RS2

### What Was The Original RapidSmith?

The original RapidSmith was written by Christopher Lavin as a part of his PhD work at BYU. It was based on the Xilinx Design Language (XDL) which provides a human-readable file format equivalent to the Xilinx proprietary Netlist Circuit Description (NCD) of ISE. With RapidSmith, researchers were able to import XDL/NCD, manipulate, place, route and export designs among a variety of design transformations. The RapidSmith project made an excellent test bed to try out new ideas and algorithms for FPGA CAD research as code could quickly be written to take advantage of the APIs available.

RapidSmith also contained packages which could parse/export bitstreams (at the packet level) and represent the frames and configuration blocks in the provided data structures. In this regard, RapidSmith did not include any proprietary information about Xilinx FPGAs that is not publicly available.

RapidSmith continues to be functional and is still available at the SourceForge.net website. There, you will find documentation, installation instructions, the RapidSmith code base, and a collection of demo programs based on it.

### What is RS2?

With the announced end of ISE (with the Virtex7 family of parts being the last family to be supported by ISE), there was no path forward to newer parts using RapidSmith. This is because XDL is not available with Vivado. However, with Vivado Xilinx has provided an extensive TCL scripting capability which it initially looked as if it could provide a similar capability to that provided by XDL in terms of accessing both Vivado’s design and device data and in terms of creating and modifying Vivado designs. The development of RS2 consisted of two parts.

#### Tincr: Integrating Custom CAD Tool Frameworks with the Xilinx Vivado Design Suite

In the first part, the Vivado TCL capability was investigated to ensure that, indeed, it did provide the needed ability to access design and device data and export that to external tools such as RapidSmith. This resulted in the Tincr project, led by Brad White as a part of his MS work at BYU, with Thomas Townsend making additions as a part of his research.

Tincr is a TCL-based library of routines which (a) provide a variety of functions to simply make working with Vivado via TCL simpler, (b) provide a way to export all the data associated with a Vivado design into what is called a Tincr Checkpoint (TCP), (c) provide a way to reimport Tincr Checkpoints back into Vivado, and (d) access device data from Vivado and output that data in the form of XDLRC files (these are the files which XDL used to describe devices and are necessary for RapidSmith to understand the structure of and the resources available for use in a given Xilinx part). Tincr is available at Github.com as the project byuccl/Tincr. Tincr is described in two publications:

B. White and B. Nelson, "Tincr — A custom CAD tool framework for Vivado," 2014 International Conference on ReConFigurable Computing and FPGAs (ReConFig14), Cancun, 2014, pp. 1-6, DOI: 10.1109/ReConFig.2014.7032560

White, Brad S., "Tincr: Integrating Custom CAD Tool Frameworks with the Xilinx Vivado Design Suite" (2014), BYU Scholars Archive, Paper 4338. URL: http://scholarsarchive.byu.edu/etd/4338

#### RS2: A Framework for BEL-Level CAD Exploration on Xilinx FPGAs

The second part of the development of RS2 was to add a new layer of design representation to RapidSmith which more closely matches that of Vivado. This was done as a part of his PhD work by Travis Haroldsen at BYU. As of this writing, an initial paper on RS2 has appeared:

Travis Haroldsen, Brent Nelson, and Brad Hutchings, “RapidSmith 2: A Framework for BEL-Level CAD Exploration on Xilinx FPGAs”, Proceedings of the 2015 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, February 2015, Monterey CA, pp. 66-69, DOI: 10.1145/2684746.2689085.

### What is All This About XDL and XDLRC and How Does RS2 Fit Into That?

The Xilinx ISE tools had the capability to export XDL and XDLRC files which RapidSmith used:

* An XDLRC file was a complete description of a given Xilinx FPGA, describing every tile, every switchbox, every wire segment, and every PIP in the part. RapidSmith was able to process this information and use it to support the creation of CAD tools such as placers and routers.
* An XDL file was a textual representation of an NCD file (a user design). It described the user design as a collection of ***Instances*** and ***Nets.*** Instances correspond to things like SLICEs, BRAMs, DSP48s, and IOBs. Instances could be placed onto primitive sites. Additionally, **Nets** in XDL consisted of a list of pins (their logical connections) and an optional list of PIPs (their physical routing connections).

In Vivado, however, designs are described as a collection of ***Cells*** where a cell corresponds to things like LUTs, flip flops, etc. Cells are placed onto ***BEL*** objects such as an ALUT or a BFF. RS2 contains a new layer of hierarchy in its design and device descriptions where Cells and BELs are first-class objects and design manipulation is all done at the Cell/BEL level.

Also, Vivado Nets are described using *directed routing strings* rather than lists of PIPs. RS2 also contains a set of new classes to enable the representation and manipulation of Nets using these routing strings.

Thus, using RS2, design manipulation is now done at the level of Cells and BELs and importing/exporting designs to/from Vivado is now fully supported.

## RS2 Usage Model and Structure

The usage model for RS2 is shown in Figure 1. As can be seen, a design can be exported from Vivado at multiple different points in the Vivado design flow. In each case, Tincr is used to export a Tincr Checkpoint which can then be imported into RS2. At those same points in the design flow, RS2 can export a Tincr Checkpoint which can then be imported back into Vivado. Thus, a complete solution involves Vivado, Tincr, and RS2.



Figure 1 – Vivado and RS2

# Getting Started

## Installation

### Getting RS2

RS2 is available on Github at:

[https://github.com/byuccl/RapidSmith2](https://github.com/xrtc/RapidSmith2)

The repository contains all the files you need (including supporting JAR files). You can either build RS2 into .class and .jar files for use in any Java environment, or you can easily build RS2 for use in Eclipse (recommended).

### Requirements for Installation

* Windows, Linux or Mac OS X all will work (see notes below for Mac OS X)
* Vivado
* JDK 1.8 or later NOTE: If you plan on using the Qt Jambi framework in a Windows environment, you will need the 32-bit JRE (Qt Jambi 4.6.3 had yet to be compiled in 64-bit Windows as of the writing of this document).
* In addition, the distribution provides copies of a number of JAR files required for use by RS2.

### Steps for Installation For Command Line Usage

The first task is to acquire RS2.  This will require a git client.  You can acquire the RS2 distribution by executing the following:

     git clone [https://github.com/xrtc/RapidSmith2](https://github.com/srtc/RapidSmith2)

The second task is to create an environment variable called RAPIDSMITH\_PATH and point it at the RapidSmith2 directory thus created.  This is needed so RS2 can find the required device files and other items as it runs.

The third task is to build RS2.  At this point you have two choices: setting up RapidSmith2 for use with Eclipse or building RapidSmith2 manually to generate .class and .jar files which you can then use with any Java installation.

#### Building for Eclipse

RS2 requires Eclipse Neon or later so install that.

Then, create an eclipse project by executing one of the following (depending on your system):

    gradlew eclipse    # Will need to change the permissions of gradlew to allow execution

    gradlew.bat eclipse

Executing these will create a .project file.  Once you have done this you can import the project into Eclipse by opening Eclipse and selecting:

    File->Open Projects From File System

and pointing it to the RapidSmith2 directory created when you cloned RS2 from github above.

All of the Java source files will be found in Eclipse under src/main/java.

#### Building Manually

Execute one of the following to build RS2:

     gradlew build     # Will need to change the permissions of gradlew to allow execution

     gradlew.bat build

This will produce a variety of things, any of which can be added to your CLASSPATH as needed:

1. The resulting RS2 class file directory tree will be found in build/classes/main.
2. A jar file of the above RS2 class files can be found in build/libs.
3. Both tar and zip files can be found in build/distributions. They contain a full jar of the RS2 build along with copies of other needed jar files. You should add them all to your CLASSPATH except the qtjambi ones - just add the qtjambi one for your particular system (note there is no 64-bit qtjambi for windows so use the 32-bit one).

At this point you should be able to write tools that use RS2.

An obvious thing to try is to mix and match – developing in Eclipse but then running the resulting apps from the command line. Just be aware that Eclipse puts its compiled .class files in very different places than where the manual build process puts its .class files. Make sure you understand that before you try that.

### Additional Notes for Mac OS X Installation

* The instructions above require you to set the RAPIDSMITH\_PATH environment variable. If running from the command line, the environment variables can be added to your .bash\_profile file as in any other UNIX-like system. However, if using an IDE such as Eclipse, you either need to define the environment variable for every Run Configuration you create you create in Eclipse or you need to add the RAPIDSMITH\_PATH definition system-wide in OS X. This can be done, but how to do so differs based on what OS X version you are running (and seems to have changed a number of times over the years). Search the web for instructions for how to do so if you desire. Hint: you will likely have to edit some .plist files.
* Another difference for OS X is that when running programs that use Qt in Java under Mac OS X, the user will need to supply an extra JVM switch, “-XstartOnFirstThread”.

### Testing Your Installation

At this point you can test your installation by executing the java DeviceBrowser program (edu.byu.ece.rapidSmith.device.browser.DeviceBrowser). This can be done either from within Eclipse or from the command line, depending on how you are running RS2 (if running under OS X be sure to provide the –XstartOnFirstThread JVM argument.

If all goes well you should see a graphical representation showing the details of a physical FPGA device as shown in Figure 2.

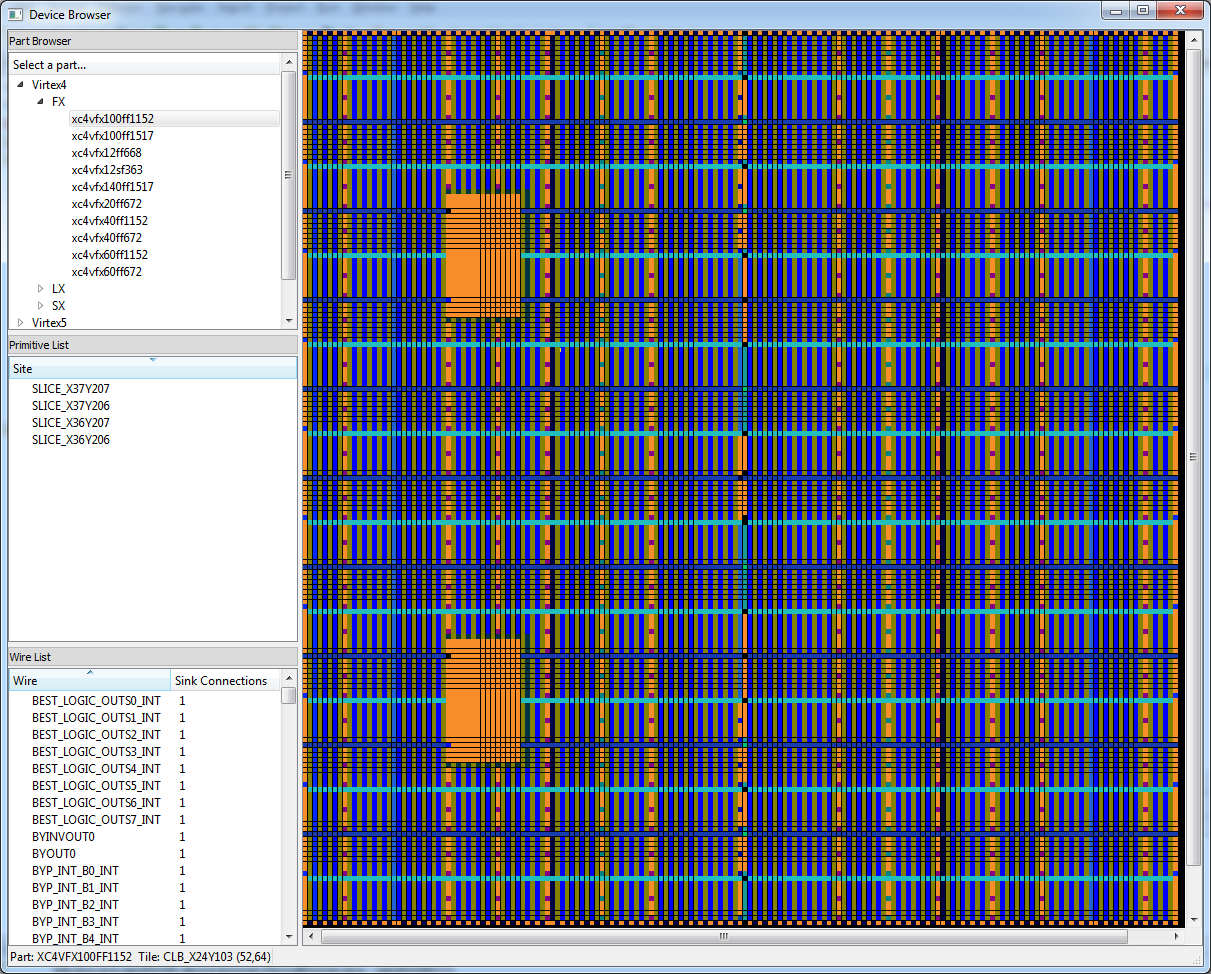


Figure 2 – Device Browser Sample Display

### Device Files For Use With RS2

Device files for one part (the xc7a100tcsg324) are included in the distribution so you can immediately start working with RS2 using this part (initially, it will be the only device available when you run the DeviceBrowser above). If you desire to work with additional parts, follow the instructions found in this documentation in **Section 7 Generating Device Files in RS2** on page 20.

# Example RS2 Programs

A variety of example programs can be found in the examples2 directory in the RS2 installation (edu.byu.ece.rapidSmith.examples2). They have been heavily commented and so provide a means to learn the RS2 API by example as we believe this is much better than reading a lot of text trying to teach you what you need to know.

There is a README.txt file in that directory to provide an overview and suggested order for learning from the examples.

In addition, the subsections below describe one or more built-in RS2 programs which you might find useful.

## Device Browser

Note: this is a program from RapidSmith, but which is discussed here because it is still very useful in RS2.

This GUI program is located in the edu.byu.ece.rapidSmith.device.browser package. It will let you browse parts at the tile level.  On the left, the user may choose the desired part by navigating the tree menu and double-clicking on the desired part name.  This will load the part in the viewer pane on the right (the first available part is loaded at startup).  The status bar in the bottom left displays which part is currently loaded.  Also displayed is the name of the current tile which the mouse is over, highlighted by a yellow outline in the viewer pane. The user may navigate inside the viewer pane by using the mouse.  By right-clicking and dragging the cursor, the user may pan.  By using the scroll-wheel on the mouse, the user may zoom.  If a scroll-wheel is unavailable, the user may zoom by clicking inside the viewer pane and pressing the minus(-) key to zoom out or the equals(=) key to zoom in.

All that is required for this to operate is a valid device file (no design required).

See below for a screenshot.

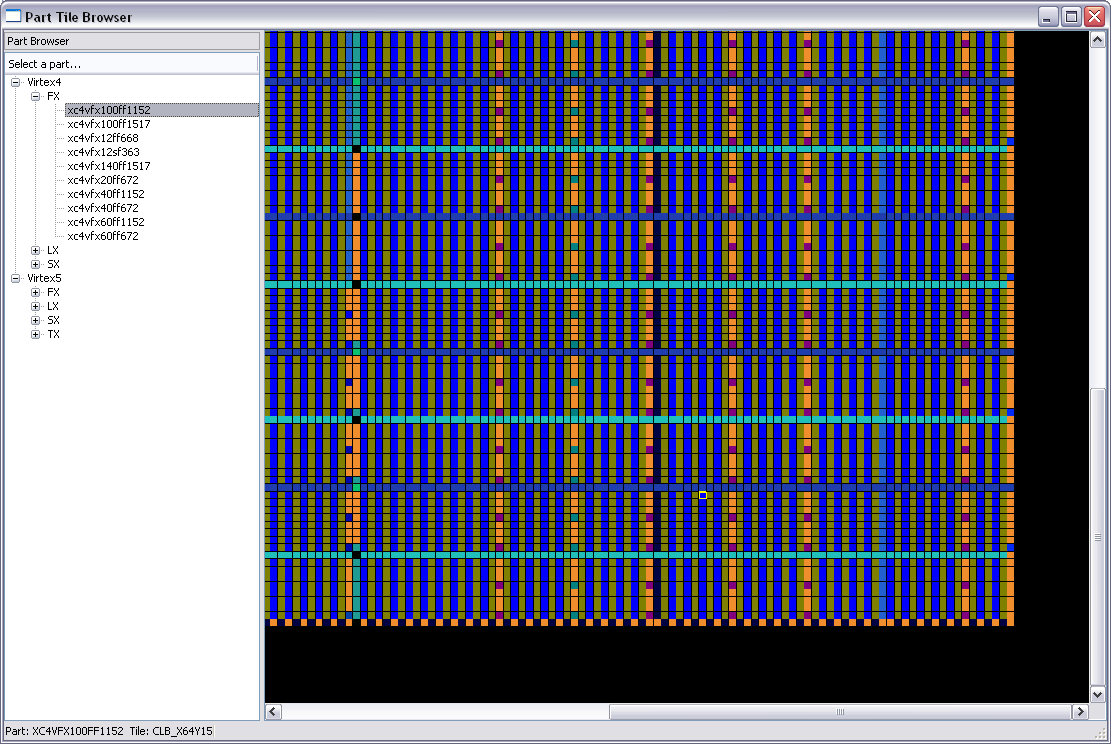


Figure 3 – Screen Shot of DeviceBrowser

The device browser also allows the user to follow the various connections found in the FPGA. By double clicking a wire in the wire list, the application will draw the connection on the tile array (as shown in the screenshot below). By hovering the mouse pointer over the connection, the wire becomes red and a tooltip will appear describing the connection made by declaring the source tile and wire followed by an arrow (->) and the destination tile and wire. By clicking on the wire, the application will redraw all the connections that can be made from the currently selected wire. By repeating this action, the user can follow connections and discover how the FPGA interconnect is laid out. This is shown below. Thanks to Chris Lavin for originally creating this app.

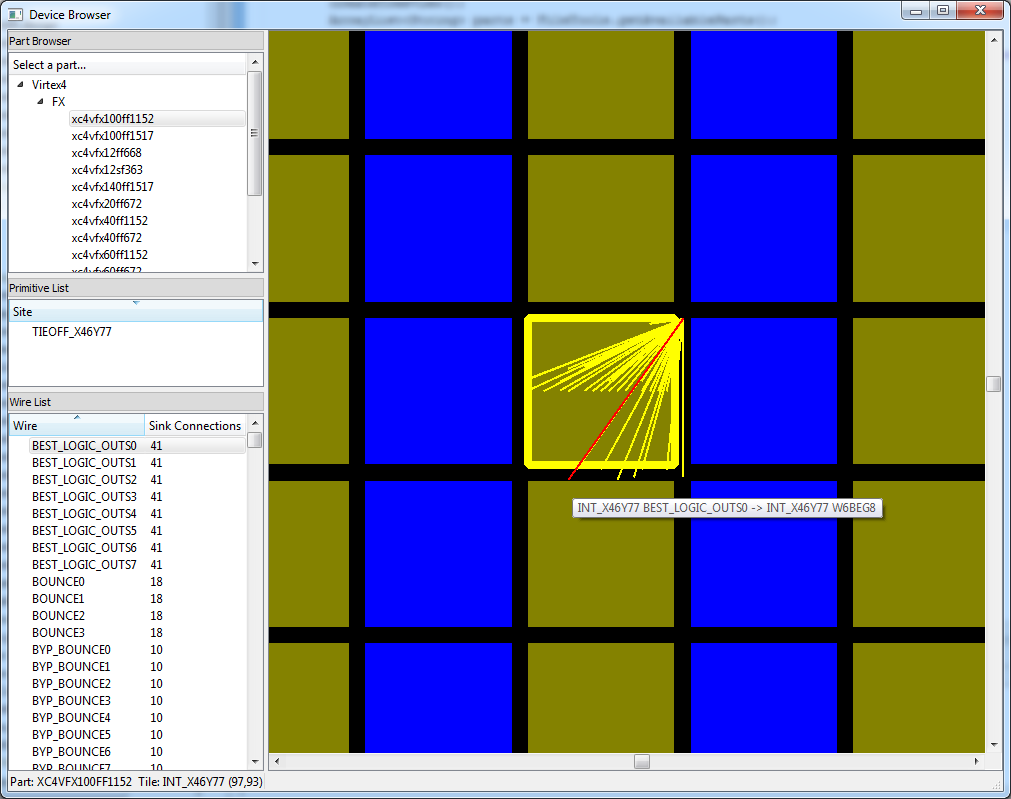


Figure 4 – DeviceBrowser Screen Shot Showing Wire Connections

# Designs in RS2

## Designs in RS2

Designs in RS2 are similar to the designs found in Vivado (and which are exported as EDIF files from Vivado).

They are essentially logical netlists. They are represented and stored in the data structures found in the **design.subsite** package. A *CellDesign* consists of a collection of *Cell* objects, interconnected by *CellNet*s. *CellNet*s connect to the *CellPin*s on *Cell*s. CellNets typically have one source pin and one or more sink pins. *Cell* objects have a name, properties, pins, a link to the library cell they are an instantiation of, etc.

*Cell*s may be placed onto *Bel*s and the corresponding *CellPin*s mapped onto *BelPin*s. *CellNet*s, when physically routed, map onto one or more *RouteTree*s.

## The Cell Class

The example programs mentioned above provide examples of manipulating Cell objects. Here are a few things you should know about cells, in no particular order:

* A Cell always contains a reference to an object of type LibraryCell, which serves as a template for its construction.
* Cells are placed onto BELs in the device. This is done by setting the Cell’s *anchor* value to point to the BEL it resides on. Determining whether a BEL location is legal for the placement of a given Cell can be done by … Generating a complete list of the possible BEL locations a Cell can be placed is done by …
* Cells as represented in EDIF files coming from Vivado may contain properties. For example, a D flip flop cell (FDRE) has a CONFIG.INIT property, indicating what its power-up state should be. These properties can be set to modify the Cell’s behavior. The examples2 directory contains a DesignAnalyzer test program which pretty-prints an RS2 logical design. As a part of its operation, it lists the properties set on each Cell in the design.
* It might be of interest, however, to learn what properties *could* be set for a given cell. This set of properties is attached to the LibraryCell objects loaded when a cell library is read in from an XML file (see the $RAPIDSMITH\_PATH/devices directory to find these XML files for any devices installed – the files are quite readable and from them you can learn much about the available LibraryCell types for a given FPGA family). Additionally , the examples2 directory contains a test program illustrating how to enumerate the possible properties which may be set for a Cell (based on its corresponding LibraryCell) as well as listing the possible values that are legal to set it to.
* In a GUI view of devices in Vivado you will see polarity inverter in many sites allowing for programmable selection of a signal or its inverse. This is shown in the GUI in the form of a 2:1 MUX. The CLK signal and its inverse entering a SLICE is an example of this. However, this is not explicitly represented in the device representation. Rather, properties on the Cells driven by the mux output signals muxes indicate whether the signal is inverted or not. For example, generate a 4-bit counter using rising-edge triggered flip flops in Vivado and generate an EDIF file for it. You will see that the counter is constructed, in part from FDRE cells. Now, modify the HDL for your counter to make it a falling-edge triggered counter and compare the resulting EDIF file. The difference you will see is that the property on each of the FDRE cells called CONFIG.IS\_C\_INVERTED has been set, indicating it is a falling-edge triggered flip flop. When bitgen is actually done by Vivado, the corresponding clock inverter will be programmed accordingly.
* It should go without saying that since there is only one such clock inverter in a SLICE, all the flip flops in a slice must be either rising-edge triggered or falling-edge triggered (they must have the same CONFIG.IS\_C\_INVERTED *control set* value). If you violate this, Vivado will throw an error. Similar restrictions exist for all cells in a site driven by shared programmable inverters. For example, flip flops in a slice (FDRE LibraryCells) share programmable inverter on their clock, D, and R inputs.
* Cell objects have pins on their periphery where CellNets connect to.
* The top-level ports of a design are tied to IPORT, OPORT, or IOPORT Cell objects. These are pseudo-cells (you won’t find them in Vivado) and represent the terminal points for signals leaving or entering the top-level.

## The CellNet Class

Here are a few things you should know about CellNet objects, in no particular order:

* A CellNet typically has one source pin and one or more sink pins. The CellNet class has methods for traversing these.
* A CellNet has a type. Legal values are WIRE, GND, VCC, and UNKNOWN. The WIRE type is the one used for normal signals.
* GND and VCC nets require special handling. They violate the one source pin assumption above. When physically routed, they are chopped up by Vivado into a collection of GND and VCC nets rather than being a single net each with one source.
* There ought to be tons to say about CellNet manipulation – what should it include?

### Physical Routing in RS2

A CellNet is physically routed by determining the metal segments and intervening PIPs that are to be used to make up the route. A physical net is called a Wire and contains some number of RouteTree objects. A given RouteTree object has the source of the route and the root and branches to represent the branching of the route between source and sink. Normal wires have only one source but, as mentioned above, GND and VCC nets may have multiple, resulting in more than one RouteTree being used to represent the physical wire.

Once a CellNet’s physical routing has been created as a RouteTree, that is converted to a *directed routing string* when RS2 designs are exported from RS2 back into Vivado.

A RouteTree object is essentially a linked list with the possibility of 2-way branching at each node. The examples2 directory program called DesignAnalyzer illustrates how to traverse a RouteTree structure as it prints the physical route for the wires associated with each CellNet in the design.

# Devices in RS2

## Devices in RS2

A device is defined in RS2 as a unique Xilinx FPGA part that includes package information but not speed grade (such as the xc7a100tcsg324 device included in the RS2 distribution). Each device contains specific information concerning its primitive sites, tiles, wires, IOBs, and PIPs that are available to realize designs. The device information is represented in RS2 in the **device** package. RS2 has significantly extended the original RapidSmith D**evice** class for its use as well as how device files are generated.

A *Device* object consists of a collection of *Tile*s, each of which contains one or more *Site*s. A *Site* contains one or more *Bel*s. *Site*s have *SitePin*s around their periphery and *Bel* objects have *BelPIN*s around theirs.

The physical wires in the device are represented by objects of type *Wire*, *TileWire*, and *SiteWire*. However, the goal of RS2 is to largely hide the differences between these three wire object types and let the user simply deal with *Wire* objects.

The previously-mentioned Device Browser program illustrates how to load and browse a device down to the Tile level.

What is the list of topics we want to tell users about the Device representation?

## Generating Device Files in RS2

RS2 is distributed with a single device file included (for an Artix7 device). The device files for this can be found in the ${RAPIDSMITH\_PATH}/devices/artix7directory and consist of a \*\_db.dat file and a \*\_info.dat file.

Additional device files for a family can be generated by a user. If these are additional device files for an already-supported device family, the process is relatively straightforward. The document: ${RAPIDSMITH\_PATH}/devices/doc/InstallingNewDevices.txt provides instructions on how to generate new device files for supported families. These should be adequate to generate new device files for families with existing support.

If you need device file support for a new family, the process is more difficult. Contact the authors for possible help in doing so.

# Routing in RS2

As understanding the routing graph in RS2’s device representation is crucial to being able to manipulate routing, this chapter provides a more detailed discussion to help users and developers. RS2’s routing handling is significantly different from that found in RapidSmith.

**Needs a total rewrite, some can be lifted from the original RapidSmith documentation.**

# Bitstreams in RS2

In the original RapidSmith, bitstreams can be parsed, manipulated, and exported for Virtex 4, Virtex 5 and Virtex 6 Xilinx FPGA families. Because of the proprietary nature of Xilinx bitstreams, RapidSmith provided only documented functionality when working with bitstreams (and was limited mainly to manipulation at the frame level including helping to assemble sequences of configuration commands which are interpreted by the FPGA configuration controller circuitry). While this has proven valuable to many researchers, it does not provide the ability to create your own bitstream from scratch because it does not provide the specific meaning of each bit in a bitstream. If you desire to use RapidSmith’s bitstream manipulation features, you should download and work with RapidSmith instead of RS2. If you do so, note that it has not been tested beyond Virtex 6. The authors would be interested in upgrading RapidSmith’s bitstream functionality to device families beyond Virtex 6 if users create it and are willing to contribute it to us for inclusion.

# Legal and Dependencies

RS2 is a derivative of RapidSmith and is thus covered by the same license:

## RapidSmith Legal Text

BYU RapidSmith Tools

Copyright (c) 2010-2016 Brigham Young University

BYU RapidSmith Tools is free software: you may redistribute it

and/or modify it under the terms of the GNU General Public License

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the License, or (at your option) any later version.

BYU RapidSmith Tools is distributed in the hope that it will be

useful, but WITHOUT ANY WARRANTY; without even the implied warranty

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RapidSmith Tools. It can be found at doc/gpl2.txt. You may also get

a copy of the license at <http://www.gnu.org/licenses/>.

## Included Dependency Projects

RS2 includes the Caucho Technology Hessian implementation which is distributed under the Apache License. A copy of this license is included in the doc directory in the file APACHE2-LICENSE.txt. This license is also available for download at:

<http://www.apache.org/licenses/LICENSE-2.0>

The source for the Caucho Technology Hessian implementation is available at:

<http://hessian.caucho.com>

RS2 also includes the Qt Jambi project jars for Windows, Linux and Mac OS X. Qt Jambi is distributed under the LGPL GPL3 license and copies of this license and exception are also available in the /doc directory in files LICENSE.GPL3.TXT and LICENSE.LGPL.TXT respectively. These licenses can also be downloaded at:

<http://www.gnu.org/licenses/licenses.html>

Source for the Qt Jambi project is available at:

<http://qt.nokia.com/downloads>

and more recent versions are available at:

[http:/qt.gitorious.org/qt-jambi](http://qt.gitorious.org/qt-jambi)

RS2 also includes the JOpt Simple option parser which is released under

the open source MIT License which can be found in this directory in the file

MIT\_LICENSE.TXT. A copy of this license can also be found at:

<http://www.opensource.org/licenses/mit-license.php>

A copy of the source for JOpt Simple can also be downloaded at:

<http://jopt-simple.sourceforge.net/download.html>

RS2 also includes the JDOM jars. JDOM is available under an Apache-style open source license, with the acknowledgment clause removed. This license is among the least restrictive license available, enabling developers to use JDOM in creating new products without requiring them to release their own products as open source. This is the license model used by the Apache Project, which created the Apache server. The license is available at the top of every source file and in LICENSE.txt in the root of the JDOM distribution.

The user is responsible for providing copies of these licenses and making available the source code of these projects when redistributing these jars.

# Appendix

Here we may put a grouping of useful topics that do not fit in with the rest of this document.

1. An XDL-based import/export capability has also been created and used with Virtex 6 devices as a part of Travis Haroldsen’s PhD work but that path is not being released, documented, or supported. [↑](#footnote-ref-1)