

**RapidSmith 2**

**A Library for Low-level Manipulation   
of Vivado Designs at the Cell/BEL Level**

**Technical Report and Documentation**

Travis Haroldsen, Thomas Townsend, Brent Nelson  
  
NSF Center for High Performance Reconfigurable Computing (CHREC)  
Department of Electrical and Computer Engineering  
Brigham Young University  
Provo, UT 84602

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# Introduction

## What is RapidSmith 2?

The original BYU RapidSmith project began in 2010 with the goal to develop a set of tools and APIs written in Java which would provide academics with an *easy-to-use* platform to try out experimental CAD ideas and algorithms on modern Xilinx FPGAs. RapidSmith 2 (abbreviated RS2 hereafter) represents a major addition to RapidSmith. Using RS2 you can write custom CAD tools which will:

* export designs from Vivado
* perform analyses on those designs
* make modifications to those designs
* import those designs back into Vivado for further processing or bitstream generation

In addition, you need not start with a Vivado design – you can create a new design from scratch in RS2 and then import it into Vivado.

So, clearly a major addition with RS2 is the ability to work with Vivado. However, the other major new capability which RS2 adds over RapidSmith is that it changes RapidSmith’s design representation from the Instances and Sites of ISE’s XDL language to the Cells and BELs of Vivado. This is a significant change as it exposes the actual design and device in a way that RapidSmith never did, opening up a world of new CAD research opportunities which were difficult to perform using Rapidsmith.

## Who Should Use RS2?

RS2 is aimed at anyone desiring to do FPGA CAD research on real Xilinx devices. It is written in Java. It also depends on some understanding of Xilinx FPGAs, Vivado, and TCL. However, the goal is that this documentation provides sufficient background and detail to help bring developers up to speed on the needed topics.

RS2 by no means is a Xilinx Vivado replacement and **cannot** be used without a valid and current license to a Xilinx tools installation (RS2 cannot generate bitstreams for a design, for example).

## Why RS2?

The Xilinx-provided TCL interface into Vivado, in theory, provides all that is needed to create any kind of CAD tool desired to augment the capabilities provided by Vivado. In practice there are a number of problems with that. First, TCL is slow, far too slow to execute a router for example. Also the Xilinx TCL interface does not manage memory well. In our experience, long running scripts eventually cause the system to run out of memory (this has been unofficially confirmed by reading between the lines of the responses we have received to bug reports we have filed). Brad White’s MS work also determined that not 100% of the device information required to do arbitrary CAD manipulations is available through TCL. As a result, additional tools (and some small amount of manual work) are required to provide the user (and CAD tools they might like to write) with all the physical details on Xilinx parts (simply put, some information is not available through the TCL interface). Finally, the ability to export and import designs to/from Vivado and operate on them outside Vivado using a modern high-level language such as Java is a hugely useful capability.

RS2 (in conjunction with Tincr which is described in a later section of this document) takes care of all of the generation of the FPGA part information that is required by CAD tools. It also takes care of exporting/importing designs from and to Vivado along with a myriad number of fairly arcane details associated with that process. In addition, RS2 creates special device files from the XDLRC files produced by Tincr and provides a nice API into those physical device details. All of this enables researchers to have more time to focus on what matters most: their research of new ideas and algorithms.

## Which Xilinx Parts does RS2 Support?

As of the writing of this document, Virtex 7 has been tested the most and is currently supported in all forms and applications. In addition, an Ultrascale device file was created and demonstrated as a part of Brad White’s MS work to show that it is possible. At some point, Ultrascale should be fully supported[[1]](#footnote-1).

As will be seen later, to generate additional device files for additional parts *within a supported family* is relatively straightforward and can be done by any user. As will also be seen later, new families can also be supported but this requires a bit more work. As time goes on the process will become simpler – that is one of the goals for RS2 moving forward.

## How is RS2 Different than VPR and VTR?

[VPR (Versatile Place and Route)](http://www.eecg.utoronto.ca/vpr/) has been an FPGA research tool for several years and has led to hundreds of publications on new FPGA CAD research. It has been a significant contribution to the FPGA research community and has grown to be a complete FPGA CAD flow for research-based FPGAs.

The main difference between RapidSmith/RS2 and VPR is that the RapidSmith tools aim to provide the ability to target commercial Xilinx FPGAs, providing the ability to exit and re-enter the standard Xilinx flow at any point. All features of commercial FPGAs which are accessible via XDL and Vivado’s TCL are available in RapidSmith and RS2.  VPR currently is limited to FPGA features which can be described using VPR's architectural description facilities.

## Why Java?

We have found Java to be an excellent rapid prototyping platform for FPGA CAD tools. The Java libraries are rich with data structures useful for such applications and Java eliminates the need to clean up objects in memory. This eliminates the time needed to debug such things, leaving more time for the researcher to focus on the real research at hand. Our experience over the past decade is that for student research projects, the lack of memory management problems (dangling pointers, memory leaks, …) and the associated errors has greatly improved our student productivity and led to far more stable CAD tools.

# Vivado, RS2, and Tincr

## RapidSmith vs. RS2

### What Was The Original RapidSmith?

The original RapidSmith was written by Christopher Lavin as a part of his PhD work at BYU. It was based on the Xilinx Design Language (XDL) which provides a human-readable file format equivalent to the Xilinx proprietary Netlist Circuit Description (NCD) of ISE. With RapidSmith, researchers were able to import XDL/NCD, manipulate, place, route and export designs among a variety of design transformations. The RapidSmith project made an excellent test bed to try out new ideas and algorithms for FPGA CAD research as code could quickly be written to take advantage of the APIs available.

RapidSmith also contained packages which could parse/export bitstreams (at the packet level) and represent the frames and configuration blocks in the provided data structures. In this regard, RapidSmith did not include any proprietary information about Xilinx FPGAs that is not publicly available.

RapidSmith continues to be functional and is still available at the SourceForge.net website. There, you will find documentation, installation instructions, the RapidSmith code base, and a collection of demo programs based on it.

### What is RS2?

With the announced end of ISE (with the Virtex7 family of parts being the last family to be supported by ISE), there was no path forward to newer parts using RapidSmith. This is because XDL is not available with Vivado. However, with Vivado Xilinx has provided an extensive TCL scripting capability which it initially looked as if it could provide a similar capability to that provided by XDL in terms of accessing both Vivado’s design and device data and in terms of creating and modifying Vivado designs. The development of RS2 consisted of three parts.

#### Tincr: Integrating Custom CAD Tool Frameworks with the Xilinx Vivado Design Suite

In the first part, the Vivado TCL capability was investigated to ensure that, indeed, it did provide the needed ability to access design and device data and export that to external tools such as RapidSmith. This resulted in the Tincr project, led by Brad White as a part of his MS work at BYU, with Thomas Townsend making additions as a part of his research.

Tincr is a TCL-based library of routines which (a) provide a variety of functions to simply make working with Vivado via TCL simpler, (b) provide a way to export all the data associated with a Vivado design into what is called a Tincr Checkpoint (TCP), (c) provide a way to reimport Tincr Checkpoints back into Vivado, and (d) access device data from Vivado and output that data in the form of XDLRC files (these are the files which XDL used to describe devices and are necessary for RapidSmith to understand the structure of and the resources available for use in a given Xilinx part). Tincr is available at Github.com as the project byuccl/Tincr. Tincr is described in two publications:

B. White and B. Nelson, "Tincr — A custom CAD tool framework for Vivado," 2014 International Conference on ReConFigurable Computing and FPGAs (ReConFig14), Cancun, 2014, pp. 1-6, DOI: 10.1109/ReConFig.2014.7032560

White, Brad S., "Tincr: Integrating Custom CAD Tool Frameworks with the Xilinx Vivado Design Suite" (2014), BYU Scholars Archive, Paper 4338. URL: http://scholarsarchive.byu.edu/etd/4338

#### RS2: A Framework for BEL-Level CAD Exploration on Xilinx FPGAs

The second part of the development of RS2 was to add a new layer of design representation to RapidSmith which more closely matches that of Vivado. This was done as a part of his PhD work by Travis Haroldsen at BYU. As of this writing, an initial paper on RS2 has appeared:

Travis Haroldsen, Brent Nelson, and Brad Hutchings, “RapidSmith 2: A Framework for BEL-Level CAD Exploration on Xilinx FPGAs”, Proceedings of the 2015 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, February 2015, Monterey CA, pp. 66-69, DOI: 10.1145/2684746.2689085.

#### Vivado and RS2 Integration

The third part of the development of RS2 was to create the ability to export designs from Vivado and into RS2 and, correspondingly, to import RS2 data back into Vivado. This was completed during 2016, largely by Thomas Townsend who was an MS student at Brigham Young University during that time. The initial public release of RS2 was made in late 2016 once that piece was in place.

### What is All This About XDL and XDLRC and How Does RS2 Fit Into That?

The Xilinx ISE tools had the capability to export XDL and XDLRC files which RapidSmith used:

* An XDLRC file was a complete description of a given Xilinx FPGA, describing every tile, every switchbox, every wire segment, and every PIP in the part. RapidSmith was able to process this information and create a device representation for use in support of CAD tools such as placers and routers.
* An XDL file was a textual representation of an NCD file (a user design). It described the user design as a collection of ***Instances*** and ***Nets.*** Instances correspond to things like SLICEs, BRAMs, DSP48s, and IOBs. Instances could be placed onto primitive sites. Additionally, **Nets** in XDL consisted of a list of pins (their logical connections) and an optional list of PIPs (their physical routing connections).

In Vivado, however, designs are described as a collection of ***Cells*** where a cell corresponds to things like LUTs, flip flops, etc. Cells are placed onto ***BEL*** objects such as an ALUT or a BFF. RS2 contains a new layer of hierarchy in its design and device descriptions where Cells and BELs are first-class objects and design manipulation is all done at the Cell/BEL level.

Also, Vivado Nets are described using *directed routing strings* rather than lists of PIPs. RS2 also contains a set of new classes to enable the representation and manipulation of Nets in a format compatible with these routing strings.

Thus, using RS2, design manipulation is now done at the level of Cells and BELs and importing/exporting designs to/from Vivado is now fully supported.

## RS2 Usage Model and Structure

The usage model for RS2 is shown in Figure 1. As can be seen, a design can be exported from Vivado at multiple different points in the Vivado design flow. In each case, Tincr is used to export a Tincr Checkpoint which can then be imported into RS2. At those same points in the design flow, RS2 can export a Tincr Checkpoint which can then be imported back into Vivado. Thus, a complete solution involves Vivado, Tincr, and RS2.



Figure – Vivado and RS2

# Getting Started

## Installation

### Getting RS2

RS2 is available on Github at:

[https://github.com/byuccl/RapidSmith2](https://github.com/xrtc/RapidSmith2)

The repository contains all the files you need (including supporting JAR files). You can either build RS2 into .class and .jar files for use in any Java environment, or you can easily build RS2 for use in Eclipse (recommended).

### Requirements for Installation

* Windows, Linux or Mac OS X all will work (see notes below for Mac OS X)
* Vivado
* JDK 1.8 or later NOTE: If you plan on using the Qt Jambi framework in a Windows environment, you will need the 32-bit JRE (Qt Jambi 4.6.3 had yet to be compiled in 64-bit Windows as of the writing of this document).
* In addition, the distribution provides copies of a number of JAR files required for use by RS2.

### Steps for Installation For Command Line Usage

The first task is to acquire RS2.  This will require a git client.  You can acquire the RS2 distribution by executing the following:

     git clone [https://github.com/xrtc/RapidSmith2](https://github.com/srtc/RapidSmith2)

The second task is to create an environment variable called RAPIDSMITH\_PATH and point it at the RapidSmith2 directory thus created.  This is needed so RS2 can find the required device files and other items as it runs.

The third task is to build RS2.  At this point you have two choices: setting up RapidSmith2 for use with Eclipse or building RapidSmith2 manually to generate .class and .jar files which you can then use with any Java installation.

#### Building for Eclipse

RS2 requires Eclipse Neon or later so install that.

Then, create an eclipse project by executing one of the following (depending on your system):

    gradlew eclipse    # Will need to change the permissions of gradlew to allow execution

    gradlew.bat eclipse

Executing these will create a .project file.  Once you have done this you can import the project into Eclipse by opening Eclipse and selecting:

    File->Open Projects From File System

and pointing it to the RapidSmith2 directory created when you cloned RS2 from github above.

All of the Java source files will be found in Eclipse under src/main/java.

#### Building Manually

Execute one of the following to build RS2:

     gradlew build     # Will need to change the permissions of gradlew to allow execution

     gradlew.bat build

This will produce a variety of things, any of which can be added to your CLASSPATH as needed:

1. The resulting RS2 class file directory tree will be found in build/classes/main.
2. A jar file of the above RS2 class files can be found in build/libs.
3. Both tar and zip files can be found in build/distributions. They contain a full jar of the RS2 build along with copies of other needed jar files. You should add them all to your CLASSPATH except the qtjambi ones - just add the qtjambi one for your particular system (note there is no 64-bit qtjambi for windows so use the 32-bit one).

At this point you should be able to write tools that use RS2.

An obvious thing to try is to mix and match – developing in Eclipse but then running the resulting apps from the command line. Just be aware that Eclipse puts its compiled .class files in very different places than where the manual build process puts its .class files. Make sure you understand that before you try that.

### Additional Notes for Mac OS X Installation

* The instructions above require you to set the RAPIDSMITH\_PATH environment variable. If running from the command line, the environment variables can be added to your .bash\_profile file as in any other UNIX-like system. However, if using an IDE such as Eclipse, you either need to define the environment variable for every Run Configuration you create you create in Eclipse or you need to add the RAPIDSMITH\_PATH definition system-wide in OS X. This can be done, but how to do so differs based on what OS X version you are running (and seems to have changed a number of times over the years). Search the web for instructions for how to do so if you desire. Hint: you will likely have to edit some .plist files.

### Running RS2 Programs

Some points to keep in mind:

* The RS2 code base contains a number of assertions which may be helpful as you are developing code. These are not enabled by default in Java. To enable them, add “-ea” as a VM argument.
* If you are running on a Mac, when running RS2 programs that use Qt (any of the built-in programs like Device Browser) that are GUI-based, you will need to supply an extra JVM switch, “-XstartOnFirstThread”.
* A common error when running RS2 programs is failing to have your RAPIDSMITH\_PATH defined. If this is the case you will typically get file open failure messages as RS2 tries to load device files and the like.

### Testing Your Installation

At this point you can test your installation by executing the java DeviceBrowser program (edu.byu.ece.rapidSmith.device.browser.DeviceBrowser). This can be done either from within Eclipse or from the command line, depending on how you are running RS2 (if running under OS X be sure to provide the –XstartOnFirstThread JVM argument.

If all goes well you should see a graphical representation showing the details of a physical FPGA device as shown in Figure 2.

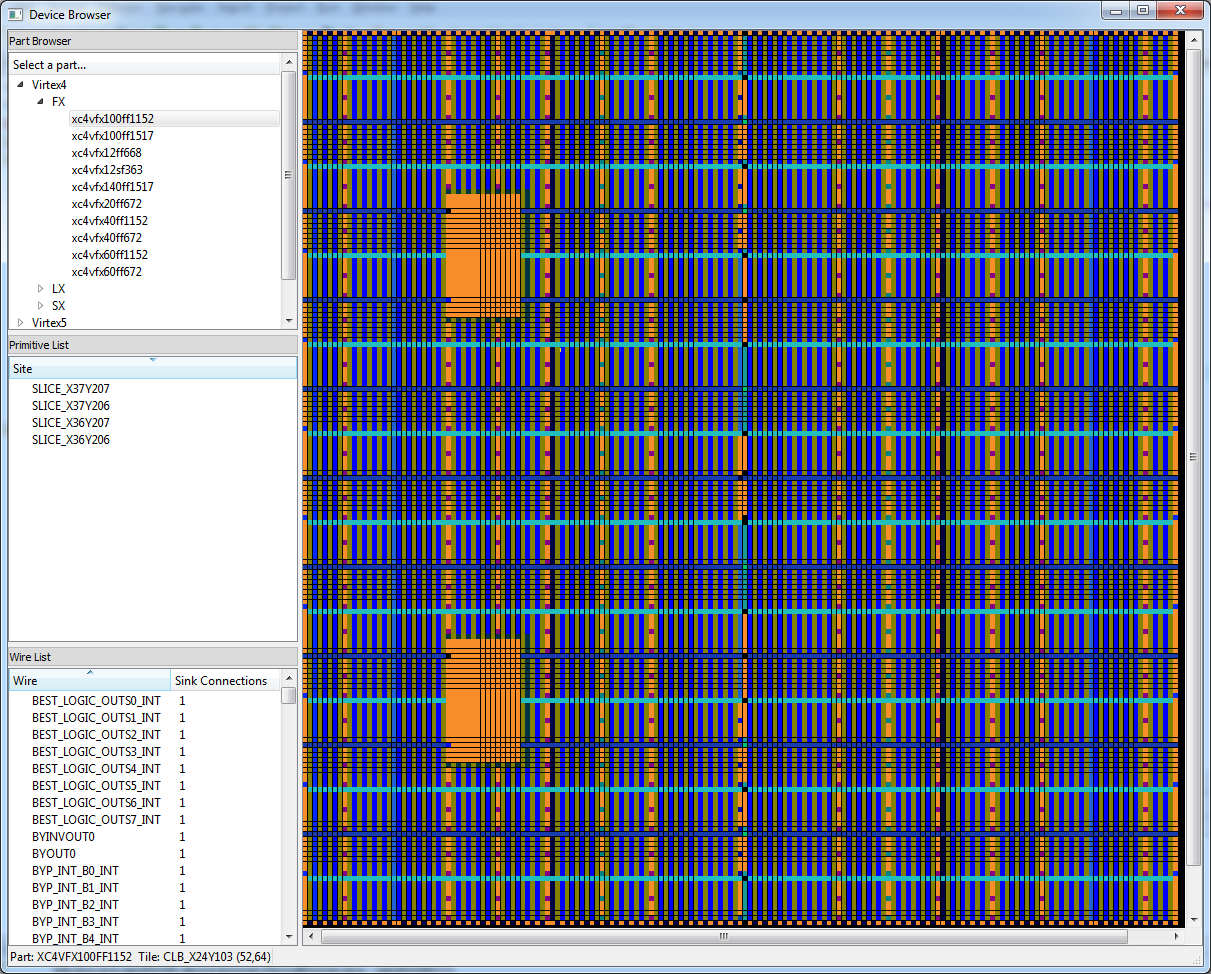


Figure – Device Browser Sample Display

### Device Files For Use With RS2

Device files for one part (the xc7a100tcsg324) are included in the distribution so you can immediately start working with RS2 using this part (initially, it will be the only device available when you run the DeviceBrowser above). If you desire to work with additional parts, follow the instructions found in this documentation in **Section 7 Generating Device Files in RS2** on page 20.

# Example RS2 Programs

A variety of example programs can be found in the examples2 directory in the RS2 installation (edu.byu.ece.rapidSmith.examples2). They have been heavily commented and so provide a means to learn the RS2 API by example as we believe this is much better than reading a lot of text trying to teach you what you need to know.

There is a README.txt file in that directory to provide an overview and suggested order for learning from the examples.

In addition, the subsections below describe one or more built-in RS2 programs which you might find useful.

## Device Browser

Note: this is a program from RapidSmith, but which is discussed here because it is still very useful in RS2.

This GUI program is located in the edu.byu.ece.rapidSmith.device.browser package. It will let you browse parts at the tile level.  On the left, the user may choose the desired part by navigating the tree menu and double-clicking on the desired part name.  This will load the part in the viewer pane on the right (the first available part is loaded at startup).  The status bar in the bottom left displays which part is currently loaded.  Also displayed is the name of the current tile which the mouse is over, highlighted by a yellow outline in the viewer pane. The user may navigate inside the viewer pane by using the mouse.  By right-clicking and dragging the cursor, the user may pan.  By using the scroll-wheel on the mouse, the user may zoom.  If a scroll-wheel is unavailable, the user may zoom by clicking inside the viewer pane and pressing the minus(-) key to zoom out or the equals(=) key to zoom in.

All that is required for this to operate is a valid device file (no design required).

See below for a screenshot.

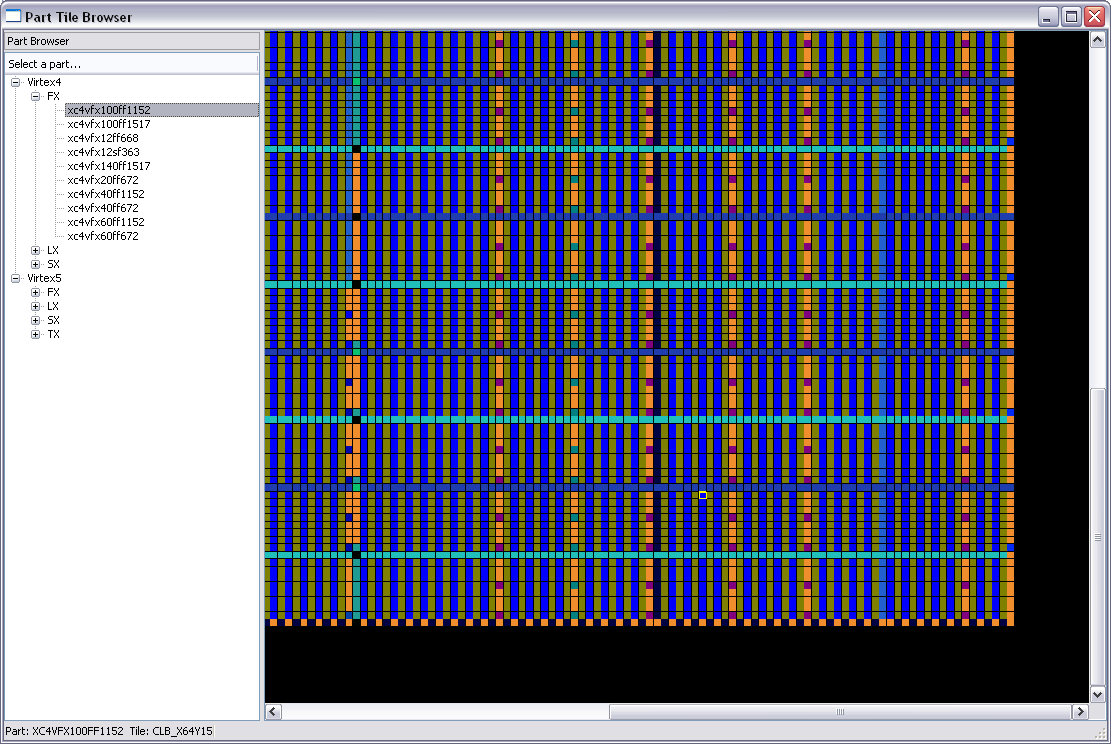


Figure – Screen Shot of DeviceBrowser

The device browser also allows the user to follow the various connections found in the FPGA. By double clicking a wire in the wire list, the application will draw the connection on the tile array (as shown in the screenshot below). By hovering the mouse pointer over the connection, the wire becomes red and a tooltip will appear describing the connection made by declaring the source tile and wire followed by an arrow (->) and the destination tile and wire. By clicking on the wire, the application will redraw all the connections that can be made from the currently selected wire. By repeating this action, the user can follow connections and discover how the FPGA interconnect is laid out. This is shown below. Thanks to Chris Lavin for originally creating this app.

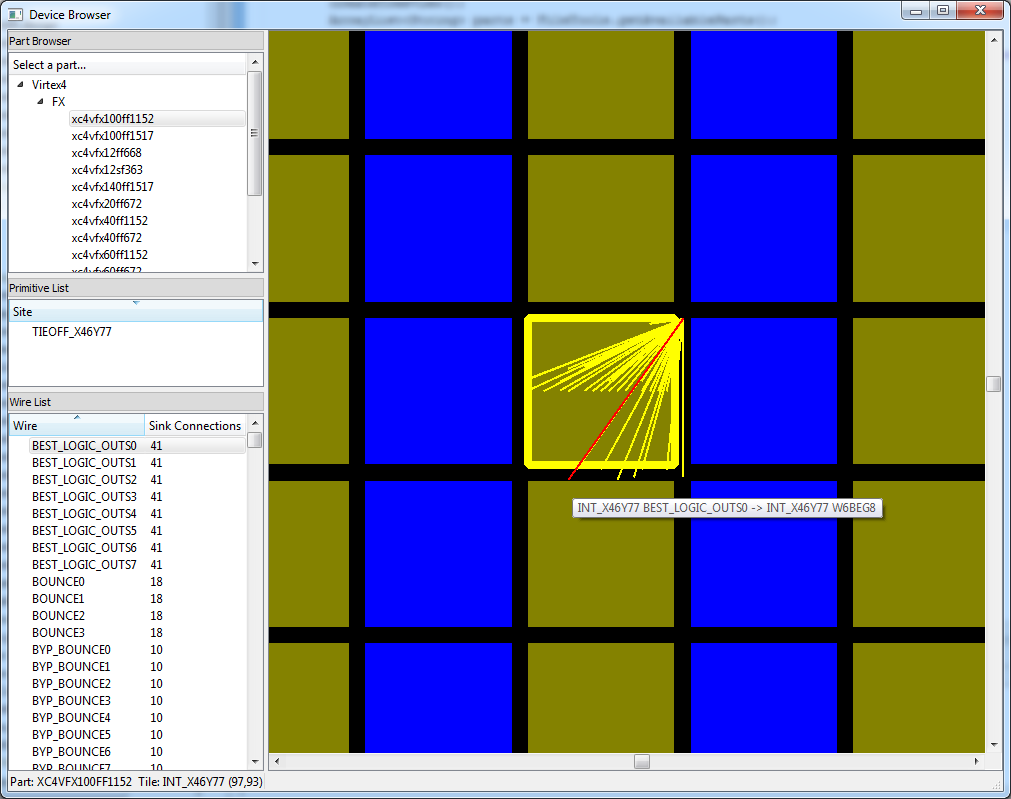


Figure – DeviceBrowser Screen Shot Showing Wire Connections

## The DesignAnalyzer Test Program

This program, along with a number of other example programs, is located in the edu.byu.ece.rapidSmith.examples2 package. After loading a design from a checkpoint, it simply walks the design data structure, printing out what it finds as it goes. As such, it provides a nice example of a number of things which would be useful for getting started with RS2:

1. How to enumerate the cells in a design, determine and print their placement information as well as their properties.
2. How to enumerate the logical nets in a design and print out their source and sink pins.
3. How to traverse and print out the physical route for a logical net (if it is routed)

## The DeviceAnalyzer Test Program

This program is also located in the examples2 package. It is designed as a simple getting started program and demonstrates how to query and print tiles in a device and wires in a tile.

## Other Test Programs

See the README.txt file in the edu.byu.edu.rapidSmith.examples2 package directory. It outlines the other test programs there which may be useful in coming up to speed on RS2.

# Designs in RS2

## Designs in RS2

Designs in RS2 are similar to the designs found in Vivado (and which are exported as EDIF files from Vivado).

They are essentially logical netlists. They are represented and stored in the data structures found in the **design.subsite** package. A *CellDesign* consists of a collection of *Cell* objects, interconnected by *CellNet*s. *CellNet*s connect to the *CellPin*s on *Cell*s. CellNets typically have one source pin and one or more sink pins. *Cell* objects have a name, properties, pins, a link to the library cell they are an instantiation of, etc.

*Cell*s may be placed onto *Bel*s and the corresponding *CellPin*s mapped onto *BelPin*s. *CellNet*s, when physically routed, map onto one or more *RouteTree*s.

## The Cell Class

The example programs mentioned above provide examples of manipulating Cell objects. Here are a few things you should know about cells, in no particular order:

* A Cell always contains a reference to an object of type LibraryCell, which serves as a template for its construction.
* Cells may be physically placed onto BELs in the device. This is done by setting the Cell’s *anchor* value to point to the BEL it resides on. If you know where you want a Cell placed you can just place it there. On the other hand, RS2 provides a way to identify the site/bel combinations where a Cell could be placed. See the program CreateDesignExample in the examples2 directory for an illustration of how to do it both ways.
* Cell objects have pins on their periphery where CellNets connect to.
* The top-level ports of a design are tied to IPORT, OPORT, or IOPORT Cell objects. These are pseudo-cells (you won’t find them in Vivado) and represent the terminal points for signals leaving or entering the top-level.

### Cell Properties

Cells as represented in EDIF files coming from Vivado may contain properties. For example, a D flip flop cell (FDRE) has a CONFIG.INIT property, indicating what its power-up state should be. These properties can be set to modify the Cell’s behavior. The DesignAnalyzer test program described above pretty-prints an RS2 logical design and, as a part of its operation, it lists the properties set on each Cell in the design. Here are some additional things about properties you should know:

* It might be of interest, however, to learn what properties *could* be set for a given cell. This set of properties can be found in the cellLibrary.xml files generated for a given family (see the $RAPIDSMITH\_PATH/devices directory to find these XML files for any devices installed). The files are quite readable and from them you can learn much about the available LibraryCell types for a given FPGA family). At some point in the future this information will be incorporated into the RS2 data structures so that user programs can query them and so RS2 can check whether they are legal values when set by a user program. For now, user code can set properties and those will be exported into EDIF when going from RS2 back into Vivado. However, no error checking will be done by RS2 as this is done.
* In a GUI view of devices in Vivado you will see polarity inverter in many sites allowing for programmable selection of a signal or its inverse. This is shown in the GUI in the form of a 2:1 MUX. The CLK signal and its inverse entering a SLICE is an example of this. However, this is not explicitly represented in the device representation. Rather, properties on the Cells driven by the mux output signals muxes indicate whether the signal is inverted or not. For example, generate a 4-bit counter using rising-edge triggered flip flops in Vivado and generate an EDIF file for it. You will see that the counter is constructed, in part from FDRE cells. Now, modify the HDL for your counter to make it a falling-edge triggered counter and compare the resulting EDIF file. The difference you will see is that the property on each of the FDRE cells called CONFIG.IS\_C\_INVERTED has been set, indicating it is a falling-edge triggered flip flop. When bitgen is actually done by Vivado, the corresponding clock inverter will be programmed accordingly.
* It should go without saying that since there is only one such clock inverter in a SLICE, all the flip flops in a slice must be either rising-edge triggered or falling-edge triggered (they must have the same CONFIG.IS\_C\_INVERTED *control set* value). If you violate this, Vivado will throw an error. Similar restrictions exist for all cells in a site driven by shared programmable inverters. For example, flip flops in a slice (FDRE LibraryCells) share programmable inverter on their clock, D, and R inputs.

## The CellNet Class

A CellNet has a type. Legal values are WIRE, GND, VCC, and UNKNOWN. The WIRE type is the one used for normal signals. CellNets have one source pin and one or more sink pins (these are of type CellPin). The CellNet class has methods for traversing these.

GND and VCC nets have some special characteristics. There is a single logical VCC net. It is driven by a single *RapidSmithGlobalVcc* cell. The output pin of that cell is the source of all VCC in the design. However, unlike other cells which get routed to, this cell is never physically placed. The situation with GND is similar.

### Physical Routing of CellNets in RS2

A CellNet is physically routed by determining the metal segments and intervening PIPs that are to be used to make up the route. A physical net is called a Wire and contains some number of RouteTree objects. A given RouteTree object has the source of the route as its root and then branches represent the branching of the route between source and sink. See later in this manual for a description for the RouteTree class. The physical routing of a net is represented by attaching one or more RouteTree objects to the net.

Normal wires (CellNets of type WIRE) have only one RouteTree, reflecting the fact that they have a single source and multiple sinks. Note that a wire cannot be physical routed to the pin of a cell which has not yet been routed.

Physically, GND and VCC nets have some unique characteristics compared to other wires. Most importantly, when a circuit has been routed by Vivado the result will be multiple physical VCC routes and multiple physical GND routes in the circuit. Each route is represented by its own RouteTree object. The source for each of these RouteTree objects will be a wire which is connected to a TIEOFF. These TIEOFFs are not physically placed but their locations can be inferred by the source wire for each of the RouteTrees making up the VCC or GND route.

Once a CellNet’s physical routing has been created as a RouteTree, that is converted to a *directed routing string* when RS2 designs are exported from RS2 back into Vivado. The DesignAnalyzer program in the examples2 directory gives an example of tracing out the RouteTrees which represent a physically routed wire.

# Devices in RS2

## Devices in RS2

A device is defined in RS2 as a unique Xilinx FPGA part that includes package information but not speed grade (such as the xc7a100tcsg324 device included in the RS2 distribution). Each device contains specific information concerning its primitive sites, tiles, wires, IOBs, and PIPs that are available to realize designs. The device information is represented in RS2 in the **device** package. RS2 has significantly extended the original RapidSmith D**evice** class for its use as well as how device files are generated.

A *Device* object consists of a collection of *Tile*s, each of which contains one or more *Site*s. A *Site* contains one or more *Bel*s. *Site*s have *SitePin*s around their periphery and *Bel* objects have *BelPIN*s around theirs.

The physical wires in the device are represented by objects of type *Wire*, *TileWire*, and *SiteWire*. However, the goal of RS2 is to largely hide the differences between these three wire object types and let the user simply deal with *Wire* objects.

The previously-mentioned DeviceBrowser and DeviceAnalyzer programs illustrate how to load and browse a device down to the Tile and Wire levels.

## Generating Device Files in RS2

RS2 is distributed with a single device file included (for an Artix7 device). The device files for this can be found in the ${RAPIDSMITH\_PATH}/devices/artix7directory and consist of a \*\_db.dat file and a \*\_info.dat file.

Additional device files for a family can be generated by a user. If these are additional device files for an already-supported device family, the process is relatively straightforward. The document: ${RAPIDSMITH\_PATH}/devices/doc/InstallingNewDevices.txt provides instructions on how to generate new device files for supported families. These should be adequate to generate new device files for families with existing support.

If you need device file support for a new family, the process is more difficult. Contact the authors for possible help in doing so.

# Routing in RS2

Because understanding the routing graph in RS2’s device representation is crucial to being able to manipulate routing, this chapter provides a more detailed discussion to help users and developers.

## Wire Resources in RapidSmith

RS2 has a unique way of representing wires and connections for Xilinx devices. This approach was developed mainly to minimize disk and memory usage while also maintaining some level of efficiency and speed.

### Wire Representation

The device files generated by RS2 each contain a list of all uniquely XDLRC-named wires that exist in a given Xilinx FPGA family. Wires can span multiple tiles in the FPGA, however, the wire has a separate name for each tile in which it crosses. An example of this concept is illustrated in the DOUBLE lines found in several family architectures. A DOUBLE line is a wire that connects switch boxes either one or two hops away in a given direction. An example of this layout is given in Figure 5.



Figure - A DOUBLE line in an FPGA illustrating how each part of the wire has a different name depending on the tile it is located in.

In this example, we see a wire that can be driven by one point, E2BEG4, and can drive either E2MID4 in tile INT\_X2Y1 and/or E2END4 in tile INT\_X3Y1. However, the wire is assigned a name as it travels through the CLB tiles (CLB\_E2BEG4 and CLB\_E2MID4). For the purposes of RS2, these wires have been removed from device files as they do not contribute to the overall possible connections a wire can make and simply add overhead to the device data structures. This technique has dramatically reduced the size of the devices files and improved routing speed as dead-end connections do not need to be examined.

In RS2, these uniquely-named wire segments are represented either as a String or as an int or Integer. Often it is represented as an integer to save space and increase comparison speed with other wires. To illustrate how this representation works, here is some example Java code that exposes the wire segments:

|  |
| --- |
| // Load the appropriate Device and WireEnumerator  // (this is done automatically when loading XDL designs)  String partName = "xc4vfx12ff668";  Device dev = FileTools.*loadDevice*(partName);  WireEnumerator we = FileTools.*loadWireEnumerator*(partName);  // Here we pick a wire name  String wireName = "E2BEG4";  // Here we get the integer enum value for that wire name  **int** wire = we.getWireEnum(wireName);  // The wire enumerator also keeps information about these wire segments  // such as wire direction and type  WireDirection direction = we.getWireDirection(wire);  WireType type = we.getWireType(wire); |

Now, there are actually several wires in an FPGA device with the same name. The wire E2BEG4 exists in almost every switch box tile in the FPGA. To uniquely identify routing resources in a device, a tile and its name or wire enumeration is required (that is, INT\_X1Y1 E2BEG4 is its unique representation).

In an effort to save space and ultimately reuse much of the routing connections, the WireConnection class is used to represent internal and external tile connections. Each tile has a special hash map where the key is the integer enum value of the wire and the value is an array of WireConnection objects. Each WireConnection object contains the following information to define a connection:

|  |
| --- |
| /\*\* The wire enumeration value of the wire to be connected to \*/  **private** **int** wire;  /\*\* The tile row offset from the source wire's tile \*/  **private** **int** rowOffset;  /\*\* The tile column offset from the source wire's tile \*/  **private** **int** columnOffset;  /\*\* Does the source wire connected to this wire make a PIP? \*/  **private** **boolean** isPIP; |

The WireConnection objects can define the connecting wire by using the integer enumeration value of the wire name and a relative offset of the tile differences between the two wires (again, relative to save space and increase reuse of the object). The WireConnection object also defines if the connection made is a programmable connection (or PIP). When the row and column tile offsets are both 0, the connection exists within the same tile and is likely a PIP.

To query the connections that can be made from INT\_X1Y1 E2BEG4, here is some sample Java code to illustrate how this is done:

|  |
| --- |
| // Load the appropriate Device and WireEnumerator  // (this is done automatically when loading XDL designs)  String partName = "xc4vfx12ff668";  Device dev = FileTools.*loadDevice*(partName);  WireEnumerator we = FileTools.*loadWireEnumerator*(partName);  // Here we pick a wire name  String wireName = "E2BEG4";  // Here we get the integer enum value for that wire name  **int** wire = we.getWireEnum(wireName);  String tileName = "INT\_X1Y1";  Tile tile = dev.getTile(tileName);  WireConnection[] wireConnections = tile.getWireConnections(wire);  **for**(WireConnection w : wireConnections){  System.*out*.println(tileName + " " +  wireName + " connects to " +  dev.getTile(tile.getRow()-w.getRowOffset(),  tile.getColumn()-w.getColumnOffset()) + " " +  we.getWireName(w.getWire()) + " (is" +  (w.isPIP()? " " : " not ") +  "a PIP connection)");  } |
| **Console Output:**  INT\_X1Y1 E2BEG4 connects to INT\_X1Y1 BOUNCE1 (is a PIP connection)  INT\_X1Y1 E2BEG4 connects to INT\_X1Y1 BOUNCE2 (is a PIP connection)  INT\_X1Y1 E2BEG4 connects to INT\_X3Y1 E2END4 (is not a PIP connection)  INT\_X1Y1 E2BEG4 connects to INT\_X2Y1 E2MID4 (is not a PIP connection) |

Routes in XDL are specified only with PIPs. Non-PIP connections (that is E2BEG4 to E2MID4, etc.) are not declared in an XDL Net since the connection is implied. The two wire segments are part of the same piece of metal on the FPGA. Thus, when declaring the routing resources used in a Net (the list of PIPs), these connections are not explicitly listed. However, the PIP connections are, for example:

|  |
| --- |
| net "main\_00/i\_ila/i\_dt0/1/data\_dly1\_20" ,  outpin "main\_00/i\_ila/i\_dt0/1/data\_dly1\_20" XQ ,  inpin "main\_00/i\_ila/i\_yes\_d/u\_ila/idata\_70" BY ,  pip CLB\_X16Y48 XQ\_PINWIRE2 -> SECONDARY\_LOGIC\_OUTS2\_INT ,  pip CLB\_X18Y48 BYP\_INT\_B4\_INT -> BY\_PINWIRE0 ,  pip INT\_X16Y48 SECONDARY\_LOGIC\_OUTS2 -> OMUX7 ,  pip INT\_X17Y48 OMUX\_E7 -> **E2BEG4** ,  pip INT\_X18Y48 **E2MID4** -> BYP\_INT\_B4 ,  ; |

The listing of PIPs in XDL is arbitrary, that is, they do not always follow from one connection to the next.

## Basic Routing

RapidSmith has included an AbstractRouter class that allows for a common template so that routers can be constructed quite easily. However, the user should not feel restricted in using this template as it may not meet everyone’s needs and/or requirements.

An example BasicRouter class has also been provided to illustrate how a router can be constructed easily. The BasicRouter class is ~400 lines of code. It is very simple and does not do any routing conflict resolution (it is a basic Maze router implementation) and it will commonly be unable to route certain connections in a design. Also, because the timing information for Xilinx parts is not publicly available, the router must use other means to optimize the router rather than delay. However, it does perform re-entrant routing, that is, it will attempt to route all nets that don’t have any PIPs while keeping the original routed nets intact. If a net is impartially routed or improperly routed before given to the router, it does not resolve these problems. The behavior and mechanics of this router are described in the remainder of this section.

### Router Structure

The basic router provided in RapidSmith is based on a simple maze router algorithm. It does not allow routing resources to be used more than once, and thus, routing resources come on a first-come-first-served basis. This makes for a very simple implementation but does not resolve routing conflicts when they arise. The router chooses a route by iterating through a growing set of nodes, represented by the Node class. A node is a unique tile and wire combination to uniquely identify any routing wire available in the FPGA. Nodes are given a cost based on their Manhattan distance from the sink of the current connection to be routed and then placed in a priority queue. Those nodes with the smallest cost propagate to the bottom of the queue.

The least cost node of the queue is iteratively removed. With each removal, the node is examined for its expanding connections and those new potential nodes are also placed on the queue. Each time a node is removed, it is tested to see if it is the sink, if it is, the method traverses the path it has found and returns, otherwise it continues to expand more connections of the current node.

The router uses the following basic algorithm:

1. The central routing method, routeDesign() prepares the nets in the design for routing.
2. For each net in the design, routeDesign() will call routeNet().
   1. routeNet() prepares each inpin or sink in the net for routing.
      1. If this is the first inpin of the net, it will only supply the outpin or source of the net as a starting point to the router.
      2. If this is the second or later inpin routed in the net, all intermediate points along those routes are added as starting points.
   2. For each inpin, routeNet() will call routeConnection().
      1. routeConnection() initializes the priority queue of potential source nodes.
      2. routeConnection() calls the main routing method route() for each connection to be routed.
         1. The route() method iterates over the nodes in the priority queue, expanding their connections and adding new ones to the queue and putting more connections on the queue. The process continues until the sink is found.
3. After a net has been routed, the routing resources used will be marked as used to avoid reusing the resources twice.

### Routing Static Sources (VCC/GND)

One major preparation step in routing a full design is preparing where the static sources will be supplied from. The basic primitive in all Xilinx FPGAs to supply VCC and GND signals to a design is the TIEOFF. The TIEOFF accompanies every switch matrix and has several connections to all sink connections to its neighboring logic tile (CLB, BRAM, DSP, etc.). It has 3 pins, HARD0 or GND, KEEP1 (VCC) and HARD1 (VCC). By default, without any configuration, it seems that pins will default to KEEP1. Some pins, however, require a HARD1 when specified to be driven with VCC.

The StaticSourceHandler class takes care of partitioning the various nets and sinks into their respective tiles and instancing the TIEOFF automatically. It also will instance SLICEs when necessary. It also “reserves” certain routing resources for certain nets that could potentially introduce routing conflicts later. These reserved nodes are released just before the net is routed in the basic router.

### Routing Clocks

When routing clocks, it is quite important that they get routed to the appropriate clock tree routing resources. The best current method to determine this is based on the WireDirection (the type CLK was placed in WireDirection because there are certain CLK wires that also fell into certain WireType categories). The cost function for determining node position in the priority queue take into account clock wires and significantly reduces their cost when routing clock nets.

### Internal Pin Names and External Pin Names

In RapidSmith, there is the notion of each pin on an instance having an internal name and an external name. This can easily get confusing, especially where this can be a weak point for XDLRC report files which lack some of this information for some primitive types.

Internal pin names occur commonly in two places (although, they do occur in other places):

1. In XDL nets which contain “outpin” and “inpin” statements
2. In XDLRC primitive\_def declarations in the primitive\_defs section of an XDLRC report.

First, let’s talk about pins found in nets in XDL designs. In XDL, pins in a net are declared first with either the keyword “outpin” (to designate the source) or “inpin” (to designate a sink). Following the keyword is the name of the instance the pin belongs to. To illustrate this, let’s look at an example:

net "netName" ,

outpin "fred" Y ,

inpin "barney" RST ,

pip CLB\_X14Y4 Y\_PINWIRE1 -> BEST\_LOGIC\_OUTS5\_INT ,

pip DCM\_BOT\_X15Y4 SR\_B0\_INT3 -> DCM\_ADV\_RST ,

pip INT\_X14Y4 BEST\_LOGIC\_OUTS5 -> OMUX8 ,

pip INT\_X15Y5 OMUX\_EN8 -> N2BEG0 ,

pip INT\_X15Y7 N2END0 -> SR\_B0 ,

;

In the example above, there are two pins, a source and a sink. The source is found on the instance “fred” and the sink is found on the instance “barney.” The source pin on “fred” is pin “Y” and the sink pin is “RST” on “barney.”

However, a problem arises when trying to use pin names in routing. For example if the pin name Y were used to specify routing to the instance it would be ambiguous because the Y pin belongs to a slice. Since PIPs declare routing resources at the tile level, the pin Y would have to be unique to the tile, however, there are actually multiple slices in a CLB tile making the reference “Y” ambiguous. To eliminate the ambiguity, Xilinx developed what we call an internal pin name and external pin name. The internal pin name (Y and RST in the example) is used when talking about a pin on an instance, however, to route to/from that pin the external name is used. In the PIP list of the example net above, the first PIP contains the external name “Y\_PINWIRE1” of pin Y on “fred” and the second PIP contains that external name “DCM\_ADV\_RST” of the pin RST. In the Virtex 4 architecture, there are 4 slices in each CLB, so the Y pin on each slice is named Y\_PINWIRE0, Y\_PINWIRE1, Y\_PINWIRE2 and Y\_PINWIRE3 respectively. The mapping of an internal pin name to an external pin name is found in the primitive\_site declaration in an XDLRC report.

Let’s look at an example of an XDLRC primitive\_site:

|  |
| --- |
| (primitive\_site SLICE\_X1Y126 SLICEL internal 27  (pinwire BX input BX\_PINWIRE1)  (pinwire BY input BY\_PINWIRE1)  (pinwire CE input CE\_PINWIRE1)  (pinwire CIN input CIN1)  (pinwire CLK input CLK\_PINWIRE1)  (pinwire SR input SR\_PINWIRE1)  (pinwire F1 input F1\_PINWIRE1)  (pinwire F2 input F2\_PINWIRE1)  (pinwire F3 input F3\_PINWIRE1)  (pinwire F4 input F4\_PINWIRE1)  (pinwire G1 input G1\_PINWIRE1)  (pinwire G2 input G2\_PINWIRE1)  (pinwire G3 input G3\_PINWIRE1)  (pinwire G4 input G4\_PINWIRE1)  (pinwire FXINA input FXINA1)  (pinwire FXINB input FXINB1)  (pinwire F5 output F51)  (pinwire FX output FX1)  (pinwire X output X\_PINWIRE1)  (pinwire XB output XB\_PINWIRE1)  (pinwire XQ output XQ\_PINWIRE1)  (pinwire Y output Y\_PINWIRE1)  (pinwire YB output YB\_PINWIRE1)  (pinwire YQ output YQ\_PINWIRE1)  (pinwire COUT output COUT1)  (pinwire YMUX output YMUX\_PINWIRE1)  (pinwire XMUX output XMUX\_PINWIRE1)  ) |

XDLRC report files show a mapping of internal pin name to external pin name on each line which starts with “(pinwire”. The pattern is:

“(pinwire <internal pin name> <direction of pin> <external pin name>)”

This is very straight forward and is the second common location to find internal and external pin names in XDL/XDLRC. In RapidSmith, the mapping between internal and external pin names can be made using the following methods:

In the PrimitiveSite class:

/\*\*

\* Gets the external wire enumeration of the name of the wire corresponding to the

\* internal wire name.

\* **@param** internalName The internal wire name in the primitive.

\* **@return** The corresponding external wire enum (Integer) name of the internal wire

\* name.

\*/

**public** Integer getExternalPinName(String internalName);

In the Device class:

/\*\*

\* Gets the external wire enumeration on the instance pin.

\* **@param** pin The pin to get the external name from.

\* **@return** The wire enumeration of the internal pin on the instance primitive of

\* pin.

\*/

**public** Integer getPrimitiveExternalPin(Pin pin);

There is a problem, however, with some primitive types and getting mappings for their internal pin names to external pin names. Sometimes, a primitive type does not have a native primitive site in any device in Xilinx FPGA family. Therefore, the primitive must be placed on a compatible primitive site of a different type. For example, an IOB primitive instance does not have a native site on most families. However, it is fully compatible with IOBM or IOBS sites.

In certain instances, the internal pin names differ on the primitive with no native sites to the sites on which it can be placed. The biggest example of this is in the Virtex 5 which has 9 different primitive types which all use the same primitive site type (RAMBFIFO36). Because the RAMBFIFO36 site is declared several times in the Virtex 5 devices, all of the internal-to-external pin mappings are available. However, 8 other sets of mappings are not present. The lack of mappings makes routing designs which contain these primitives impossible. The solution to this problem is to apply a patch with the proper mappings. A complete patch will be included with RapidSmith in a future release.

# Importing/Exporting Designs Between Vivado and RS2

# Bitstreams in RS2

In the original RapidSmith, bitstreams can be parsed, manipulated, and exported for Virtex 4, Virtex 5 and Virtex 6 Xilinx FPGA families. Because of the proprietary nature of Xilinx bitstreams, RapidSmith provided only documented functionality when working with bitstreams (and was limited mainly to manipulation at the frame level including helping to assemble sequences of configuration commands which are interpreted by the FPGA configuration controller circuitry). While this has proven valuable to many researchers, it does not provide the ability to create your own bitstream from scratch because it does not provide the specific meaning of each bit in a bitstream. If you desire to use RapidSmith’s bitstream manipulation features, you should download and work with RapidSmith instead of RS2. If you do so, note that it has not been tested beyond Virtex 6. The authors would be interested in upgrading RapidSmith’s bitstream functionality to device families beyond Virtex 6 if users create it and are willing to contribute it to us for inclusion.

# Legal and Dependencies

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RS2 includes the Caucho Technology Hessian implementation which is distributed under the Apache License. A copy of this license is included in the doc directory in the file APACHE2-LICENSE.txt. This license is also available for download at:

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Source for the Qt Jambi project is available at:

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The user is responsible for providing copies of these licenses and making available the source code of these projects when redistributing these jars.

# Appendix

Here we may put a grouping of useful topics that do not fit in with the rest of this document.

1. An XDL-based import/export capability has also been created and used with Virtex 6 devices as a part of Travis Haroldsen’s PhD work but that path is not being released, documented, or supported. [↑](#footnote-ref-1)