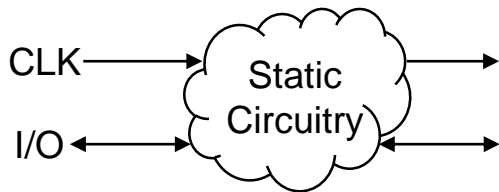


# FPGA

## Static Region



CLK →

I/O ↔

Static  
Circuitry

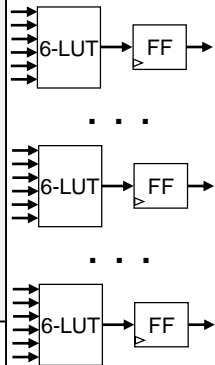
PR  
Region

RM 4

RM 3

RM 2

RM 1



6-LUT

FF

...

6-LUT

FF

...

6-LUT

FF