Hardware Security Project

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Created on Oct 4 2014, Modified on November 15, 2014

Outline

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Oct 8 , 2014

Three Parts of Work

- *Sheng Wei*
  - The main point of the paper is to develop an one-gate trojan trigger circuit. The attack circuitry is on TrustHub. TrustHub has various kinds of attacking circtuits' verilog codes.
  - Sheng works on only a small part of the project for developing triggers. He can help us develop the trigger but not the attacking circtuit.
  - Leakage power analysis has been applied for detecting trojans that are off at first and then turned on later. For example, trigger can comes from a counter.

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Second part

- *Ronen*
  - The whole circuit's photonics response is simulated by adding up single gate response. **Gate-to-gate wires are excluded.**
  - There is a space issue with the single gate design. The attenuation for the reflected signal is too small. The way to solve this problem is to change the layout to bring more open space for Ronen.
  - One good way to solve the signal attenuation is to utilize the open space for antenna design. My idea is to fill the antenna with the rest of the circuit. Ronen agrees that it will bring the reflected back signal much stronger.
  - Ronen needs a month after I handling him the standard cells. So that will push my work's deadline to the end of Oct.

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Oct 15 , 2014

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A *'Good Trojan'* in Information Leakage

Size

The area of added circuit must be small due to extra energy consumption and die size.

Side-Channel Leakage

In order to leak information, the circuit must consume more energy for secret info transmitting. A *'good Trojan'* must consume energy as small as possible but leak information as much as possible.

Trigger

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AES-T100 Explanation

- *Side Channel Attack* This method is implemented with power side channel attack. It leaks the secret information through CDMA channel.
- *CDMA Leakage* The attacking circuit consists of a PRNG for spread spectrum. In this way, the leakage information will be distributed through many cycles so that the leakage power analysis can not detect the information
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Trojan Free Layout

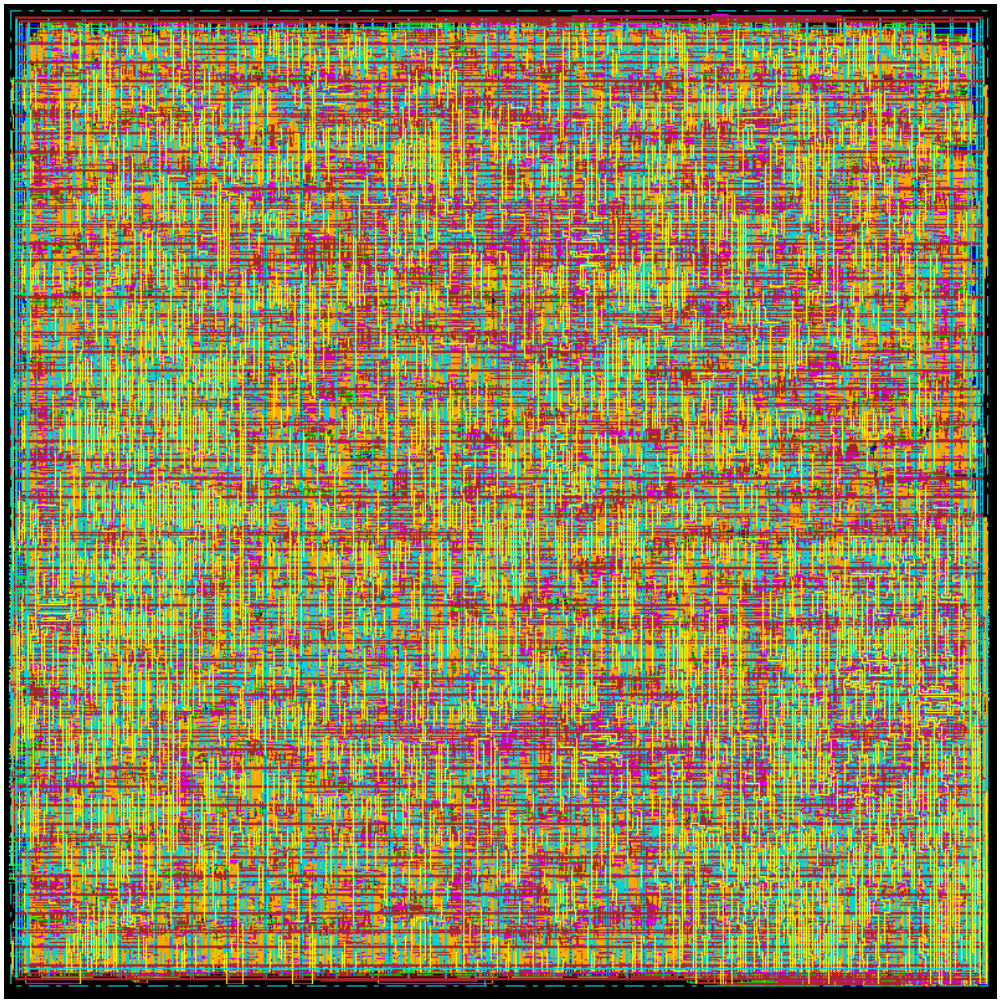

Figure: AES-T100 Trojan Free Circuit

Trojan Free Layout Without Filler Cells

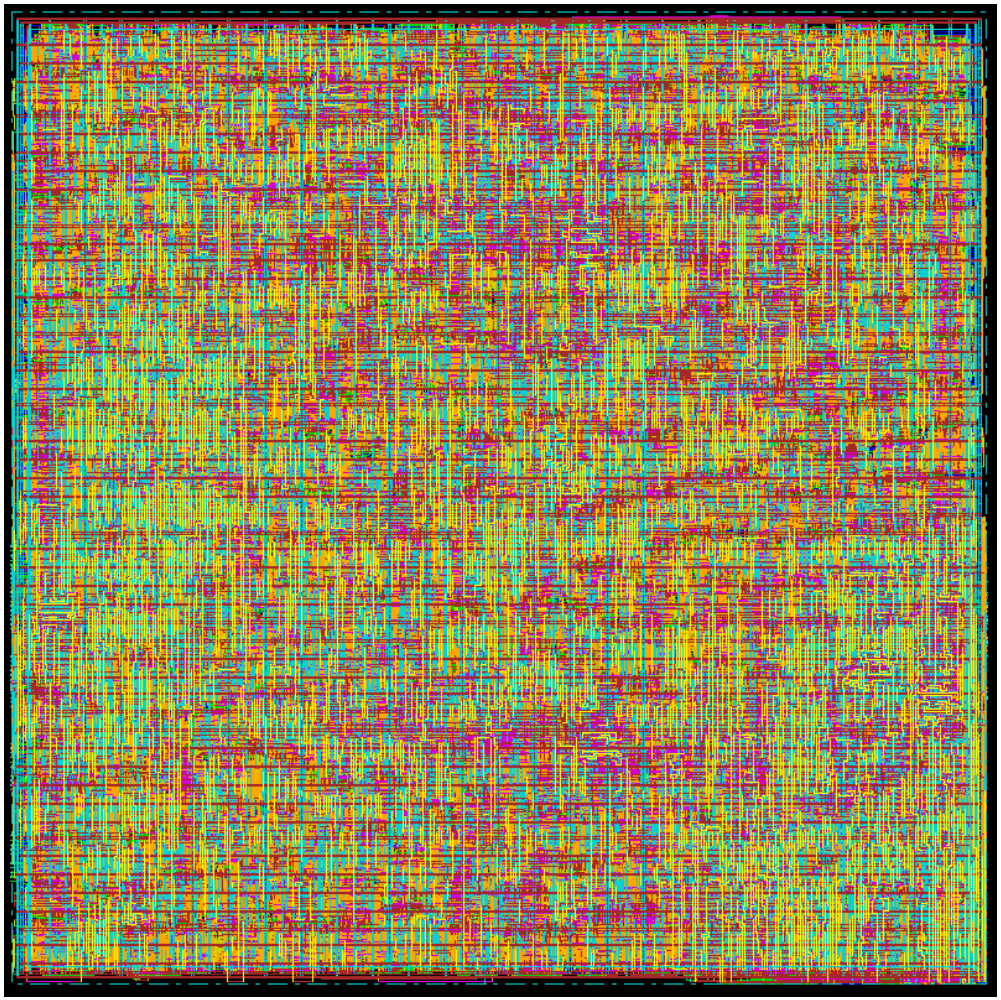

Figure: AES-T100 Trojan Free Circuit without Filler Cells

Trojan In Layout

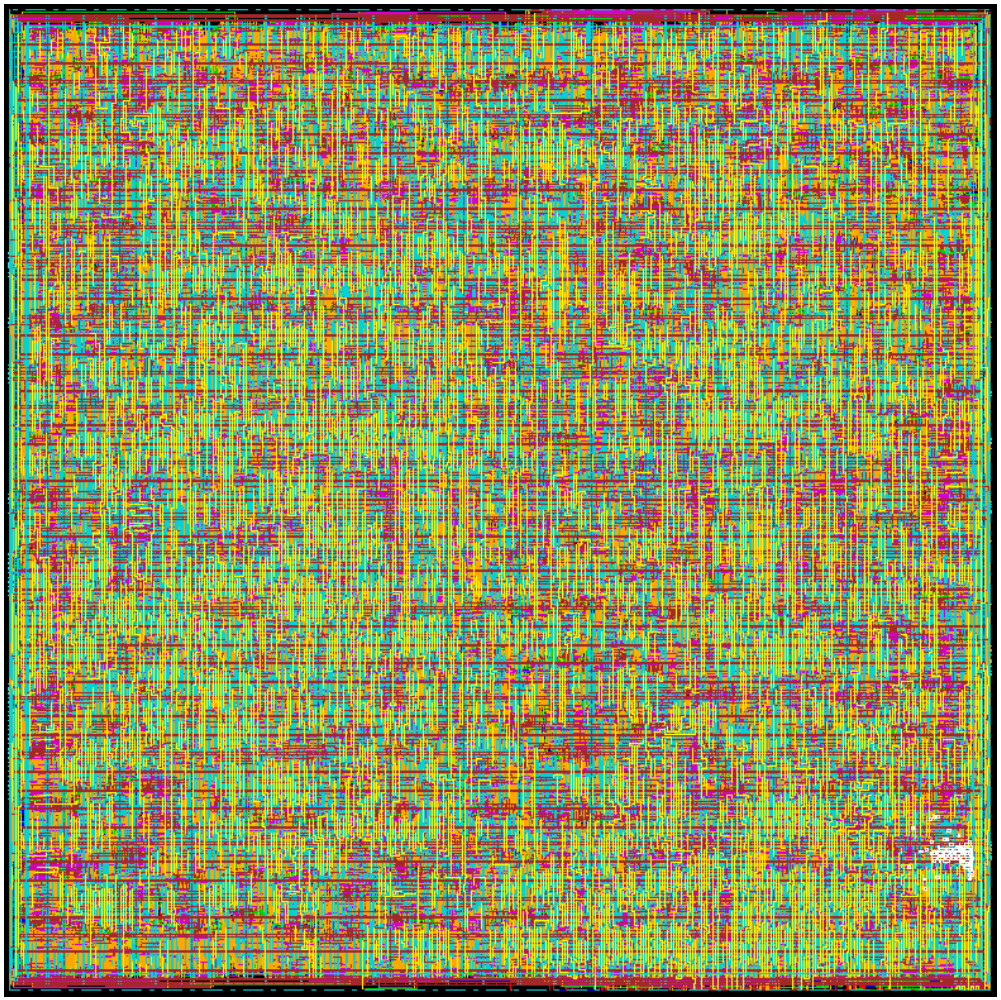

Figure: AES-T100 Trojan Inserted Circuit

Trojan Free Layout Without Filler Cells

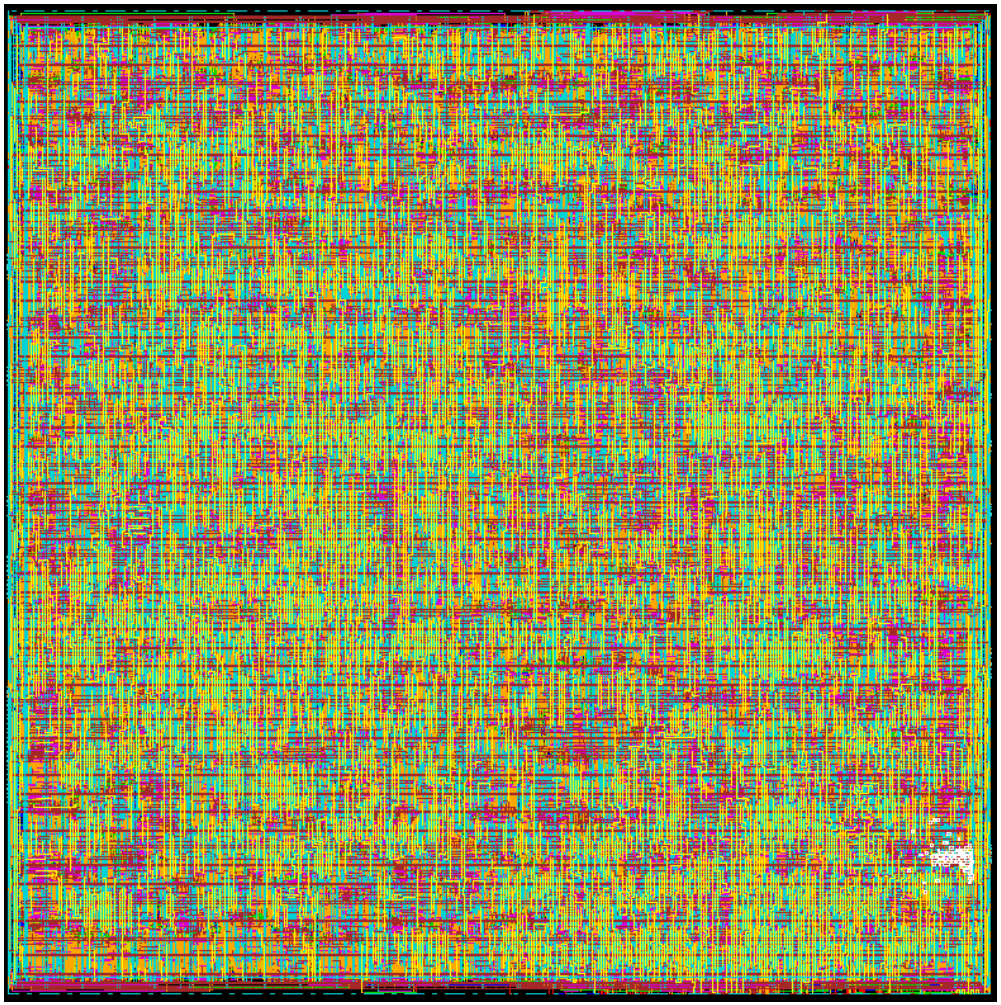

Figure: AES-T100 Trojan Inserted Circuit without Filler Cells

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b15-T100

- **Functionality** Slows down part of the cicuit by reducing the clock frequency by half.
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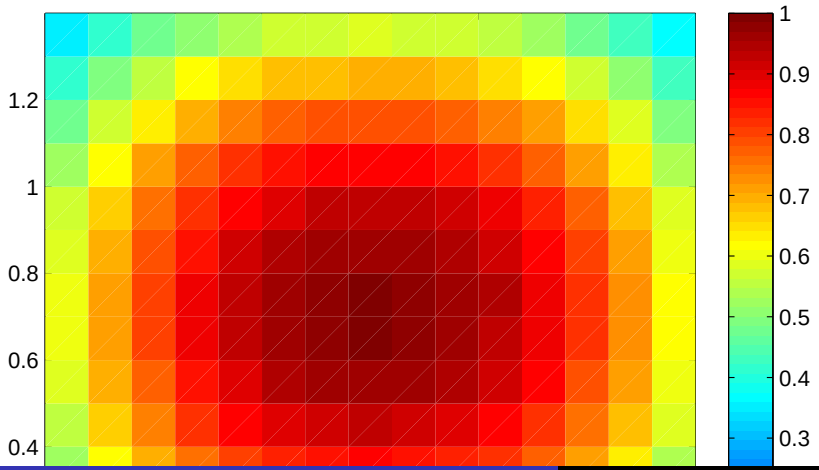

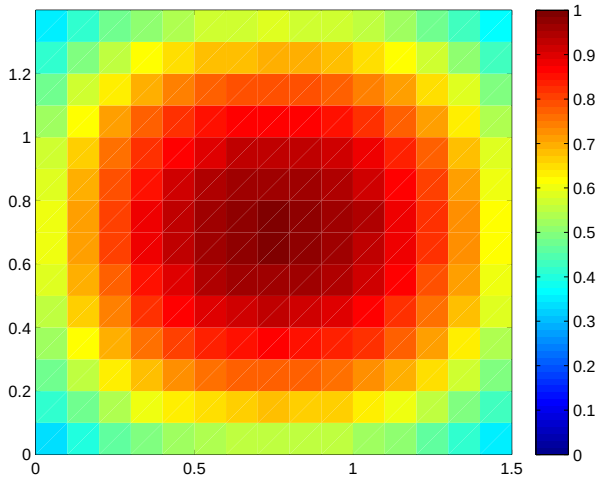

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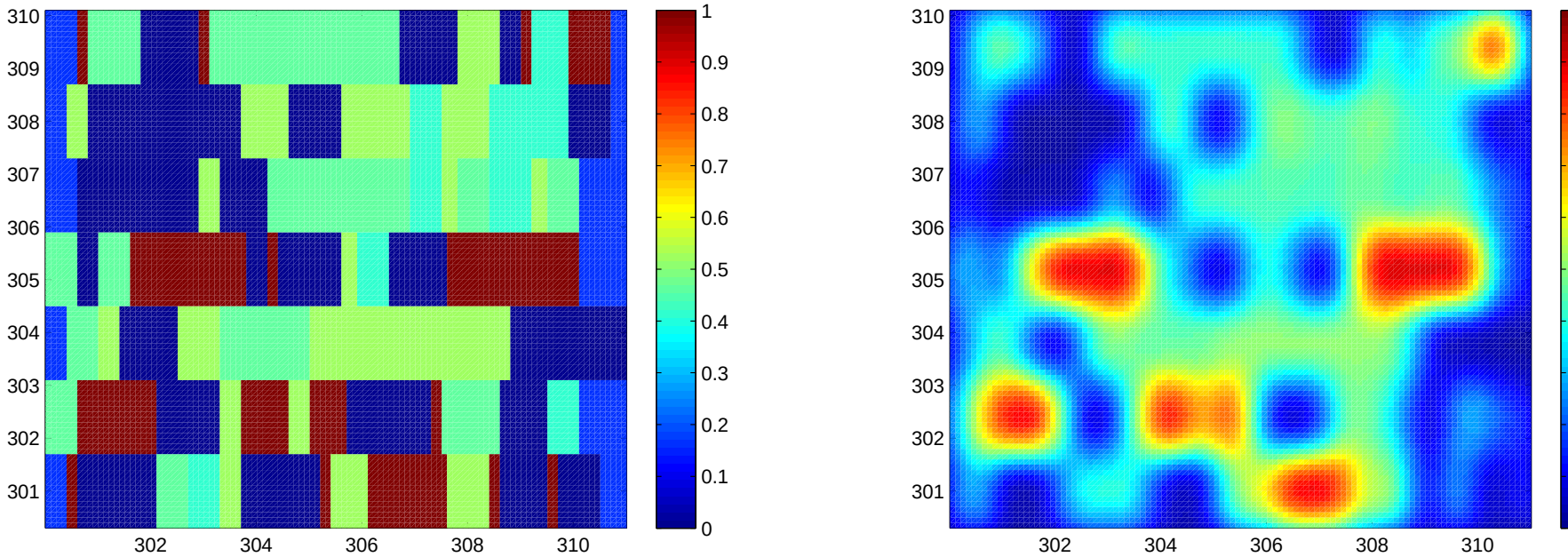
Circuit with Trojans Response



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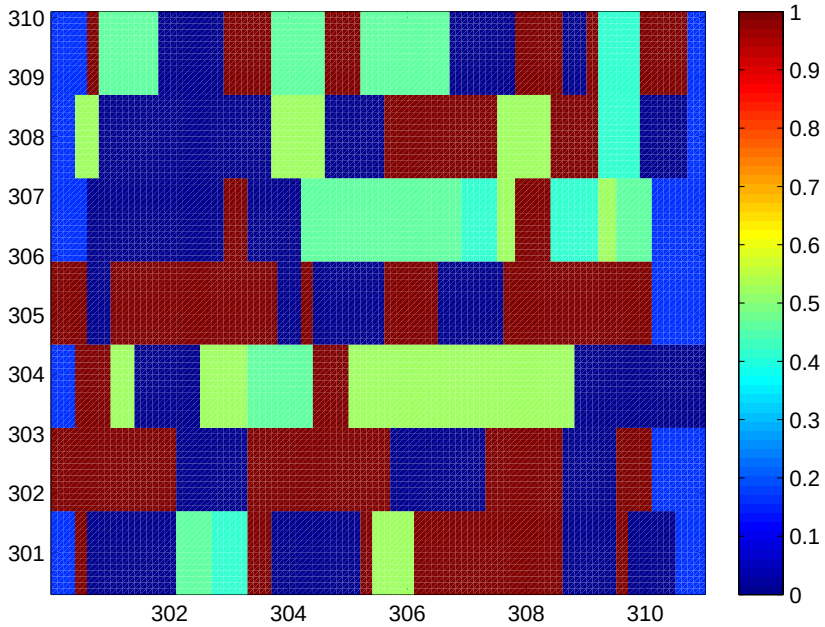


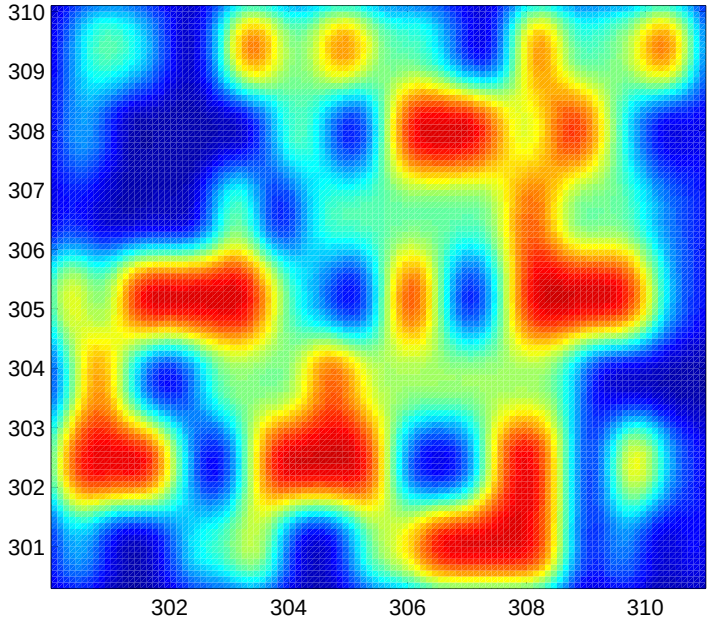
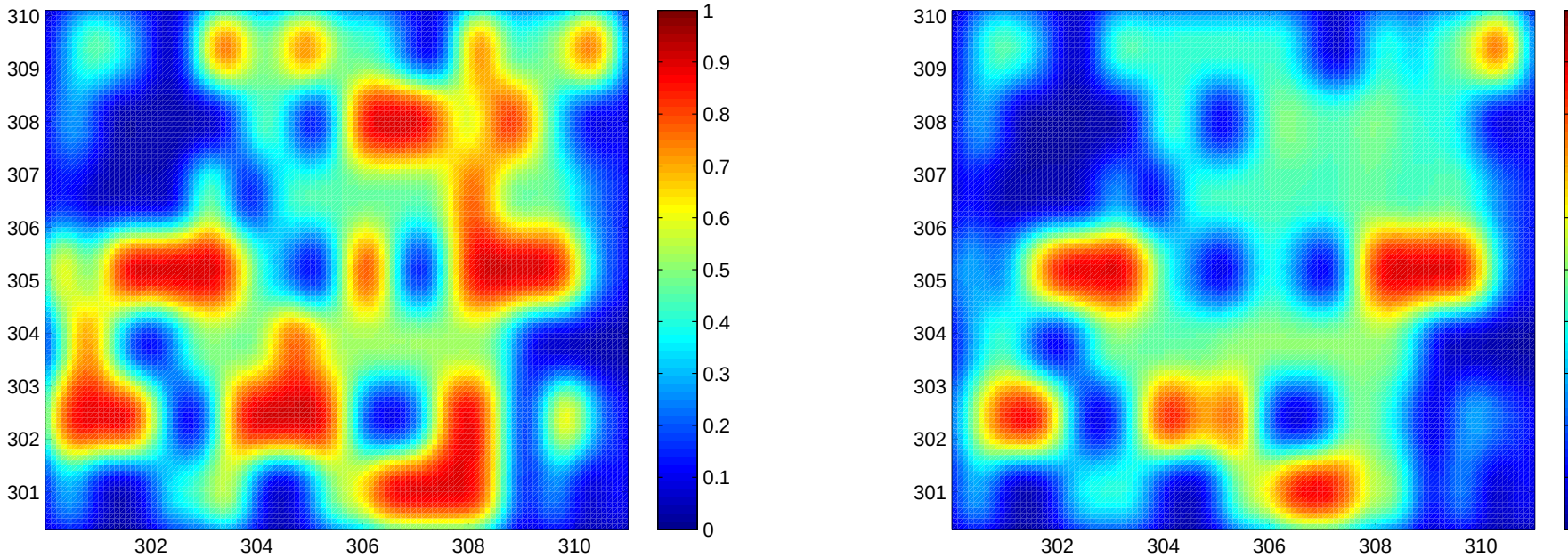


Figure: Circuit without Trojans

Response Comparison



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Error Rate of False Alarm

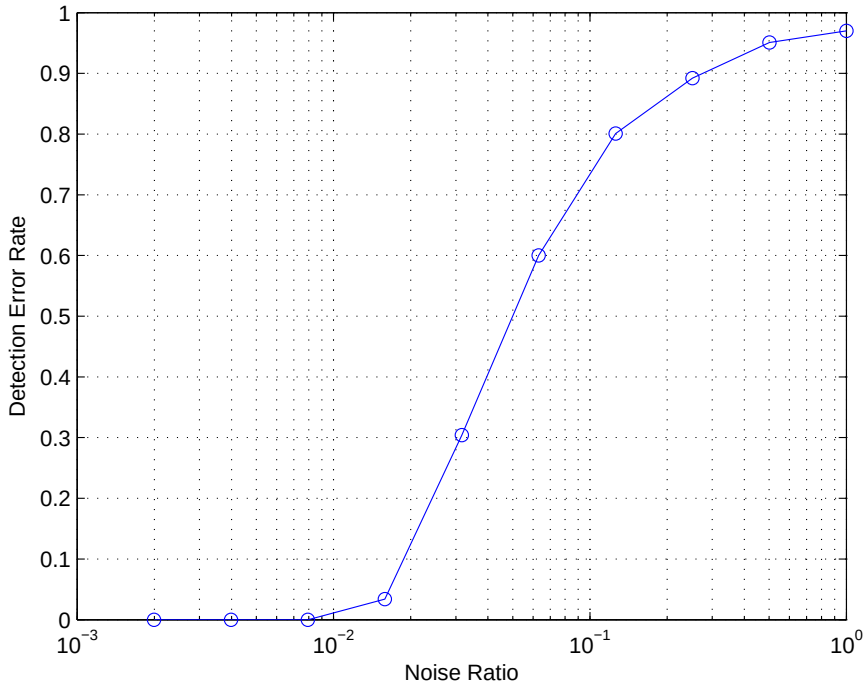
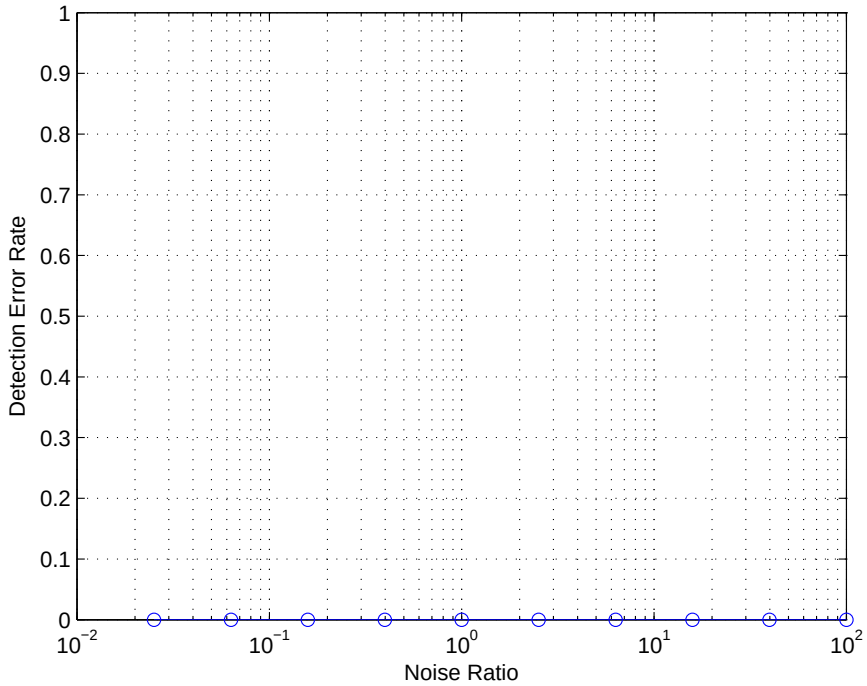


Figure: Error Rate of False Alarm

Error Rate of Miss Test



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Trojan Free Response

Trojan In Response

Trojan In minus Trojan Response

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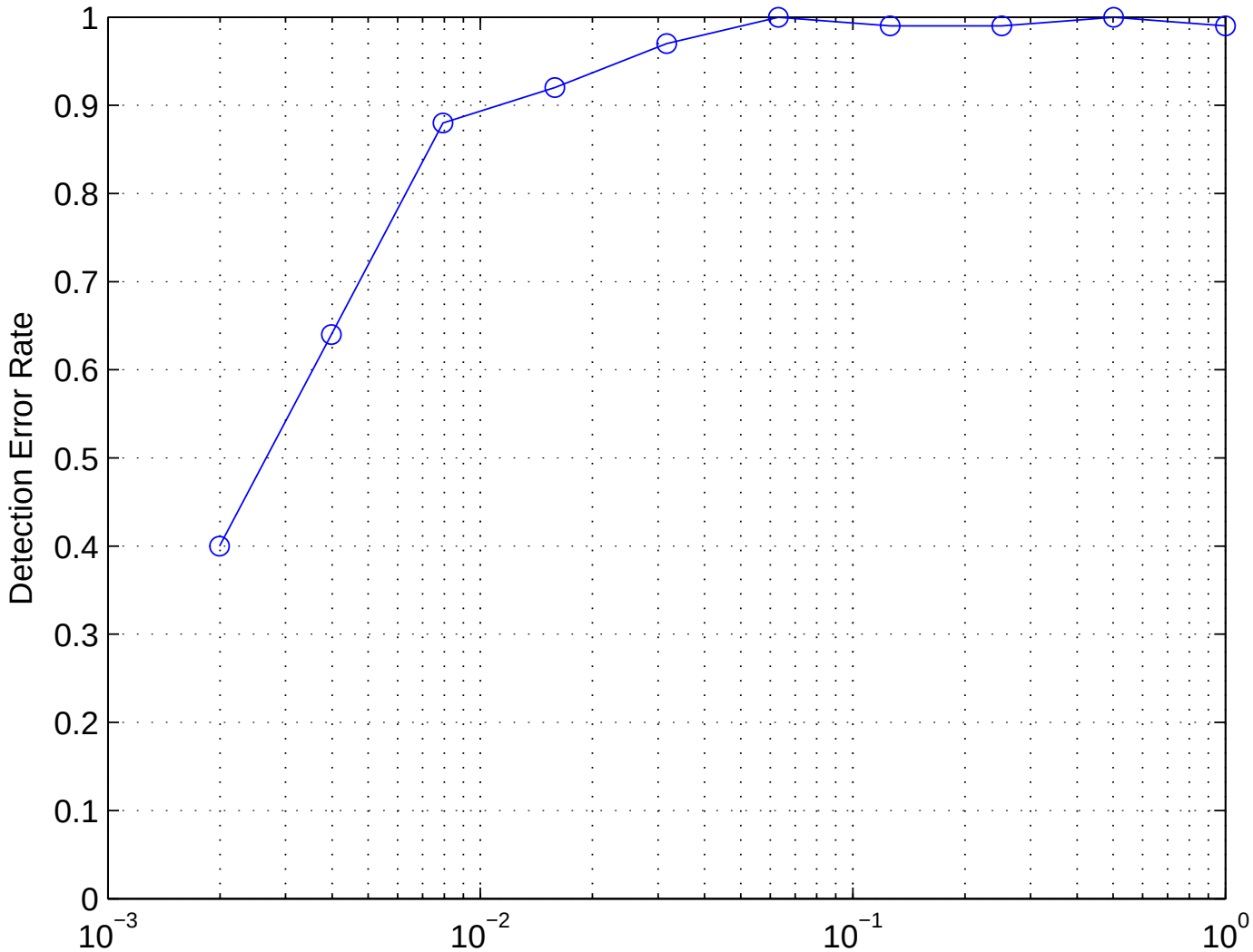

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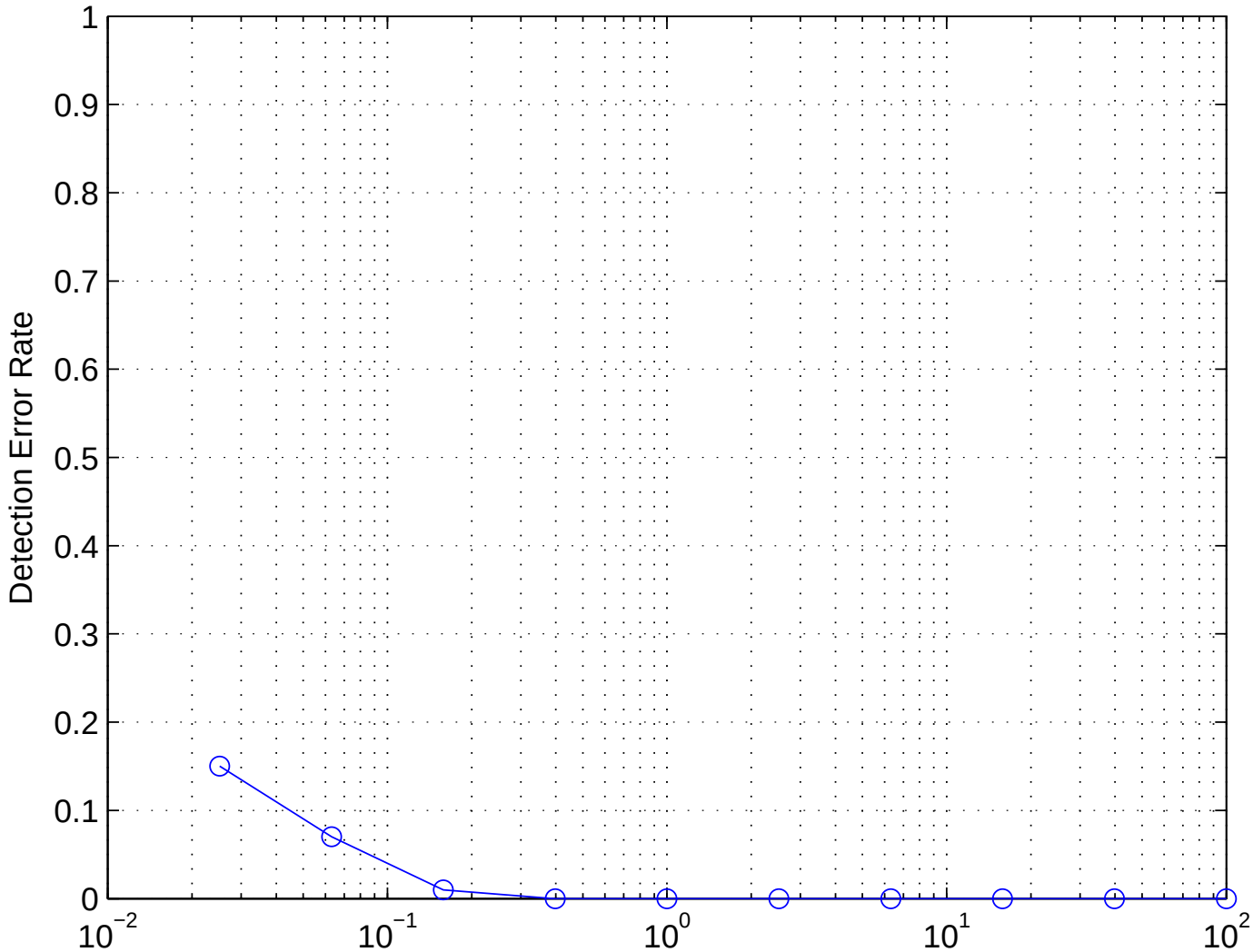

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