

# Han(Ben) Zhang

H Zhang2002@outlook.com | (925) 336-4668 | San Diego, CA |  
linkedin.com/in/Han-Zhang-2002 | han-zhang.cn | github.com/bz010

## CAREER PROFILE

Aspiring hardware designer with a strong passion for **hardware** acceleration and **embedded systems**, currently pursuing a Master's in Computer Engineering at UC San Diego. Proficient in **RTL** coding, **simulation**, and **synthesis** using industry-standard tools like **Intel Quartus**, with hands-on experience in **FPGA** design and **PCB** prototyping. Successfully participated in international **automotive** and **robotics** prototyping competitions, further honing expertise in **digital system design**. Demonstrated leadership in cross-functional teams and led critical projects in battery management systems and real-time data analysis, driving measurable improvements in system performance. Dedicated to leveraging technical expertise in **FPGA** prototypes, **Linux** server projects, and **PCBA design** to innovate and solve complex engineering challenges.

## EDUCATION

### UNIVERSITY OF CALIFORNIA, SAN DIEGO

Expected June 2026

*Master of Science, Computer Engineering*

- Coursework in Computer Architecture, **VLSI**, and **FPGA** design.
- Key Projects: Design **VLSI** hardware accelerator for the VGG algorithm.

### UNIVERSITY OF CALIFORNIA, SAN DIEGO

September 2020 - June 2024

*Bachelor of Science, Computer Engineering*

- Coursework in **Computer Architecture**, **Machine Learning**, and Operating Systems Design.
- Cumulative GPA 3.15 / 4.0, Major GPA 3.31/4.0

## TECHNICAL SKILLS

- 3D Modeling Skills: SolidWorks, Autodesk Fusion 360.
- ECAD/PCBA modeling and validation: OrCAD Allegro, **Altium**, **Pspice**, Wire harness design and manufacture.
- Programming Skills: **C Language**, **Assembly**, **C++**, **Python**, Git/CICD, Website development, and Linux Operation.
  - Including TensorFlow, ROS2, PyTorch, Artificial Intelligence, and Machine/Deep Learning.
- FPGA and Signal Processing: **Verilog**, **System Verilog**, ModelSim, DSP, and **MATLAB/LabView**.
  - Including Quartus compile and validation and CANBUS design.
- Native in Mandarin and English. Working proficiency in German.

## LEADERSHIP EXPERIENCE

### Society of Automotive Engineers - Triton Racing, Vice President / Electrical Lead

March 2021- June 2024

- Electrical Lead till 05/2023, Vice President 05/2023 – 06/2024.
- Led cross-functional collaboration between engineering and business teams, streamlining workflows and improving efficiency.
- Directed end-to-end design and manufacturing of Formula-style racecars, reducing production time by 15%.
- Supervised by Professor Maziar Ghazinejad.
- Spearheaded Battery Management System project for 2023 EV car using **Altium** PCB Designer, successfully prototyping an 80kWh battery and 400kW HV system.
- Led UCSD team to secure 4th place out of 120 colleges in FSAE Michigan competition by optimizing vehicle performance through real-time data analysis through **Python** Model.
- Improved data acquisition and analysis systems using **MATLAB**, increasing racing performance and driver training efficiency by 50%.

## WORK EXPERIENCE

### Servo Motor Firmware R&D Intern, Shanghai, China

June 2023 - September 2023

*Shanghai AMP & MOONS' Automation Co. Limited*

- Developed and implemented SVPWM (Space Vector Pulse Width Modulation) control on an **FPGA** platform, using **MATLAB Simulink** to simulate and optimize the design, achieving a 20% increase in processing frequency compared to the existing TI TMS320 DSP system.
- Prototyped a more precise PWM wave generation system, enhancing control accuracy by 15%, which resulted in improved high-torque performance and motor efficiency.
- Collaborated with cross-functional teams to integrate the new control system into existing hardware, ensuring compatibility and seamless operation within the company's servo motor architecture.
- Documented the development process by creating detailed reports on test results, system performance metrics, and workflow improvements, contributing to knowledge sharing and future iterations.