# AGC: Very quick and incomplete documentation

**Inputs**

clk: 16 MHz Clock Input

RESETn: Active-low reset

amplified\_signal [15:0]: Output of the 16-bit ADC

overload: 1-bit saturation signal

ext\_or\_int: Toggles mode of AGC; when 0, internal\_overload = 1 if amplified\_signal = 16’d16 (i.e. if the ADC output actually saturates the entire 16 bit range)

Note: using the amplified\_signal to adjust gain (i.e. ext\_or\_int=0) has not been tested yet.

**Outputs**

vgaX\_control: Ignore these for now. It’s meant to control the VGAs, but a new mapping logic will have to be created to map to the thermometer code

gain\_array\_out [5:0]: The 6 bit register that stores the current gain value. In the final module, this should only be an internal signal, the mapped vgaX\_controls are the actual outputs we care about.

done\_out: Indicates that all 6 bits have been scanned and/or the preamble time (128us) have passed. The gain will not change once this is 1.

**Internal Modules/Signals**

counter1: Envelope detection timer, currently set to 16 clock cycles (1us @ 16MHz).

counter2: Delay wait timer, currently set to 16 clock cycles.

preamble\_counter: Preamble length counter. Currently set to 2048 clock cycles (128us @ 16MHz).

indicator: a register for the internal\_overload signal

internal\_overload: Either hard wired to the external overload signal, or to the reduction AND of the amplified\_gain signal, depending on the value of ext\_or\_int.

adjust\_pos\_edge: A positive edge detector for the adjust signal, so that only one adjustment to the gain is made per detection period.

up\_dn: Signals whether the gain should be increased or decreased

done: logical OR of the done signal coming from gain\_binary\_search (binary search through all bits of the gain\_array is complete), and the reduction AND of the preamble\_counter.

mapping\_function: Fully combinational mapping logic that maps the gain\_array to the vgaX\_controls.

agc\_controller: FSM, has four states: s\_reset, s\_detect, s\_adjust, s\_done. When active, automatically goes from s\_reset to s\_detect.

* s\_detect
  + counter1 is enabled
  + indicator is enabled. If internal\_overload is on at any point, indicator will stay on
  + Transitions to s\_done if done signal is asserted from top module
  + Transitions to s\_adjust if counter1 reaches 15.
* s\_adjust
  + counter1 is reset and disabled
  + indicator is reset and disabled
  + counter2 is enabled
  + adjust is enabled
  + up\_dn is set according to the past indicator
  + gain\_binary\_search module does all its work in the first/second cycle of s\_adjust
* s\_done
  + Stops all operations

gain\_binary\_search: Performs binary search of gain\_array. Changes gain\_array when clk is high and adjust\_pos\_edge is high. Note: currently only maxes at 38 (6’b100110) due to easier mapping of overall gain range. Therefore special interaction is hardcoded for two transition cases. This may not be necessary in the final module. We can enable the full range and map it to the thermometer coded inputs of the VGA to allow for finer adjustment. Settling time should be the same, as it still only searches for 6 bits.