Zhaori Bi, Ph.D.

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Employment

Jun. 2021 –	**Assistant Professor,** State Key Laboratory of Integrated Chips and Systems, Fudan University, Shanghai
Jun. 2018 – Jun. 2021	**Assistant Researcher,** National Clinical Research Center for Aging and Medicine, Huashan Hospital, Fudan University, Shanghai
Jun. 2016 – Aug. 2016	**Design Automation Engineer Intern,** AMS-AG, Plano, TX
Jun. 2013 – May 2017	**Teaching Assistant,** The University of Texas at Dallas.

Education

Aug. 2013 – Dec. 2017	**Ph.D. Computer Engineering** The University of Texas at Dallas, Richardson, TX., Advisor: Dr. Dian Zhou Thesis: *Efficient and Quality Assured Techniques for Analog Circuit Design Automation*
Aug. 2011 – May 2013	**M.Sc. Electrical Engineering** The University of Texas at Dallas, Richardson, TX., Advisor: Dr. Dian Zhou Thesis: *Near Field Communication System Design with A Circuit Implementation*
Sep. 2009 – Jun. 2011	**B.A.(Second Degree), English Language and LiteratureLetters** Huazhong University of Science and Technology, Wuhan, Hubei.
Sep. 2007 – Jun. 2011	**B.Eng., Electronic Information Engineering** Wuhan University of Technology, Wuhan, Hubei.

Fund

2024 – 2026, lead	**Young Scientists Fund 62304052 (¥300k)** National Natural Science Foundation of China (NSFC)
2023 – 2024, lead	**General Research Project Fund (¥400k)** State Key Laboratory of Integrated Chips and Systems
2019 – 2022, lead	**Shanghai Sailing Program 19YF1405600 (¥200k)** The Science and Technology Commission of Shanghai Municipality (STCSM)

Service

Associate Editor	**VLSI, Integration** since 2023.7
Session Chair	**IEEE ASP-DAC/ASICON** 2023/2023
TPC Member	**IEEE APCCAS** 2018

Service (continued)

Reviewer — **IEEE TBE/TCAD/TCAS-II, ACM TODAES**
since 2018

Teaching

2013 – 2018 (UTDallas TA)

- EE2310 Introduction to Digital Systems
- EE3320 Digital Circuits
- EE3120 Digital Circuits Labs
- EE3101 Electrical Network Analysis Labs
- EE5325 Hardware Modeling using HDL
- EE6301 Advance Digital Logic
- EE6302 Microprocessor System Labs
- EE6306 Application Specific Integrated Circuit Design

2018 – Current (FDU AP)

- MICR130037 EDA system software analysis and design methodology
- MICR130038 Fundamentals of Computer Software
- INFO820021 Analog Circuit CAD Design

Awards

2023

- **Honorable Mention Award**, IEEE ICCAD CAD 2023 Problem C.
- **1st place Award**, OpenDACs 2023 Competition.

2024

- **EDA² Youth Technology Award**
- **ISEDA Best Paper Award**
- **CODES+ISSS Best Paper Nomination**
- **3rd place Award, China Postgraduate Innovation Competition EDA Elite Challenge**
- **2nd place Award, China College IC Competition(Huadong)**

Research Publications (Corresponding author * / Co-first author #)

Conference Proceedings

1. T. Gu, R. Lyu, **Z. Bi***, C. Yan, F. Yang, D. Zhou, T. Cui, X. Liu, Z. Zhang, and X. Zeng, "HiMOSS: A novel high-dimensional multi-objective optimization method via adaptive gradient-based subspace sampling for analog circuit sizing," in *2024 61th ACM/IEEE Design Automation Conference (DAC 24)*, IEEE, 2024.
2. H. Sun, **Z. Bi***, W. Jiang, Y. Lu, C. Yan, F. Yang, W. Hu, S.-G. Wang, D. Zhou, and X. Zeng, "EVDMARL: Efficient value decomposition-based multi-agent reinforcement learning with domain-randomization for complex analog circuit design migration," in *2024 61th ACM/IEEE Design Automation Conference (DAC 24)*, IEEE, 2024.
3. A. Zhao, X. Wang, Z. Lin, **Z. Bi***, X. Li, C. Yan, F. Yang, L. Shang, D. Zhou, and X. Zeng, "cVTS: A constrained voronoi tree search method for high dimensional analog circuit synthesis," in *2023 60th ACM/IEEE Design Automation Conference (DAC 23)*, IEEE, 2023.
4. R. Lyu, A. Zhao, Y. Meng, K. Zhu, **Z. Bi***, C. Yan, F. Yang, D. Zhou, and X. Zeng, "Revisiting sensitivity-based analog sizing with derivative-aware bayesian optimization and error-suppressed adjoint analysis," in *2024 ACM/IEEE International Conference on Computer-Aided Design (ICCAD 24)*, IEEE, 2024.

5. X. Zhao, T. Gao, A. Zhao, **Z. Bi***, C. Yan, F. Yang, S.-G. Wang, D. Zhou, and X. Zeng, "ROI-HIT: Region of interest-driven high-dimensional microarchitecture design space exploration," in *2024 CODES+ISSS (ESWEEK 24)*, IEEE, 2024.

6. T. Gu, J. Wang, **Z. Bi***, C. Yan, F. Yang, Y. Qin, T. Cui, and X. Zeng, "Tss-bo: Scalable bayesian optimization for analog circuit sizing via truncated subspace sampling," in *2024 Design, Automation and Test in Europe Conference (DATE 24)*, IEEE, 2024, p. 1.

7. Y. Meng, R. Lyu, **Z. Bi***, C. Yan, F. Yang, W. Hu, D. Zhou, and X. Zeng, "Circuits physics constrained predictor of static ir drop with limited data," in *2024 Design, Automation and Test in Europe Conference (DATE 24)*, IEEE, 2024, p. 1.

8. X. Zhao, **Z. Bi***, C. Yan, F. Yang, Y. Lu, D. Zhou, and X. Zeng, "Synchronous batch constrained multi-objective bayesian optimization for analog circuit sizing," in *2024 29th Asia and South Pacific Design Automation Conference (ASP-DAC 24)*, IEEE, 2024, p. 1.

9. R. Lyu, Y. Meng, A. Zhao, **Z. Bi***, K. Zhu, F. Yang, C. Yan, D. Zhou, and X. Zeng, "A study on exploring and exploiting the high-dimensional design space for analog circuit design automation," in *2024 29th Asia and South Pacific Design Automation Conference (ASP-DAC 24)*, IEEE, 2024, p. 1.

10. J. Zhao, C. Yan, **Z. Bi**, F. Yang, X. Zeng, and D. Zhou, "A novel and efficient bayesian optimization approach for analog designs with multi-testbench," in *2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC 22)*, IEEE, 2022, pp. 86–91.

11. X. Fu, C. Yan, **Z. Bi**, F. Yang, D. Zhou, and X. Zeng, "A batch bayesian optimization approach for analog circuit synthesis based on multi-points selection criterion," in *2022 IEEE International Symposium on Circuits and Systems (ISCAS 22)*, IEEE, 2022, pp. 2886–2890.

12. Z. Yiyang, L. Li, R. Lyv, **Z. Bi***, C. Yan, and X. Zeng, "HD-MCTS: An analog circuit optimization algorithm based on high-dimensional monte carlo tree search," in *2022 IEEE International Symposium of EDA (ISEDA 24)*, IEEE, 2024.

13. W. Li, **Z. Bi***, and X. Zeng, "High-dimensional analog circuit sizing via bayesian optimization in the variational autoencoder enhanced latent space," in *2022 IEEE International Symposium of EDA (ISEDA 24)*, IEEE, 2024.

14. P. Dong, R. Lyu, C. Wang, J. Chen, L. Jiang, C. Lan, **Z. Bi***, and C. Yan, "Automated design of analog circuits based on parallel trust region bayesian optimization," in *2022 IEEE International Symposium of EDA (ISEDA 24)*, IEEE, 2024.

15. J. Shen, F. Yang, L. Shang, C. Yan, **Z. Bi**, D. Zhou, and X. Zeng, "Topology optimization of operational amplifiers using a performance-aware representation," in *2022 IEEE International Symposium of EDA (ISEDA 24)*, IEEE, 2024.

16. C. Lan, X. Wang, Z. Jiang, H. Pan, K. Zhu, **Z. Bi**, C. Yan, and X. Zeng, "On accelerating domain-specific mc-ts with knowledge retention and efficient parallelization for logic optimization," in *2022 IEEE International Symposium of EDA (ISEDA 24)*, IEEE, 2024.

17. M. Li, **Z. Bi**, D. Zhou, and X. Zeng, "Analog circuit performance bound estimation based on extreme value theory," in *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 15)*, IEEE, 2015, pp. 1–4.

18. **Z. Bi**, W. Li, D. Zhou, X. Zeng, and S.-G. Wang, "Mixed-signal system verification by systemc/systemc-ams and hsim-vcs in near field communication tag design," in *2013 IEEE 10th International Conference on ASIC (ASCION 13)*, IEEE, 2013, pp. 1–4.

Journal Articles

1. A. Zhao, R. Lyu, X. Zhao, **Z. Bi**, F. Yang, C. Yan, D. Zhou, Y. Su, and X. Zeng, "Vtsmoc: An efficient voronoi tree search boosted multi-objective bayesian optimization with constraints for

high-dimensional analog circuit synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2024.

2. X. Zhao, T. Gao, Z. Wu, **Z. Bi***, C. Yan, F. Yang, S.-G. Wang, D. Zhou, and X. Zeng, "Apple-dse: Asynchronous parallel pareto set learning for microarchitecture design space exploration," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2024.

3. T. Gao, Y. Wang, M. Zhu, X. Wu, D. Zhou, and **Z. Bi**, "A risc-v ppa-fusion cooperative optimization framework based on hybrid strategies," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI 24)*, vol. –, no. –, pp. –, 2024.

4. T. Gu, W. Li, A. Zhao, **Z. Bi***, X. Li, F. Yang, C. Yan, W. Hu, D. Zhou, T. Cui, *et al.*, "BBGP-sDFO: Batch bayesian and gaussian process enhanced subspace derivative free optimization for high-dimensional analog circuit synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD 24)*, 2024.

5. Z. Chen, J. Cai, C. Yan, **Z. Bi***, Y. Ma, B. Yu, W. Hu, D. Zhou, and X. Zeng, "Pneurfill: Enhanced neural network model-based dummy filling synthesis with perimeter adjustment," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD 24)*, 2024.

6. J. Bao, J. Zhang, Z. Huang, X. Feng, **Z. Bi**, X. Zeng, and Y. Lu, "Multiagent based reinforcement learning (ma-rl): An automated designer for complex analog circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD 24)*, 2024.

7. B. He, S. Zhang, Y. Wang, T. Gao, F. Yang, C. Yan, D. Zhou, **Z. Bi***, and X. Zeng, "A batched bayesian optimization approach for analog circuit synthesis via multi-fidelity modeling," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD 23)*, 2022.

8. Y. Yang, H. Zhu, **Z. Bi**, C. Yan, D. Zhou, Y. Su, and X. Zeng, "Smart-msp: A self-adaptive multiple starting point optimization approach for analog circuit synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD 17)*, vol. 37, no. 3, pp. 531–544, 2017.

9. A. Zhao, T. Gu, **Z. Bi***, F. Yang, C. Yan, X. Zeng, Z. Lin, W. Hu, and D. Zhou, "D3pbo: Dynamic domain decomposition based parallel bayesian optimization for large-scale analog circuit sizing," *ACM Transactions on Design Automation of Electronic Systems (TODAES 24)*, vol. 1, no. 1, pp. 1–25, 2024.

10. **Z. Bi**, D. Zhou, S.-G. Wang, and X. Zeng, "Optimization and quality estimation of circuit design via random region covering method," *ACM Transactions on Design Automation of Electronic Systems (TODAES 17)*, vol. 23, no. 1, pp. 1–25, 2017.

11. L. Qian, **Z. Bi**, D. Zhou, and X. Zeng, "Automated technology migration methodology for mixed-signal circuit based on multistart optimization framework," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI 14)*, vol. 23, no. 11, pp. 2595–2605, 2014.

12. Y. Wang, **Z. Bi#**, Y. Xie, T. Wu, X. Zeng, S. Chen, and D. Zhou, "Learning from highly confident samples for automatic knee osteoarthritis severity assessment: Data from the osteoarthritis initiative," *IEEE Journal of Biomedical and Health Informatics (JBHI 21)*, vol. 26, no. 3, pp. 1239–1250, 2021.

13. W. Zhang, Q. Du, J. Xiao, **Z. Bi**, C. Yu, Z. Ye, M. Wang, and J. Chen, "Modification and validation of the phosphate removal model: A multicenter study," *Kidney and Blood Pressure Research*, vol. 46, no. 1, pp. 53–62, 2021.

14. W. Zhang, G. Ye, **Z. Bi**, W. Chen, J. Qian, M. Zhang, D. Ding, M. Wang, and J. Chen, "Higher one-year achievement rate of serum phosphate associated with lower cardiovascular mortality in hemodialysis patients," *BMC nephrology*, vol. 22, pp. 1–10, 2021.

15. G. Ye, W. Yang, **Z. Bi**, L. Huang, and F. Liu, "Effects of a high-phosphorus diet on the gut microbiota in ckd rats," *Renal Failure*, vol. 43, no. 1, pp. 1577–1587, 2021.

16 G. Ye, J. Zhang, **Z. Bi**, W. Zhang, M. Zhang, Q. Zhang, M. Wang, and J. Chen, "Dominant factors of the phosphorus regulatory network differ under various dietary phosphate loads in healthy individuals," *Renal Failure*, vol. 43, no. 1, pp. 1076–1086, 2021.

17 **Z. Bi**, M. Wang, L. Ni, G. Ye, D. Zhou, C. Yan, X. Zeng, and J. Chen, "A practical electronic health record-based dry weight supervision model for hemodialysis patients," *IEEE Journal of Translational Engineering in Health and Medicine(JTEHM 19)*, vol. 7, pp. 1–9, 2019.

18 M. Zhang, **Z. Bi#**, X. Fu, J. Wang, Q. Ruan, C. Zhao, J. Duan, X. Zeng, D. Zhou, J. Chen, *et al.*, "A parsimonious approach for screening moderate-to-profound hearing loss in a community-dwelling geriatric population based on a decision tree analysis," *BMC geriatrics*, vol. 19, no. 1, pp. 1–11, 2019.

Thesis

1 **Z. Bi**, *Efficient and Quality Assured Techniques for Analog Circuit Design Automation*. The University of Texas at Dallas, 2017.

2 **Z. Bi**, *Near field communication system design with a circuit implementation*. The University of Texas at Dallas, 2013.