OKI Semiconductor

MSM6255
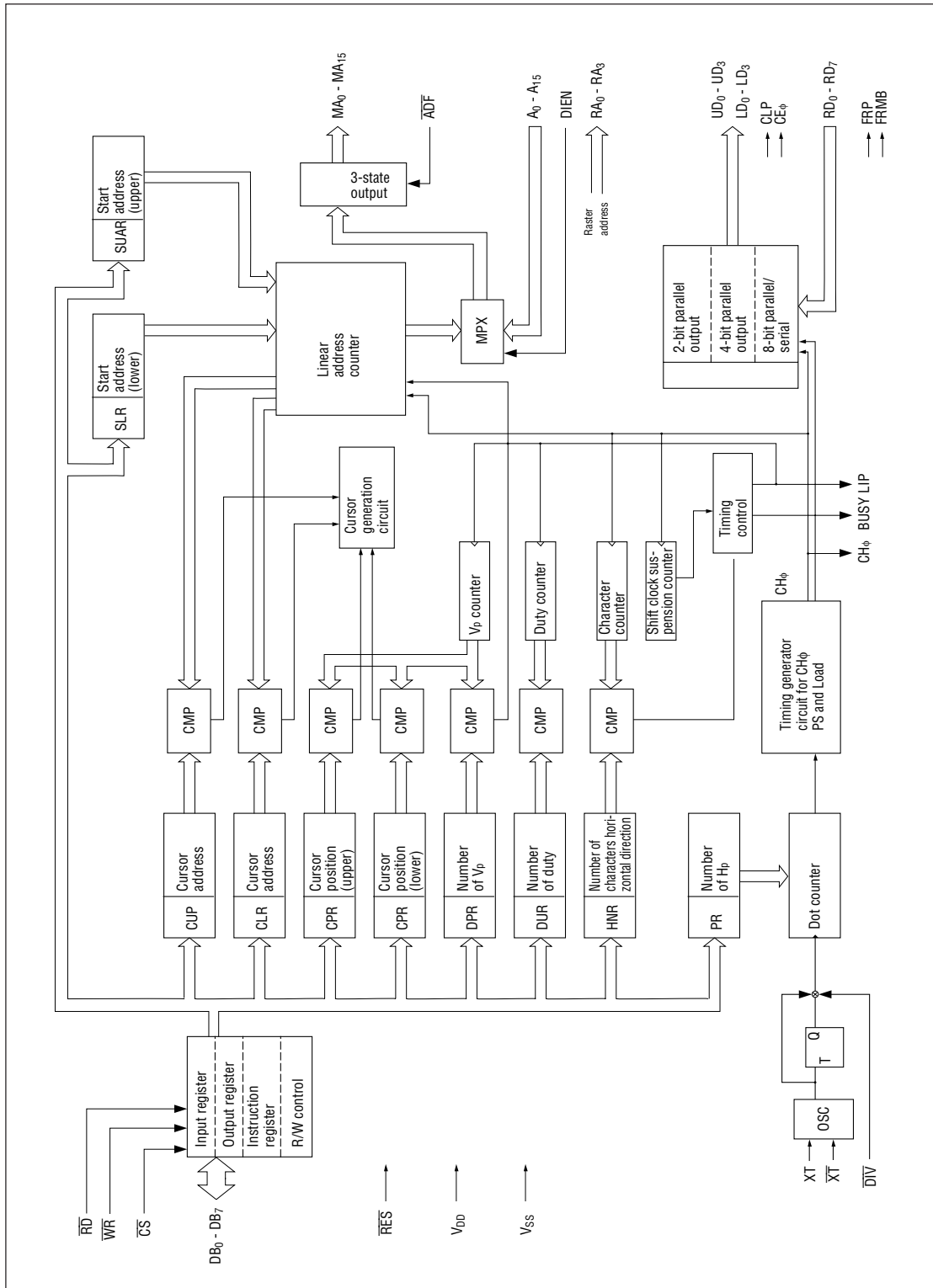
DOT MATRIX LCD CONTROLLER

GENERAL DESCRIPTION

The MSM6255 is a CMOS si-gate LSI designed to display characters and graphics on a DOT MATRIX LCD panel.
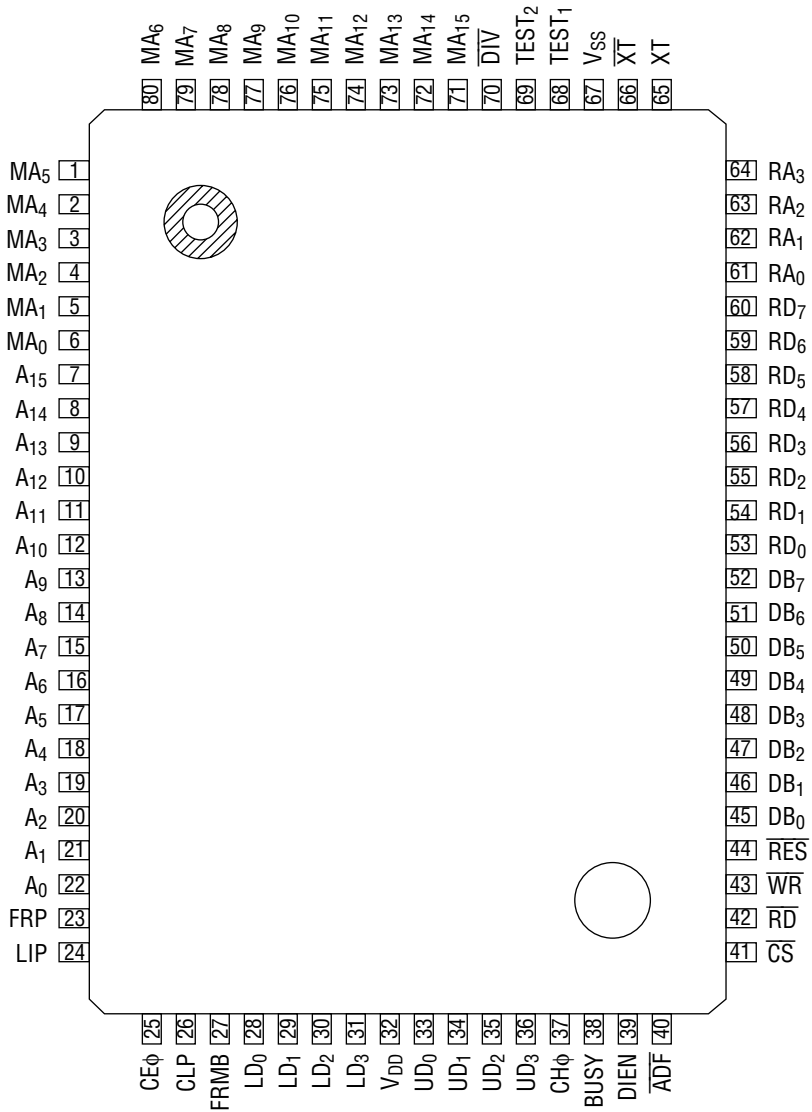
FEATURES

- Display control capacity
    - Graphic mode   : 512,000 dots (2^{16} bytes)
                                         Memory address MA_0 to MA_{15}
    - Character mode   : 65,536 characters (2^{16} bytes)
                                         Display address MA_0 to MA_{15}
- Direct interface with 8085 or Z80 CPU
- Duty   : 1/2 to 1/256 selectable
- Attributes
    - Screen clear
    - Cursor ON/OFF/blink
- Scrolling and paging
- Display system   : AC inversion at each frame
- Data output (upper and lower display outputs)
    4-bit parallel output, 2-bit parallel output, 1-bit serial output
- Crystal oscillation/external clock selectable
- Single +5V power supply
- Package options:
    80-pin plastic QFP (QFP80-P-1420-0.80-K)   (Product name: MSM6255GS-K)
    80-pin plastic QFP (QFP80-P-1420-0.80-BK) (Product name: MSM6255GS-BK)

BLOCK DIAGRAM

PIN CONFIGURATION (TOP VIEW)

Top pins (left to right): 80 MA$_6$, 79 MA$_7$, 78 MA$_8$, 77 MA$_9$, 76 MA$_{10}$, 75 MA$_{11}$, 74 MA$_{12}$, 73 MA$_{13}$, 72 MA$_{14}$, 71 MA$_{15}$, 70 $\overline{\text{DIV}}$, 69 TEST$_2$, 68 TEST$_1$, 67 V$_{SS}$, 66 $\overline{\text{XT}}$, 65 XT

Left pins (top to bottom):

MA$_5$	1
MA$_4$	2
MA$_3$	3
MA$_2$	4
MA$_1$	5
MA$_0$	6
A$_{15}$	7
A$_{14}$	8
A$_{13}$	9
A$_{12}$	10
A$_{11}$	11
A$_{10}$	12
A$_9$	13
A$_8$	14
A$_7$	15
A$_6$	16
A$_5$	17
A$_4$	18
A$_3$	19
A$_2$	20
A$_1$	21
A$_0$	22
FRP	23
LIP	24

Right pins (top to bottom):

64	RA$_3$
63	RA$_2$
62	RA$_1$
61	RA$_0$
60	RD$_7$
59	RD$_6$
58	RD$_5$
57	RD$_4$
56	RD$_3$
55	RD$_2$
54	RD$_1$
53	RD$_0$
52	DB$_7$
51	DB$_6$
50	DB$_5$
49	DB$_4$
48	DB$_3$
47	DB$_2$
46	DB$_1$
45	DB$_0$
44	$\overline{\text{RES}}$
43	$\overline{\text{WR}}$
42	$\overline{\text{RD}}$
41	$\overline{\text{CS}}$

Bottom pins (left to right): 25 CEϕ, 26 CLP, 27 FRMB, 28 LD$_0$, 29 LD$_1$, 30 LD$_2$, 31 LD$_3$, 32 V$_{DD}$, 33 UD$_0$, 34 UD$_1$, 35 UD$_2$, 36 UD$_3$, 37 CHϕ, 38 BUSY, 39 DIEN, 40 $\overline{\text{ADF}}$

80-Pin Plastic QFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1 - 6 71 - 80	MA_0 MA_{15}	O	Address output for displaying RAM. MA_0 - MA_{15} are high impedance when $\overline{ADF}$ = "L".
7 22	A_0 A_{15}	I	Memory address input pins
23	FRP	O	Frame signal. Synchronization of display
24	LIP	O	Display data latch signal
25	CE_ϕ	O	Chip enable clock for LCD segment driver
26	CLP	O	Display data shift clock
27	FRMB	O	Alternate signal output pin
28 31	LD_0 LD_3	O	Display data parallel output for lower side
32	V_{DD}	O	Supply voltage
33 36	UD_0 UD_3	O	Display data parallel output, Upper display 4-bit output (OD1, ED1, OD2 and ED2 outputs)
37	CH_ϕ	O	Character clock
38	Busy	O	Ready state signal. This signal is used while serial transmission stops.
39	DIEN	I	Display enable signal. When this signal is "H", display is enabled.
40	$\overline{ADF}$	I	Address floating input. When this signal is "L", MA_0 - MA_{15}, RA_0 - RA_3 are high impedance, and when it is "H", A_0 - A_{15} or a refresh address is output to MA_0 - MA_{15}.
41	$\overline{CS}$	I	Chip select. $\overline{CS}$ = "L"
42	$\overline{RD}$	I	Read. Reading data is valid when $\overline{RD}$ = "L"
43	$\overline{WR}$	I	Write. Data is written when $\overline{WR}$ = "H"
44	$\overline{RES}$	I	Reset. Resets each counter.
45 52	DB_0 DB_7	I/O	8-bit data bus. Common pins for 3-state I/O.
53 60	RD_0 RD_7	I	ROM/RAM data input. Dot pattern data for the character generator
61 64	RA_0 RA_3	O	Raster address output. *This output is not used in the graphic mode. RA_0 - RA_3 are high impedance when $\overline{ADF}$ = "L".
65 66	XT $\overline{XT}$	I O	X'tal osc. When an external clock is used by setting $\overline{DIV}$ to "H", feeds it to XT.
67	V_{SS}	—	Ground pin.
70	$\overline{DIV}$	I	"H" : EXT clock "L" : Self oscillation

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +6	V
Input Voltage	V_I	Ta = 25°C	−0.3 to V_{DD}	V
Storage Temperature	T_{STG}	—	−50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	V_{SS} = 0V	4.5 to 5.5	V
Operating Temperature	T_{op}	—	−20 to +85	°C
Operating Frequency	f_{osc}	V_{DD} = 5V ±10%	0 to 11	MHz

ELECTRICAL CHARACTERISTICS

Input Characteristics

(V_{DD} = 5V ± 5%, Ta = −20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input Voltage	V_{IH}	2.4	—	—	V	DB_0 - DB_7, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A_0 - A_{15},
"L" Input Voltage	V_{IL}	—	—	0.7	V	DIEN, ADF, RD0 - RD7
"H" Input Voltage	V_{IH}	4.5	—	—	V	$\overline{RES}$, $\overline{DIV}$, XT
"L" Input Voltage	V_{IL}	—	—	1.0	V	
"H" Input Current	I_{IH}	—	—	1	μA	DB_0 - DB_7, $\overline{CS}$, $\overline{RD}$, $\overline{WA}$, A_0 - A_{15},
"L" Input Current	I_{IL}	—	—	−1	μA	DIEN, $\overline{ADF}$, RD_0 - RD_7, $\overline{RES}$, $\overline{DIV}$
"H" Input Current	I_{IH}	25	—	100	μA	TEST1, TEST2
"L" Input Current	I_{IL}	—	—	−1	μA	

Output Characteristics

(V_{DD} = 5V ± 5%, Ta = −20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Output Current	I_{OH}	V_{OH} = 2.8V	−500	—	—	μA	LD_0 - LD_3 UD_0 - UD_3 MA_0 - MA_{15} RA_0 - RA_3
"L" Output Current	I_{OL}	V_{OL} = 0.4V	2.4	—	—	mA	CH_ϕ, CE_ϕ, LIP, FRP FRMB, BUSY, CLP DB_0 - DB_7

Supply Current

(V$_{DD}$ = 5V ± 5%, Ta = −20 to +85°C)

Parameter	Symbol	V$_{DD}$	Condition	Min.	Typ.	Max.	Unit
Static Current	I$_{DDS}$	5	f$_{osc}$ = 0 Hz, no load	—	—	50	μA
Dynamic Current	I$_{DD}$	5	f$_{osc}$ = 10 MHz, no load	—	—	15	mA

Note: TEST 1 and TEST2 are open, and other inputs are either V$_{DD}$ or GND.

Switching Characteristics
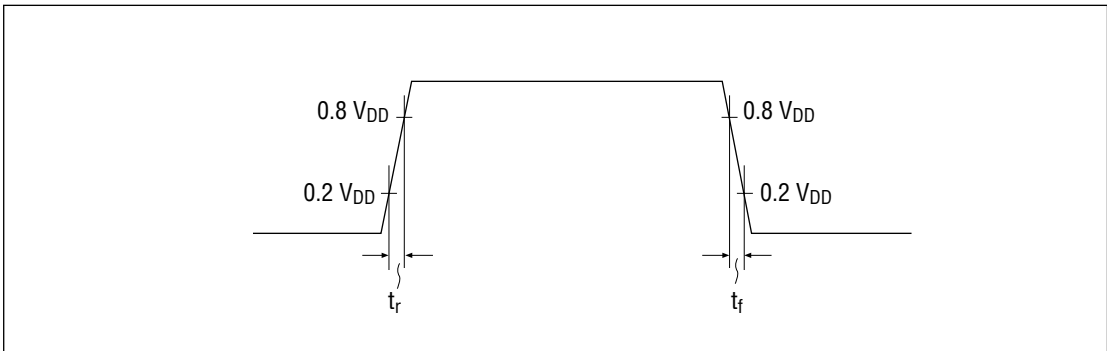
(V$_{DD}$ = 5V ± 5%, Ta = −20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Rise Time	t$_r$	C$_L$ = 60 pF	—	—	100	ns	All output pins
Fall Time	t$_f$	C$_L$ = 60 pF	—	—	100	ns	

Operating Frequency

(V$_{DD}$ = 5V ± 5%, Ta = −20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
Oscillating Frequency	f$_{osc}$	$\overline{DIV}$ = "L"	—	—	11	MHz	Crystal oscillator
Basic Clock Frequency	f$_s$	$\overline{DIV}$ = "H"	—	—	5.5	MHz	External clock

TIMING DIAGRAM

LCDC Control Signal Timing Characteristics

(C_L = 30pF, V_{DD} = 5V ± 5%, Ta = −20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	t_{CP}	180	—	—	ns
Clock "H" Level Pulse Width	P_{WH}	80	—	—	ns
Clock "L" Level Pulse Width	P_{WL}	80	—	—	ns
Clock Rise/Fall Time	t_{cr}/t_{cf}	—	—	20	ns
Character Clock Delay Time	t_{CH}	—	—	200	ns
Memory Address Clock Delay Time	t_{MA}	—	—	100	ns
Memory Address Disable Delay Time	t_{AD1}	—	—	40	ns
Memory Address Enable Delay Time	t_{AD2}	—	—	40	ns
CPU Address Delay Time	t_{AD3}	—	—	100	ns
Refresh Address Delay Time	t_{AD4}	—	—	100	ns
Reset "H" Level Pulse Width	t_{RES}	1	—	—	µs
CPU Address Delay Time	t_{AD5}	—	—	100	ns
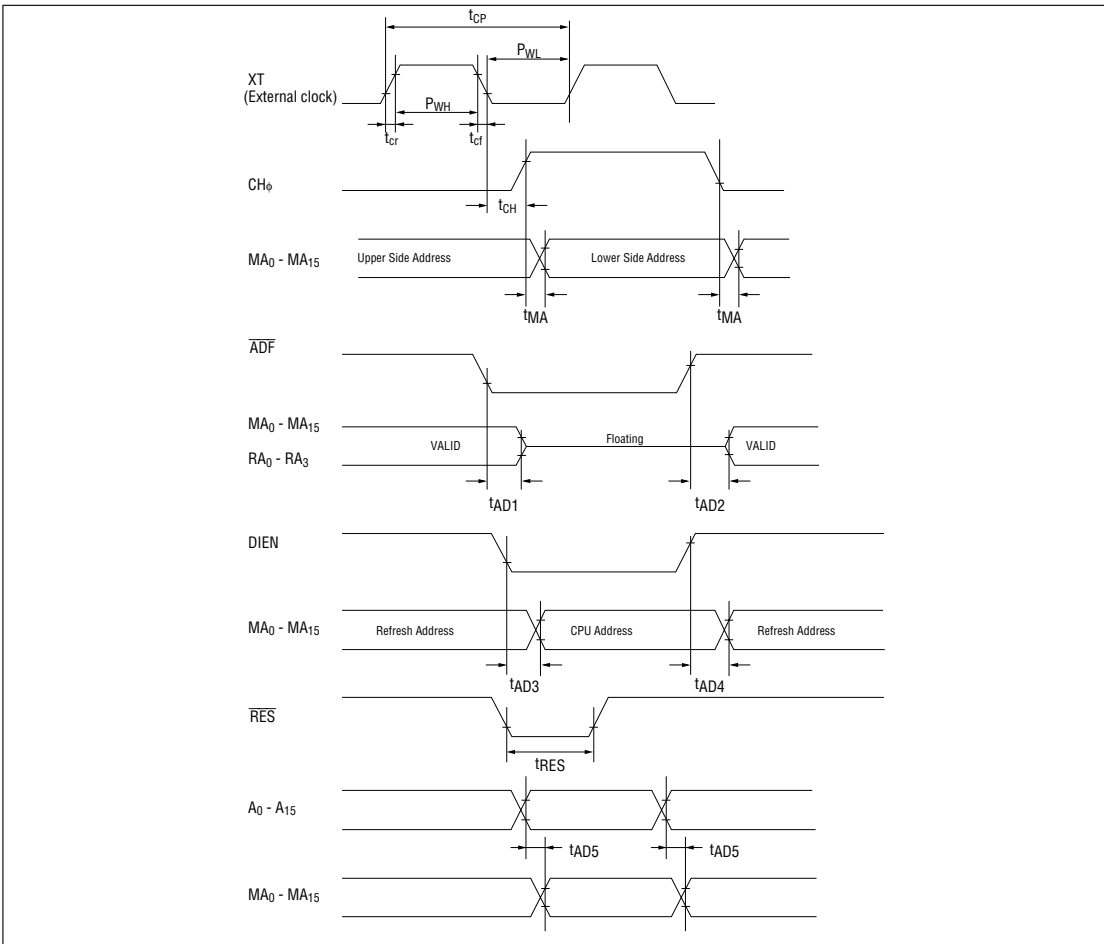
Bus Timing Characteristics

(C_L = 50pF, V_DD = 5V ± 5%, Ta = −20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
A_0, $\overline{CS}$ Setup Time	t_{CS}	30	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width	t_{CW}	200	—	—	ns
Address Hold Time	t_{AH}	10	—	—	ns
Data Setup Time	t_{DS}	60	—	—	ns
Data Hold Time	t_{DH}	20	—	—	ns
Output Disable Time	t_{OH}	0	—	40	ns
Access Time	t_{ACC}	—	—	200	ns
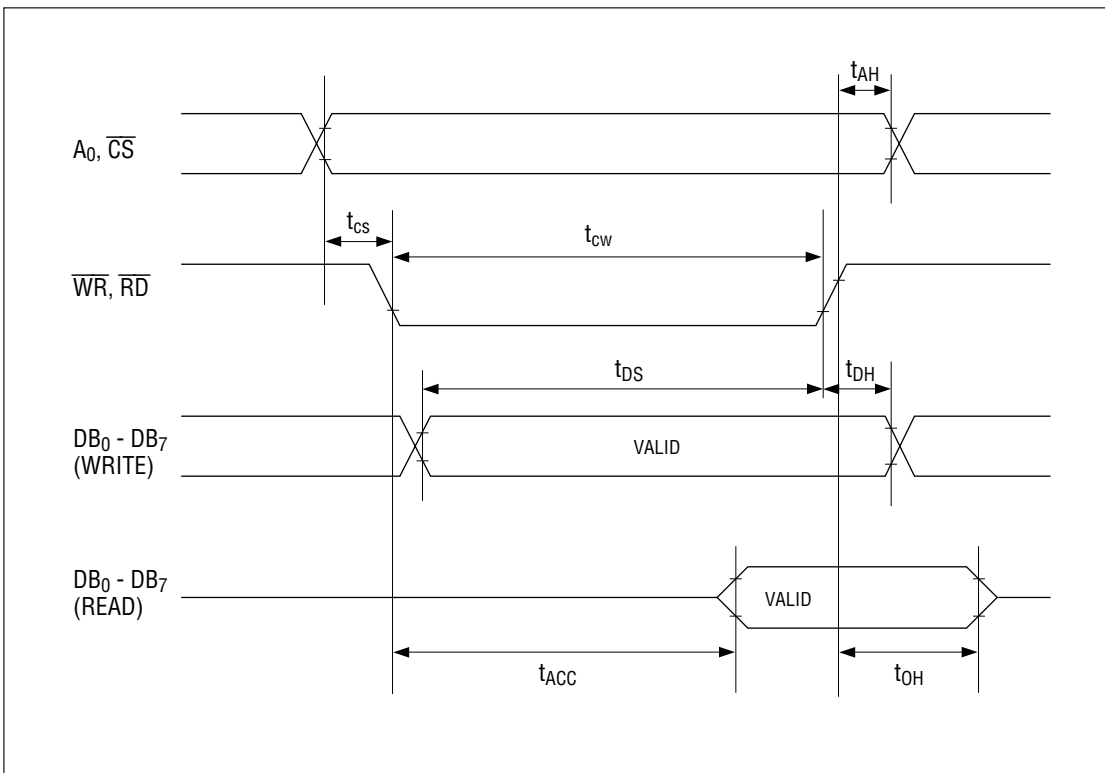
LCDC Driver Interface Timing Characteristics

$(C_L = 30pF, V_{DD} = 5V \pm 5\%, Ta = -20 \text{ to } +85°C)$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Data Delay Time	t_{DA}	—	—	100	ns
1 Character Cycle Time	$t_{CH\phi}$	730	—	—	ns
Latch Signal Delay Time	t_ℓ	—	—	200	ns
Latch Signal "H" Time	t_{LIP}	1.46	—	—	µs
Chip Enable Clock Delay Time	t_{CE}	—	—	200	ns
Chip Enable Clock "H" Time	$t_{CE\phi}$	730	—	—	ns
Ready Signal Delay Time	t_B	—	—	200	ns
Ready Signal "H" Time	t_{BUSY}	5.11	—	—	µs
Frame Signal Delay Time	t_{FRP}	$2t_{CH\phi}$	—	$2t_{CH\phi} +200$	ns
Alternating Frame Signal Delay Time	t_{FR}	—	—	200	ns
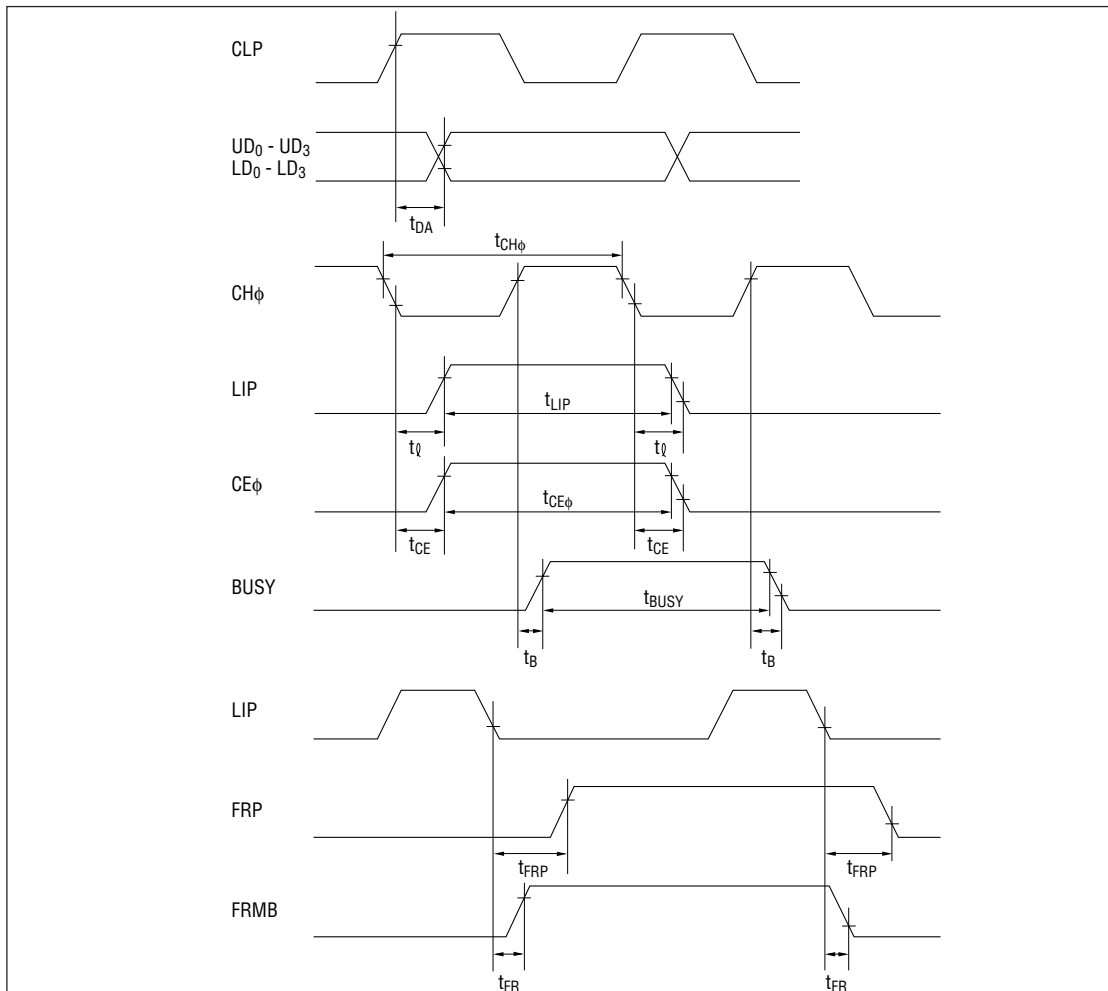
Timing for Fetching Pattern Data

$(V_{DD} = 5V \pm 5\%, Ta = -20 \text{ to } +85°C)$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Upper Side Data Setup Time	t_{UDS}	120	—	—	ns
Upper Side Data Hold Time	t_{UDH}	0	—	—	ns
Lower Side Data Setup Time	t_{LDS}	120	—	—	ns
Lower Side Data Hold Time	t_{LDH}	0	—	—	ns
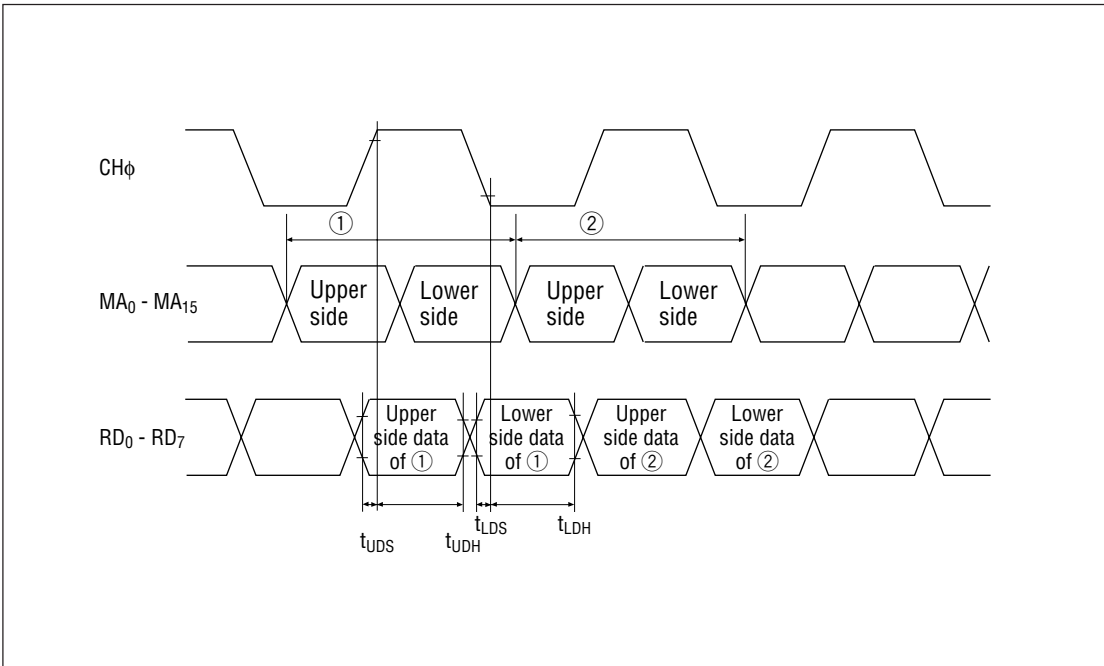
FUNCTIONAL DESCRIPTION

LCDC Internal Registers

The internal registers include one instruction register (IR) and nine data registers. (See Table 1.)

Table 1   MSM6255 Internal Registers

$\overline{CS}$	A_0	Instruction register 3 2 1 0	Register	Register name	READ	WRITE	Data bit 7	6	5	4	3	2	1	0
H	X	X X X X	–	Invalid	–	–								
L	H	X X X X	IR	Instruction register	○	○	X	X	X	X				
L	L	L L L L	MOR	Mode control register	X	○	X							
L	L	L L L H	PR	Character pitch register	○	○					X			
L	L	L L H L	HNR	Horizontal character number register	○	○	X							
L	L	L L H H	DVR	Duty number register	X	○								
L	L	L H L L	CPR	Cursor form register	○	○								
L	L	L H L H	SLR	Start address (lower) register	○	○								
L	L	L H H L	SUR	Start address (upper) register	○	○								
L	L	L H H H	CLR	Cursor address (lower) register	○	○								
L	L	H L L L	CUR	Cursor address (upper) register	○	○								

Note: "L" is read if the data of the registers marked X is read.

– Instruction register
The instruction register is a register for specifying the address of the data register which is accessed.
This register is cleared when $\overline{RES}$ input is "L".

– Mode control register

The mode control register is specified by writing "00_H" in the instruction register.

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	L	L	L
Mode control register	L	L	MODE DATA						

D_6	D_5	D_4	D_3	D_2	D_1	D_0	Output mode	
H/L	H/L	H/L	H/L	L	L	L	1-bit serial	Character display
				H	L		2-bit parallel	
				X	H		4-bit parallel	
				X	H			
				L	L	H	1-bit serial	Graphics
				H	L		2-bit parallel	
				X	H		4-bit parallel	
				X	H			

Column labels (bottom, by bit):
- D_6: Blink time
- D_5: Cursor ON/OFF
- D_4: Cursor blink
- D_3: Display ON/OFF
- D_2: 2-bit parallel
- D_1: 4-bit parallel/1-bit serial

D_3 (Display ON/OFF):
H: Display ON
L: Display OFF

D_5, D_4 (Cursor):

D_5	D_4	
L	L	Cursor OFF
L	H	Cursor OFF
H	L	Cursor ON
H	H	Cursor blink

D_6 (Blink time):
H: 16 frames ⎫
L: 32 frames ⎬ Half of blinking cycle
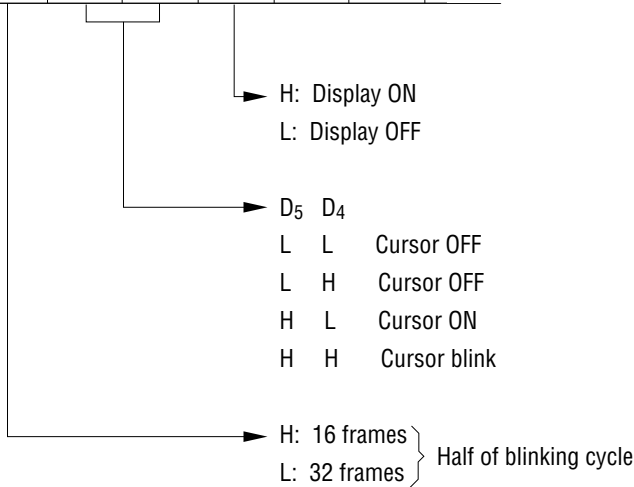
– Character pitch register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	L	L	H
Character pitch register	L		$(V_p - 1)$			L		$(H_p - 1)$	

H_p represents the number of bits to be displayed among one byte display data sent from RAM. The value of H_p is the following five types.

H_p	D_2	D_1	D_0
4	L	H	H
5	H	L	L
6	H	L	H
7	H	H	L
8	H	H	H

– Horizontal character number register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	L	H	L
Character number register	L	L				$(H_N - 1)$			

Assuming that the total horizontal dot number of the display is n_H,

$$n_H = H_p \times H_N, \quad \text{where } H_N = 2 \text{ to } 128.$$

The maximum value of $n_H = 8 \times 128 = 128$ bytes = 1,024 dots.

– Duty number register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	L	H	H
Time division register	L				$(N_x - 1)$				

$N_x = 2$ to 256

– Cursor form register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	H	L	L
Cursor position register	L		$(C_{pu} - 1)$				$(C_{pd} - 1)$		

The cursor is displayed on the lines from C_{pu} to C_{pd} in the character display mode. The length of the cursor in the horizontal direction is equal to the character pitch in the horizontal direction, H_p. The cursor is not displayed in graphic mode. The relation between the cursor and V_p is as follows.

Font configuration of $H_p = 7$ and $V_p = 8$

$C_{pu} = 8, C_{pd} = 8$ $C_{pu} = 7, C_{pd} = 8$ $C_{pu} = 2, C_{pd} = 6$
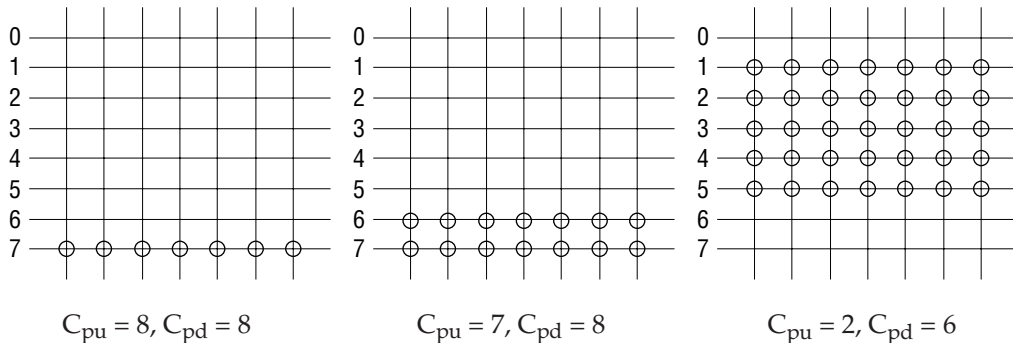
Notes: (1) Setting of C_{pu}, $C_{pd} > V_p$ is not available.
      (2) The cursor signal and pattern data are displayed subject to EX-OR.

– Start address (lower) register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	H	L	H
Display start address register (lower byte)	L	Start address (lower)							

– Start address (upper) register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	H	H	L
Display start address register (upper byte)	L	Start address (upper)							

The display start address shows an address of the RAM which stores data displayed at the left end and the most upper position. The start address is composed of upper and lower 8 bits (16 bits in total).

– Cursor address (lower) register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	H	H	H
Cursor address register (lower byte)	L	Cursor address (lower)							

– Cursor address (upper) register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	H	L	L	L
Cursor address register (upper byte)	L	Cursor address (upper)							

By this instruction, the value of the cursor address is written in the cursor address register. The cursor is displayed at the position specified by the cursor address register.
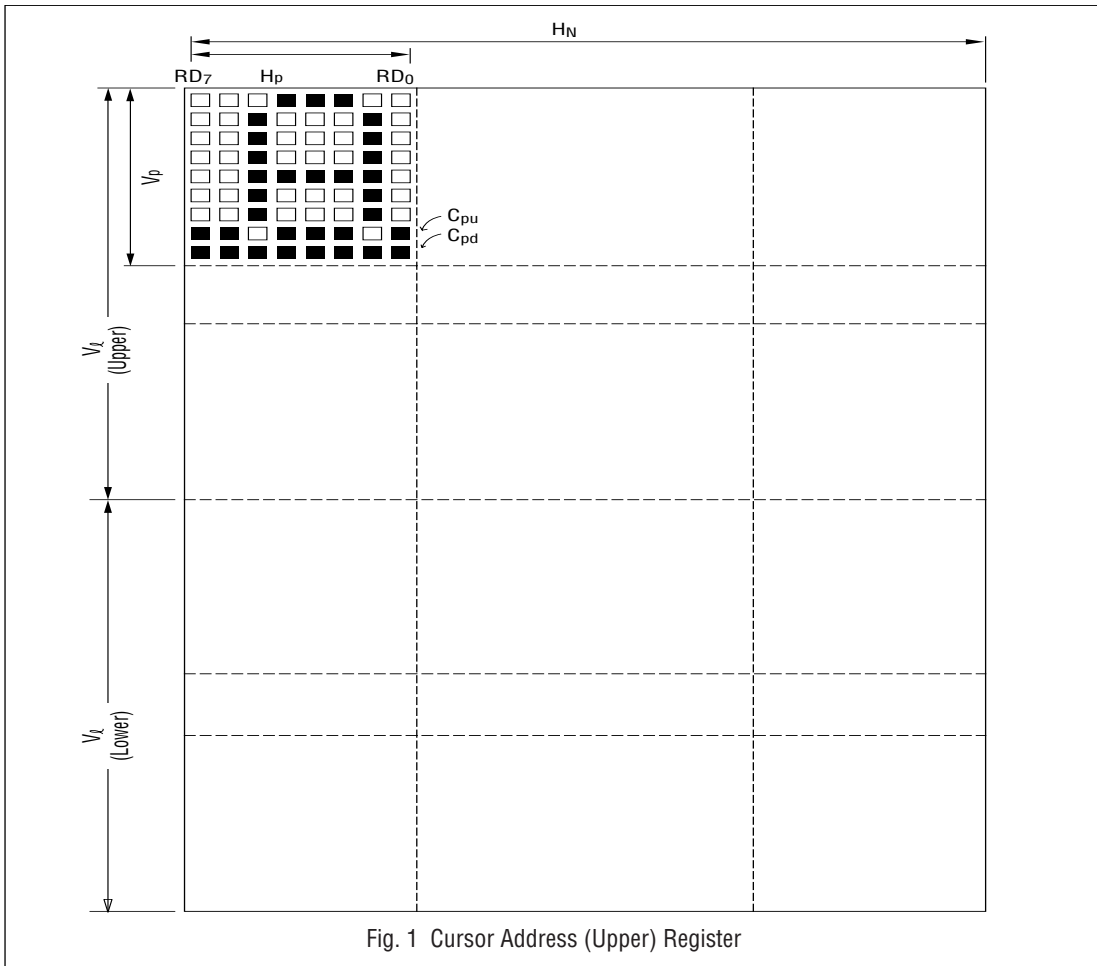
Fig. 1 Cursor Address (Upper) Register

Table 2 Legend

Symbol	Name	Meaning	Value
H_p	Horizontal pitch	Pitch of characters in horizontal direction	4 - 8 dots
V_p	Vertical pitch	Pitch of characters in vertical direction	1 - 16 dots
H_N	Number of characters in one line	Number of characters per line or number of words per line	2 - 128 characters
V_ℓ	Number of rows	Display duty	2 - 256
C_{pu}	Cursor start position	A position where the cursor starts display	Line 1 - 16
C_{pd}	Cursor end position	A position where the cursor stops display	Line 1 - 16

- Built-in Bus Averter
  The bus averter which switches the address buses A_0 - A_{15} of the CPU with the memory address buses of the refresh. The refresh memory addresses are output to MA_0 - MA_{15} when the DIEN pin is set at high level and A_0 - A_{15} are output to MA_0 - MA_{15} when the DIEN pin is set at low level.

- External Clock Operation
  An external clock enables the MSM6255 to operate when the $\overline{DIV}$ pin is set at high level. Input the external clock to XT.(Leave $\overline{XT}$ open.)
  When the $\overline{DIV}$ pin is set at low level, the IC enters the crystal oscillation mode.

- Address Output Floating
  MA_0 - MA_{15} and RA_0 - RA_3 become high impedance when the $\overline{ADF}$ pin is set at low level.
  MA_0 - MA_{15} and RA_0 - RA_3 become normal impedance when the ADF pin is set at high level.

- Power Down Function
  The chip select function becomes enabled for the segment driver by connecting the CE_ϕ pin to the ECLK input of the MSM5279. The power down function is valid only in 4-bit parallel output mode.

- Refresh Memory Address (MA_0 - MA_{15}) Operation
  In the horizontal direction, MA_{xx} is counted up at the falling edge of CH_ϕ. Upper side is addressed while CH_ϕ is set at low level and lower side is addressed while CH_ϕ is set at high level.
  MA_{xx} is counted up even if it exceeds the number of horizontal display characters, but this does not affect the display since no data is being transferred at the time.
  The period in which the data transfer is suspended corresponds to eight characters. When the period passes, one horizontal cycle is completed and the next cycle is commenced.
  Memory address operation in the graphic mode is shown in Fig. 2 and that in the character mode is shown in Fig. 3.

Address configuration of display RAM

MSB															LSB
MA_{15}	MA_{14}	MA_{13}	MA_{12}	MA_{11}	MA_{10}	MA_9	MA_8	MA_7	MA_6	MA_5	MA_4	MA_3	MA_2	MA_1	MA_0

Fig. 2   Memory Address in Graphic Mode (640 x 200)
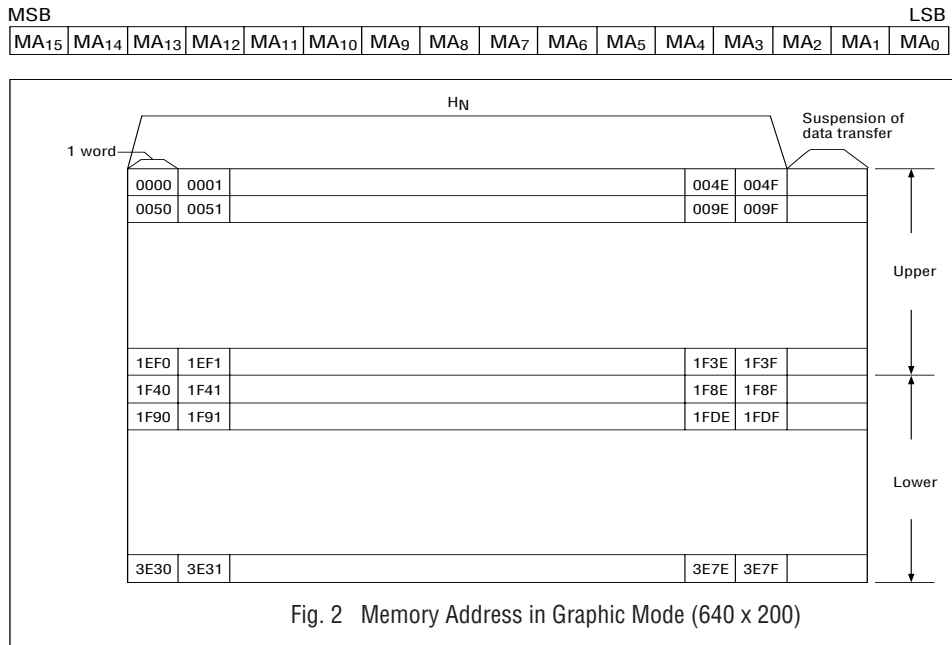
Note: "L" is output for RA_0 - RA_3.

H$_N$ (Number of characters in horizontal display line)

Suspension of data transfer

Raster address	1 character					
000	0000	0001	⟶	004E	004F	
001	0000	0001	⟶	004E	004F	
010						
011						
100						
101						
110						
111	0000	0001	⟶	004E	004F	
000	0050	0051	⟶	009E	009F	
111	0050	0051	⟶	009E	009F	
000	0370	0371	⟶	03BE	03BF	
111	0370	0371	⟶	03BE	03BF	
000	03C0	03C1	⟶	040E	040F	
111	03C0	03C1	⟶	040E	040F	
000	0730	0731	⟶	077E	077F	
111	0730	0731	⟶	077E	077F	

Line 1, Line 2, Line 12, Line 13, Line 24

Upper / Lower

Note : Start address is 0000, 80 characters x 24 lines and V$_P$ = 8

Fig. 3 Memory Address in Character Mode (80 characters x 24 lines)

– Output Mode

Three kinds of modes, 1-bit serial, 2-bit parallel and 4-bit parallel, are available as output modes. Data flows of each mode are shown below.

Fig. 4 1-Bit Serial Data Transfer

Fig. 5 2-Bit Parallel Data Transfer

Fig. 6   4-bit Parallel Data Transfer
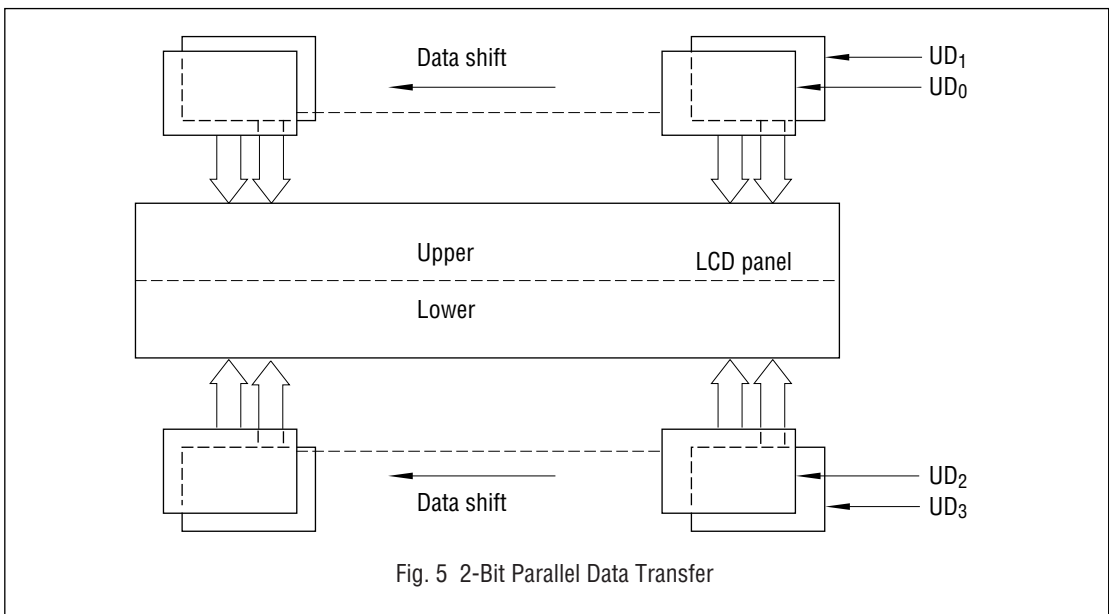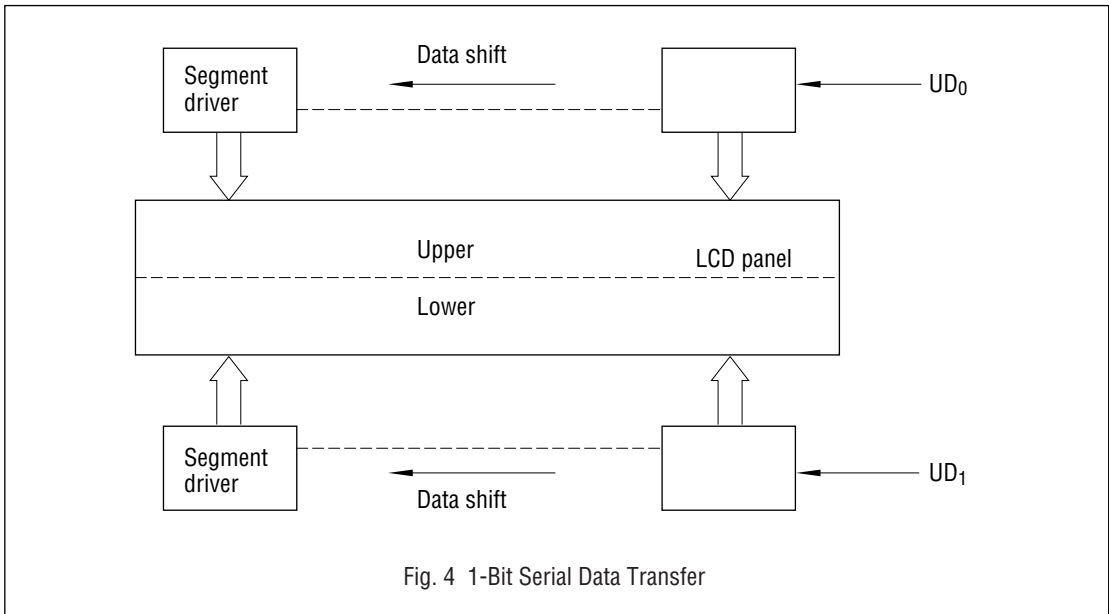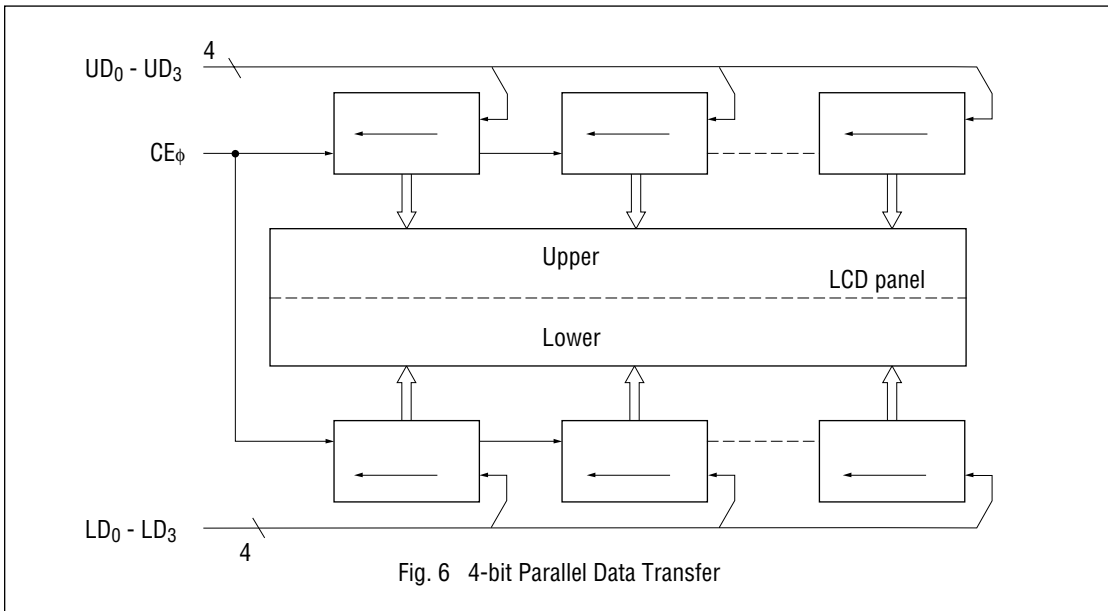
Time charts corresponding to data transfers shown in Fig. 4 - Fig. 6 are shown in Fig. 7 - Fig. 9. fs, the dot clock, shown in Figs.7-9, is a signal inside the IC. For more information see "Relation between Reference Clock (fs) and External Clock" on page 601.
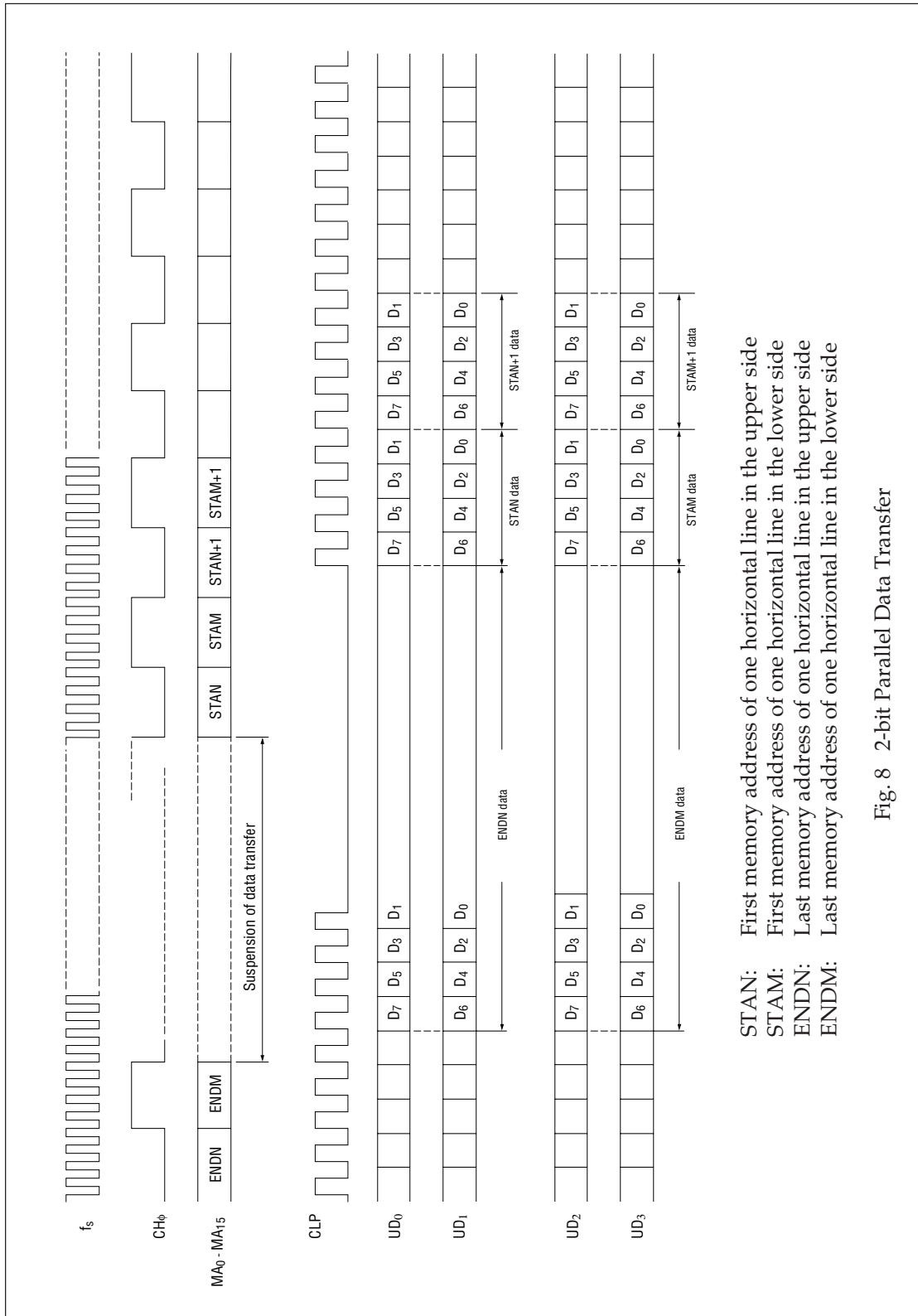
STAN: First memory address of one horizontal line in the upper side
STAM: First memory address of one horizontal line in the lower side
ENDN: Last memory address of one horizontal line in the upper side
ENDM: Last memory address of one horizontal line in the lower side

Fig. 7 1-bit Serial Data Transfer

Fig. 8 2-bit Parallel Data Transfer

STAN: First memory address of one horizontal line in the upper side
STAM: First memory address of one horizontal line in the lower side
ENDN: Last memory address of one horizontal line in the upper side
ENDM: Last memory address of one horizontal line in the lower side
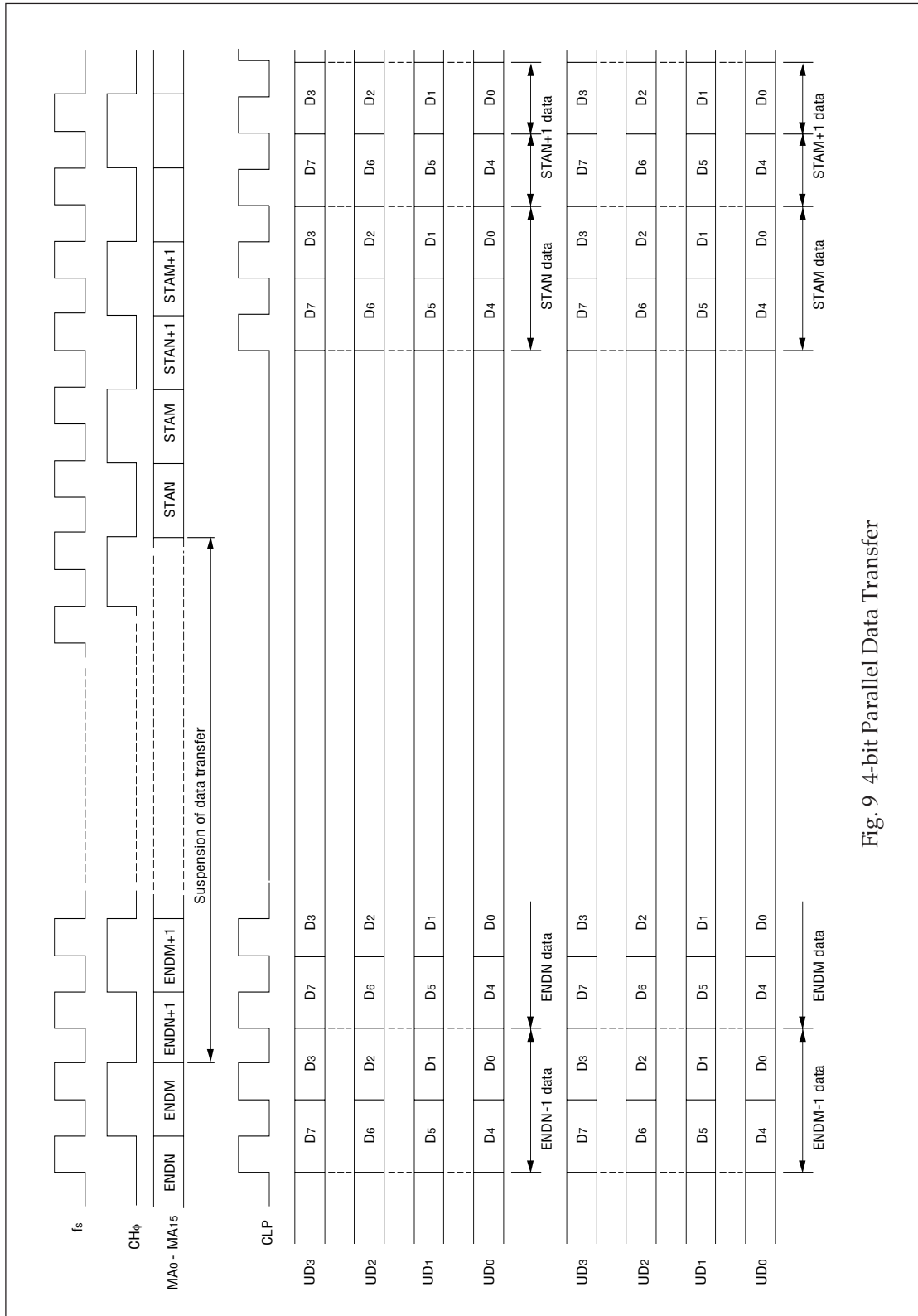
Fig. 9 4-bit Parallel Data Transfer

– Relation Between Duty and Number of Lines
Number of lines is determined by V_ℓ , number of lines in vertical direction(display duty).
Number of lines = V_ℓ x 2

Note: In the character display mode, number of lines should not be odd number.

– Calculation of Crystal Oscillation Frequency (f_{osc})

Table 3 Calculation Formula of f_{osc}

DIV	Output mode	Calculation formula of f_{osc}	Calculation exmaple (MHz)
L	①	FRP x (H_N + 8) x H_p x V_ℓ x 2	9.856
L	②	FRP x (H_N + 8) x V_ℓ x 4	2.464
H	①	FRP x (H_N + 8) x H_p x V_ℓ	4.928
H	②	FRP x (H_N + 8) x V_ℓ x 2	1.232

Note: (1) Table 3 shows a calculation example assuming that FRP = 70 Hz, H_N = 80, H_p = 8 and
V_ℓ = 100. However, the example of H_p = 4 to 7 in 4-bit parallel is not included.
(2) Output mode ① : H_p = 4 to 7 in 1-bit serial, 2-bit parallel and 4-bit parallel
Output mode ② : H_p = 8 in 4-bit parallel

– Calculation of Character Clock (CH_ϕ) Frequency

$$CH_\phi = FRP \text{ x } (H_N + 8) \text{ x } V_\ell$$

Example: Assuming FRP = 70 Hz, H_N = 80 and Vr= 100, CH_ϕ = 1.62 (μs)

– Calculation of Shift Clock (CLP) Frequency

Table 4 Calculation Formula of CLP

Output mode	Calculation formula of CLP	Calculation exmaple (MHz)
1-bit serial	RP x (H_N + 8) x H_p x V_ℓ	4.928
2-bit parallel	FRP x (H_N + 8) x H_p x V_ℓ x 1/2	2.464
4-bit parallel	FRP x (H_N + 8) x H_p x V_ℓ x 1/4	1.232

Note: Table 4 shows a calculation example assuming that FRP = 70 Hz, H_N = 80, H_p = 8 and
V_ℓ = 100.

– Relation Between Reference Clock (f_s) and External Clock
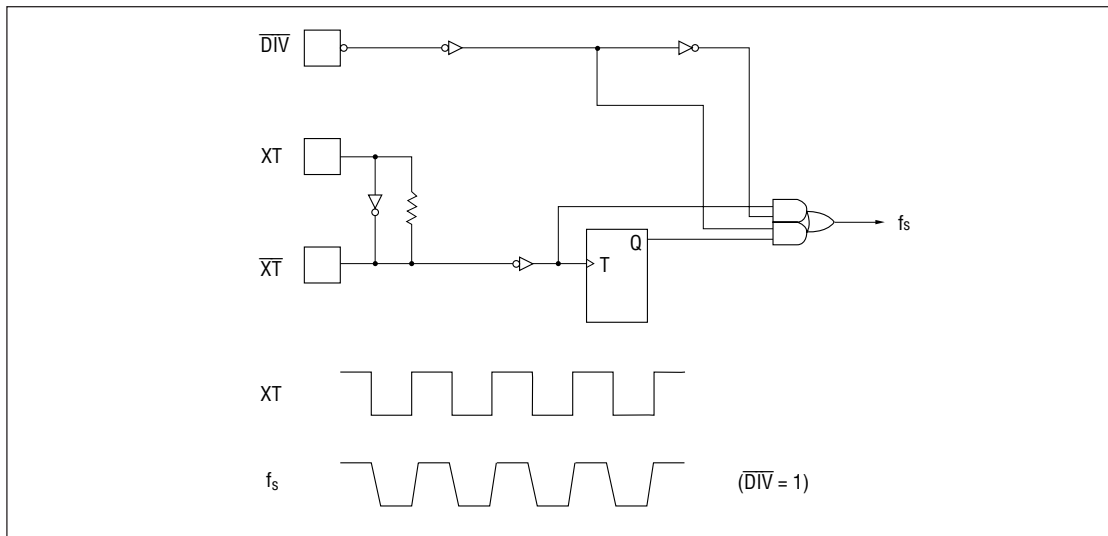
f_s functions as a dot clock in LCDC and the dot counter inside the IC is counted up at the trailing edge of f_s.

The dot counter operates as a N-ary counter on a basis of H_P and generates the character clocks (CH_ϕ).

(Refer to the time charts Fig. 7 - 9 and Fig. 14.)

– Access to the Display RAM

In writing/reading the data to/from the display RAM, DIEN should be low level. By setting DIEN signal at low level, the address from the CPU are output from MA0 - MA15, and this enables the access to the display RAM.

There are three methods of accessing display RAM from the CPU.

(1) Direct access from CPU

Display RAM is accessed directly from the CPU, irrespective of the condition of MSM6255 (refresh cycle or not).

In this method, the RAM address changes to the CPU address when the display is on the screen. So, frequent access to the RAM causes flickering on the screen.

(2) Access while BUSY signal is high

BUSY signal indicates the period when the data transfer stops, and BUSY signal is set high when the data transfer stops. The period when BUSY signal is high corresponds to that of seven characters'. If display RAM is accesed during this period (when BUSY is high), the display on the screen does not flicker.

Note: This method is effective when the size of screen is small. In the case of big size screen, 640 x 200 dots, 1character needs approx. 1.6ms. So, in this case, the period when BUSY is at high level is 11.2ms, which is impossible to write or read a lot of data.

(3) Synchronized access (only for operating the IC by external clock)

Refresh cycle and CPU cycle are alternately performed. So, there is not flickering on the screen and there is no need to sense the BUSY signal.

When using this method, however, some external circuitry is necessary. The timing chart of this method is described in the Figure 10 below.

Fig. 10   Basic Timing of Synchronized Access to Display RAM
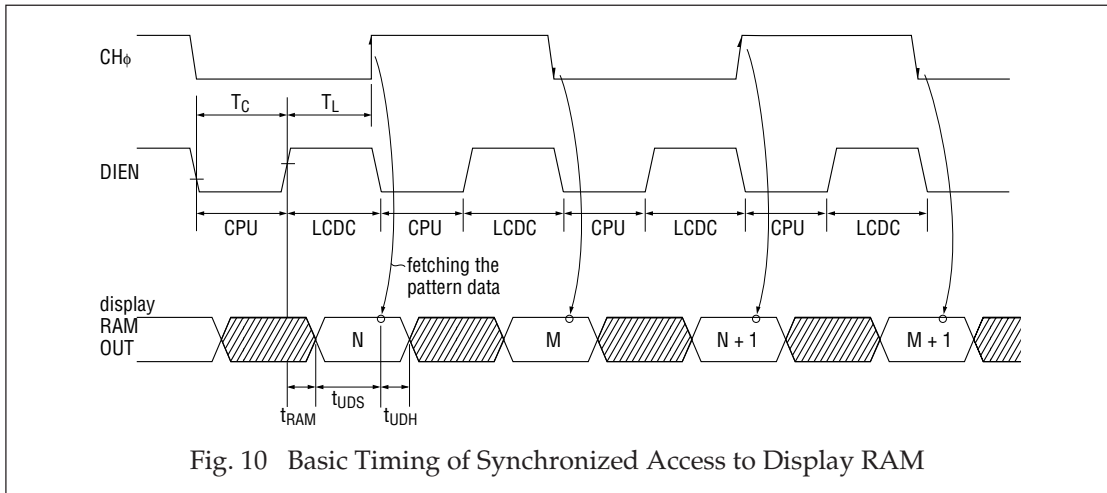
Legend

T_C : Period when the address bus is occupied by CPU
T_L : Period when the LCDC fetches the refreshed data
t_{RAM} : Refresh address delay time + memory access time
t_{UDS} : Upper side data set-up time
t_{UDH} : Upper side data hold time

When DIEN is high, MA_0 - MA_{15} output address to the upper side when CH_ϕ is low and to the lower side when CH_ϕ is high.
To perform synchronized access method, the timing between DIEN and CH_ϕ should be as described in Figure 10.

Fig. 11   Wait Function Controlling Circuit
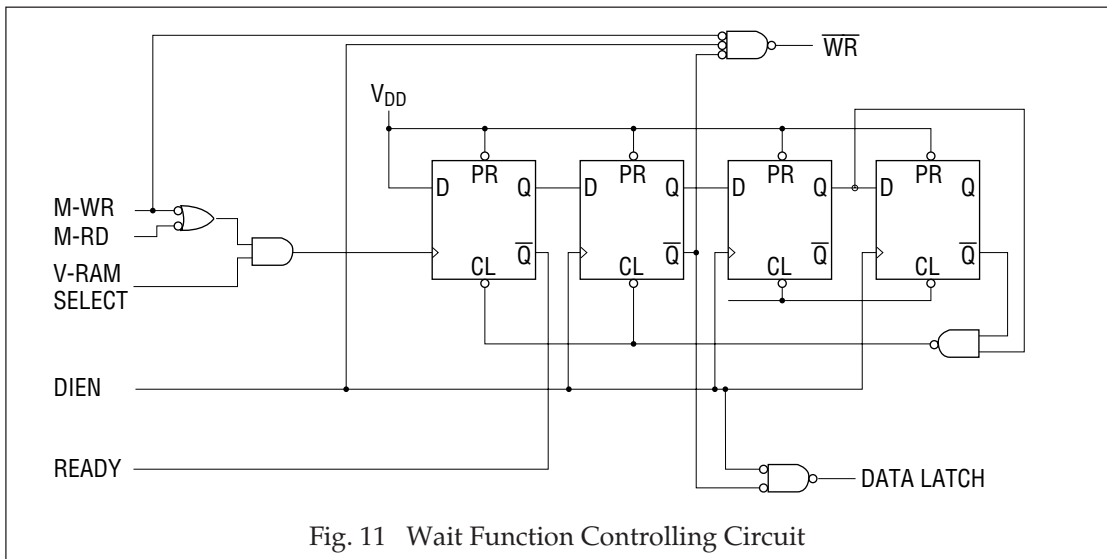
Display RAM must meet the following condition:

$$T_L > t_{RAM} + t_{UDS}$$

In writing data into the display RAM, LCDC should be synchronized so that the write pulse occurs during the period of T_C. In reading the pattern data from the CPU, the data of display RAM should be latched first.
Figure 11 shows the controlling circuit.

– DIEN
DIEN has to be generated when the display RAM is accessed by Synchronized access method.

(1) When the LCD screen is not split into upper and lower ones

If, for example, an LCD panel with a total of 64 dots in vertical direction is displayed at 1/64 duty, either the upper side data or the lower side data becomes unnecessary, and then the CHϕ signal can be used as a DIEN signal.

(2) When the LCD screen is split into upper and lower ones

If 4-bit parallel output mode is set and H_P=8, the timing diagram of the dot clock and the character clock is as shown below.
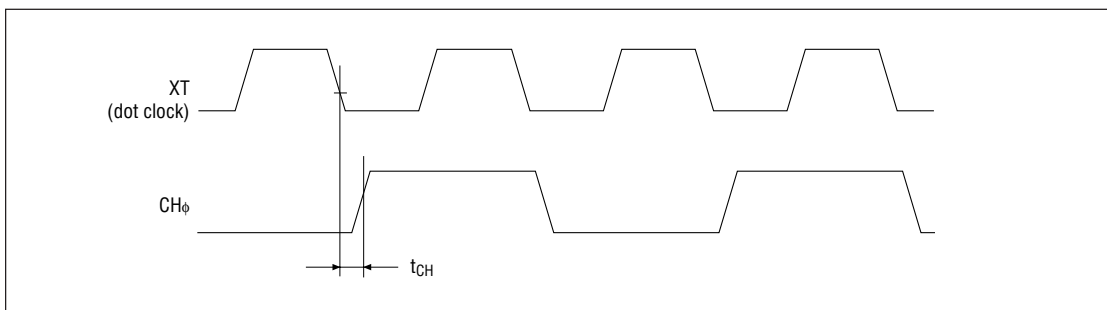
DIEN signal is generated by XT and CH$_\phi$.
DIEN signal generating circuit is shown below.
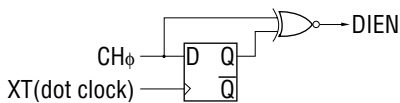
When $H_p \pi 8$ in the 1-bit serial, 2-bit parallel and 4-bit parallel mode, the relation between XT and CH$_\phi$ should be referred to Figures 7 and 8.

– Scroll◊Paging
Scroll◊paging is enabled by setting the display start address to the scroll address register.

(1) Memory address of vertical scroll◊paging
Figure 2 shows the memory address when the start address is 0000. When the start address is set at 0050, the display will be vertically shifted by +1.
By setting the starting address one by one, the screen will scroll vertically.

paging will be performed by setting the start address as 3E80.

(2) Memory address of horizontal scroll
When the starting address is set at 0001 in Figure 2, the display on the screen will be shifted by +1 byte horizontally. The data shown as 004F in Figure 2 corresponds to the memory data in the 2nd line shown as 0050.

APPLICATION CIRCUITS

Interface With CPU

MSM6255

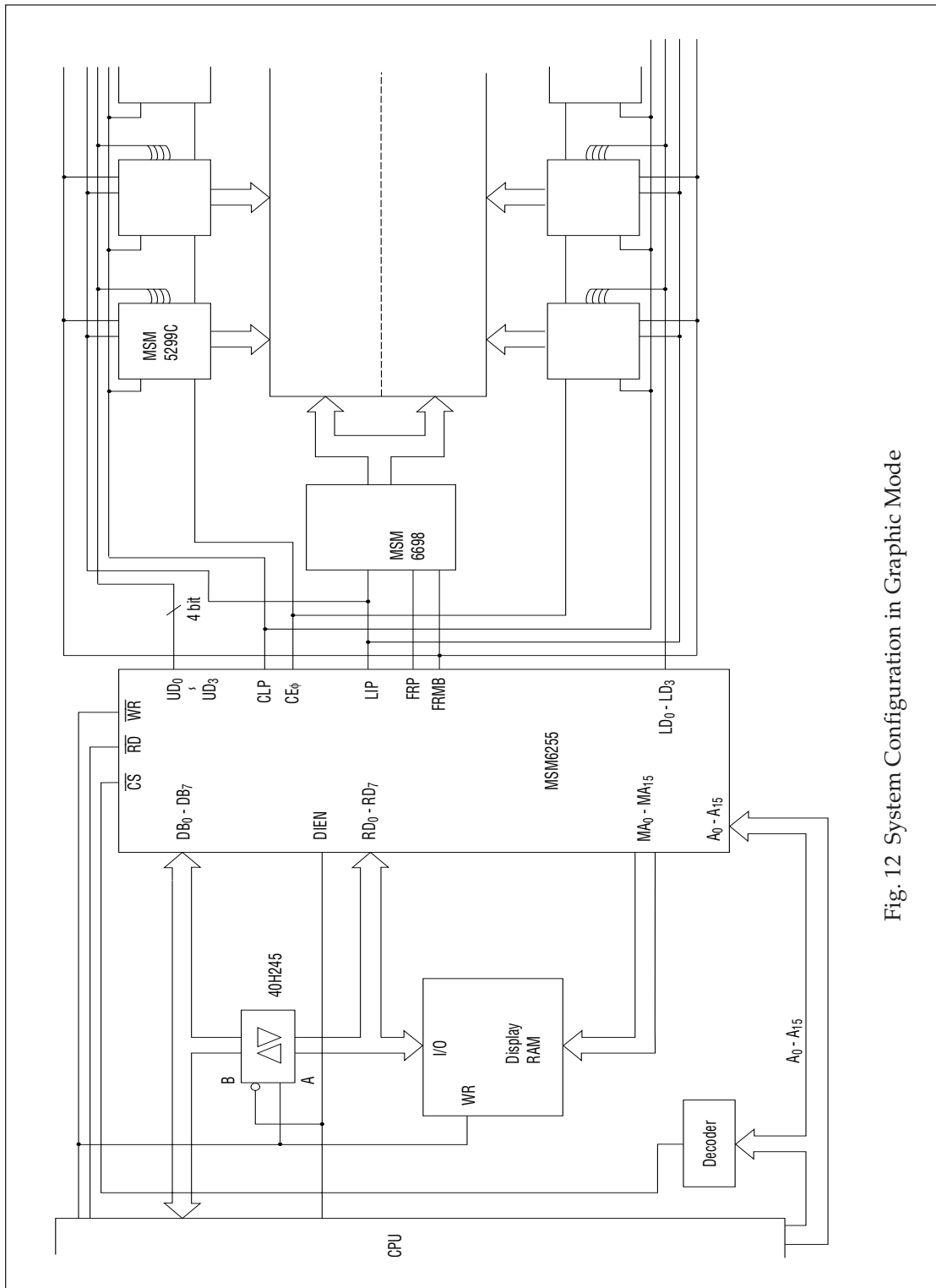8086

WR
RD

M/IO

A₁ - A₁₅   Decoder   CS

DT/R
DEN

AD₀ - AD₁₅   Trans-ceiver   D₀ - D₁₅   D₁ - D₇   DB₀ - DB₇
A₁₆ - A₁₉

Latch   A₀ - A₁₉   BHE   A₀ - A₁₅

BHE
ALE

*Minimum mode

MSM6255

6800

φ2   RD
VMA   WR
RD/WR

A₁ - A₁₅   Decoder   CS

D₀ - D₇   DB₀ - DB₇

A₀ - A₁₅   A₀ - A₁₅
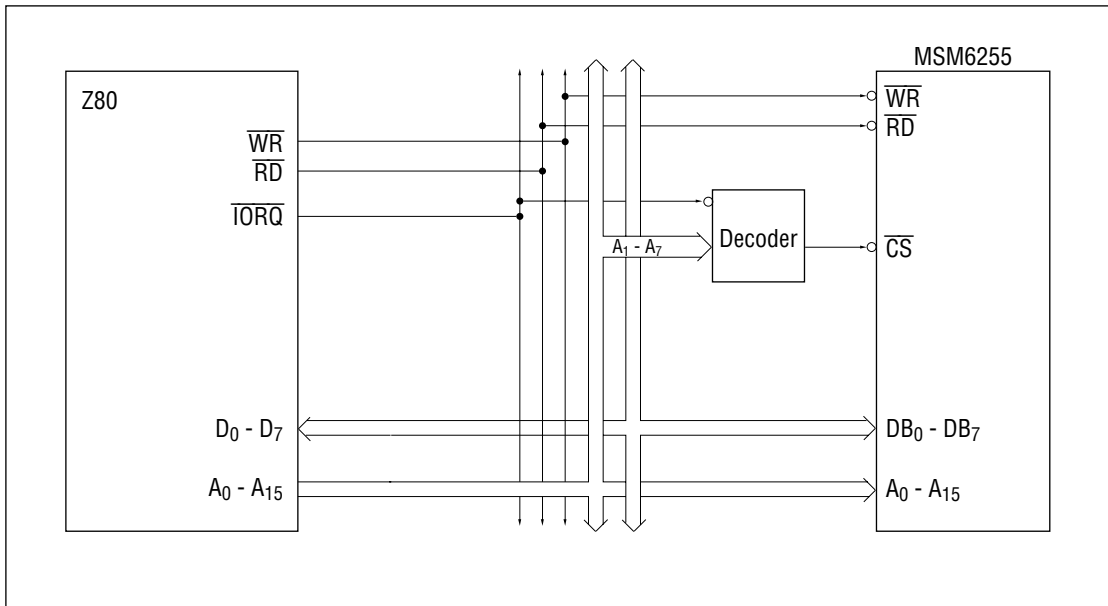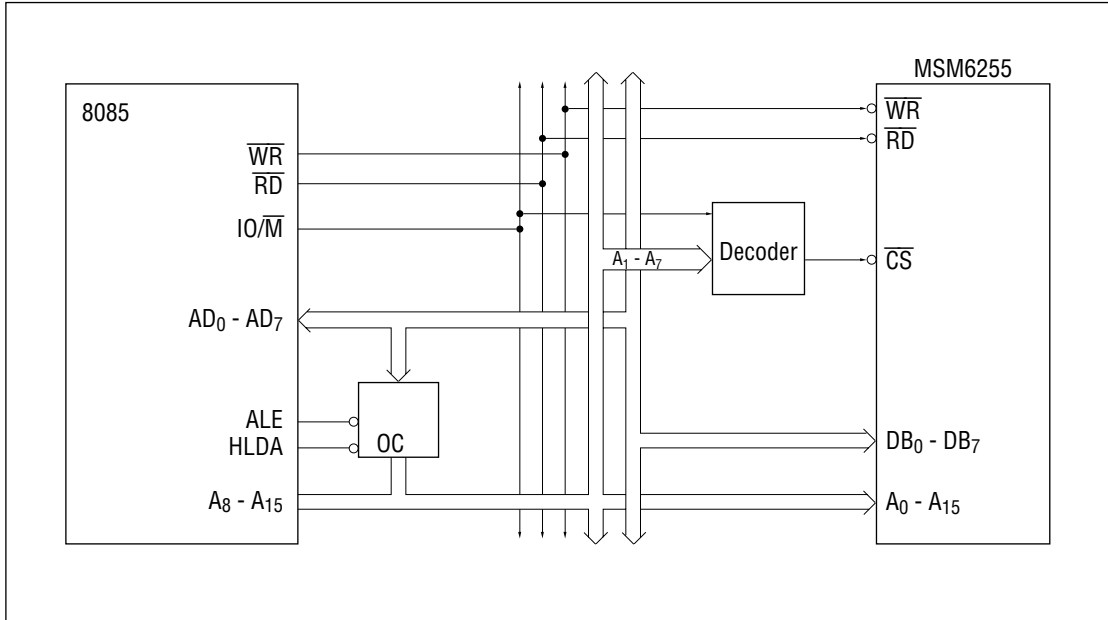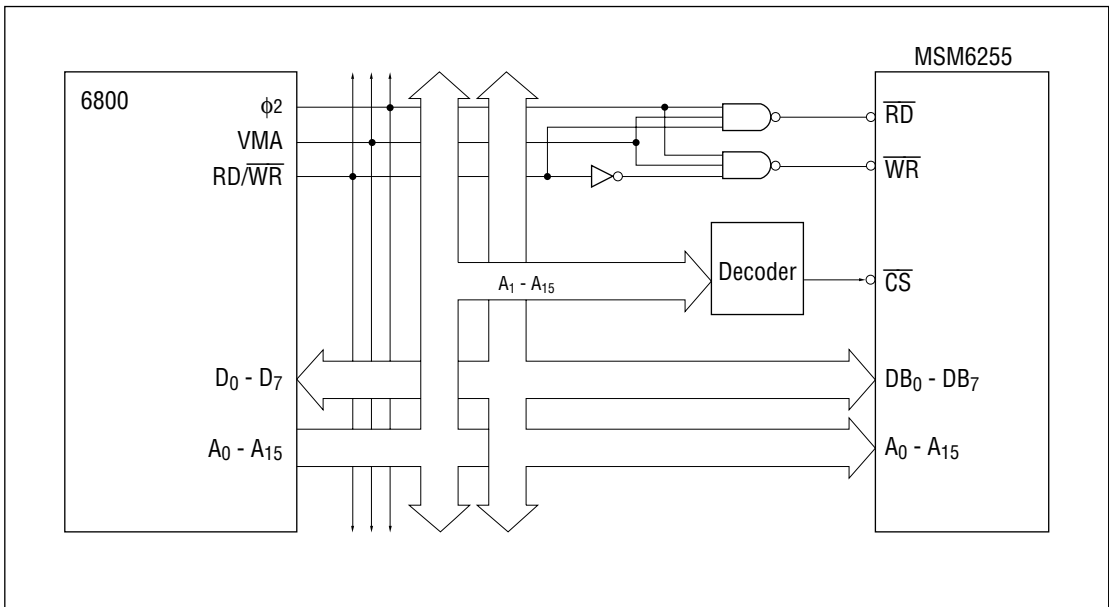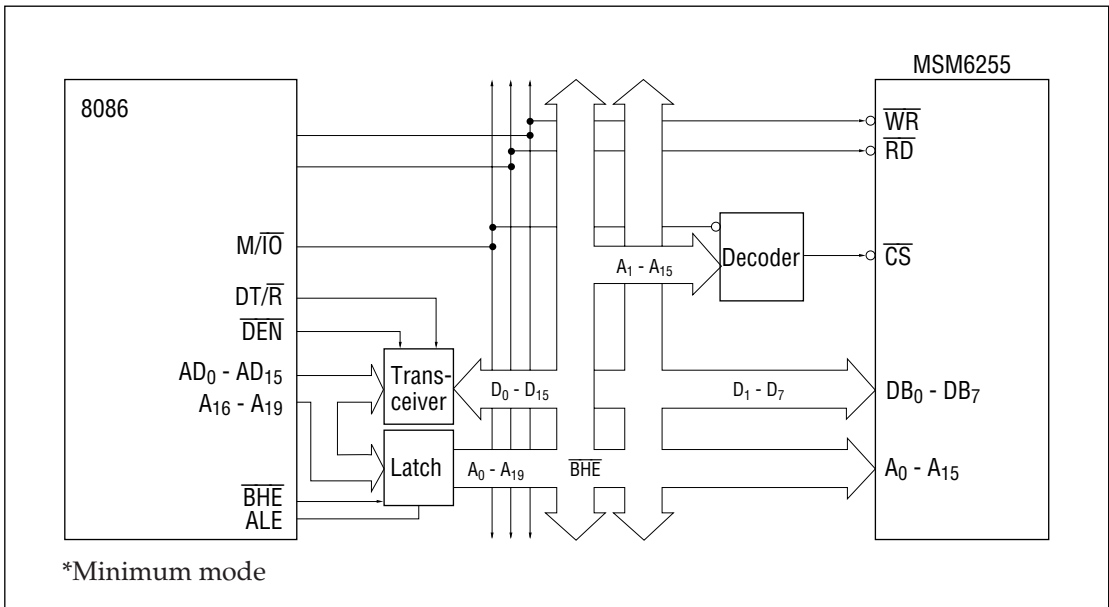
System Configuration

Fig. 12 System Configuration in Graphic Mode
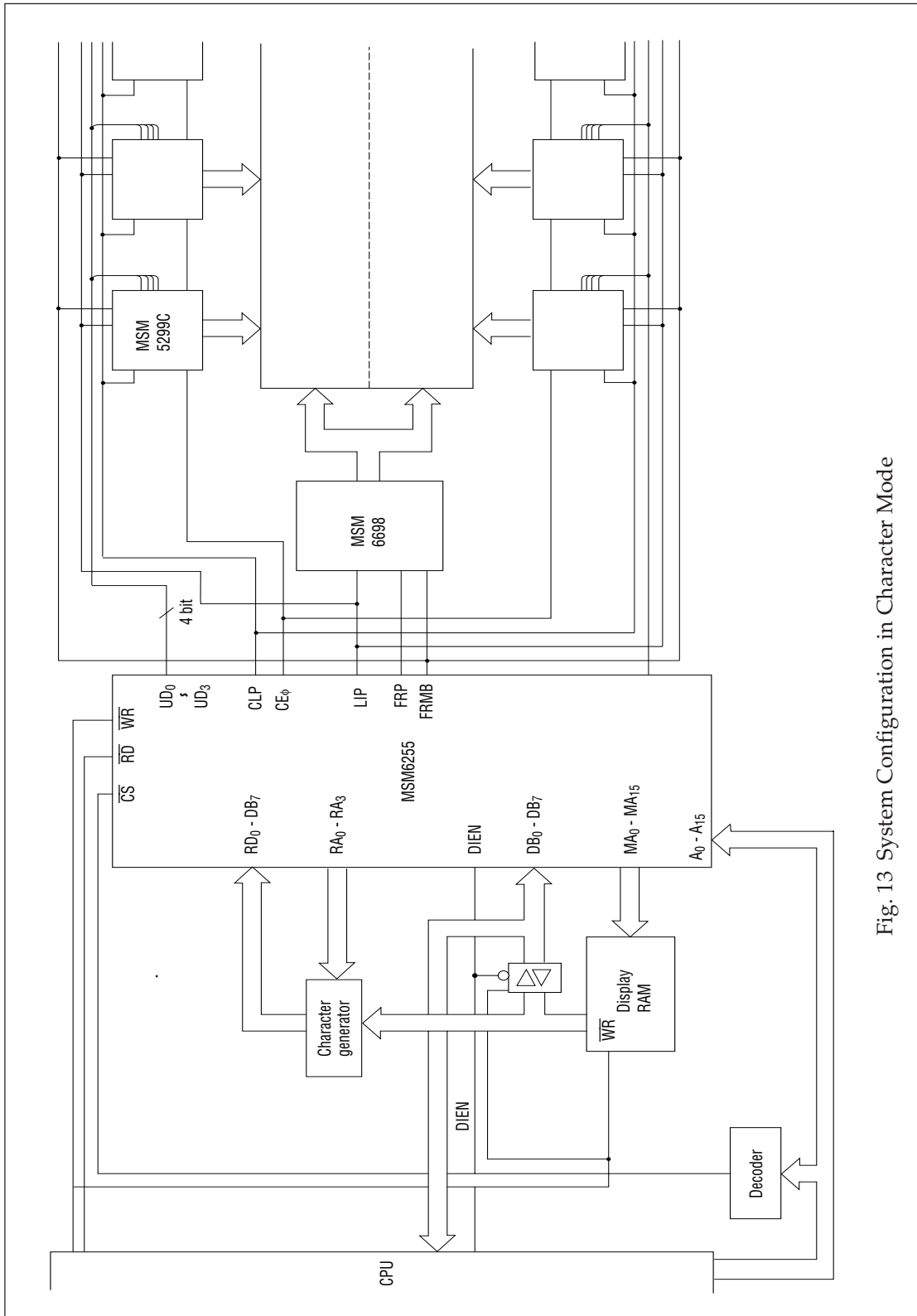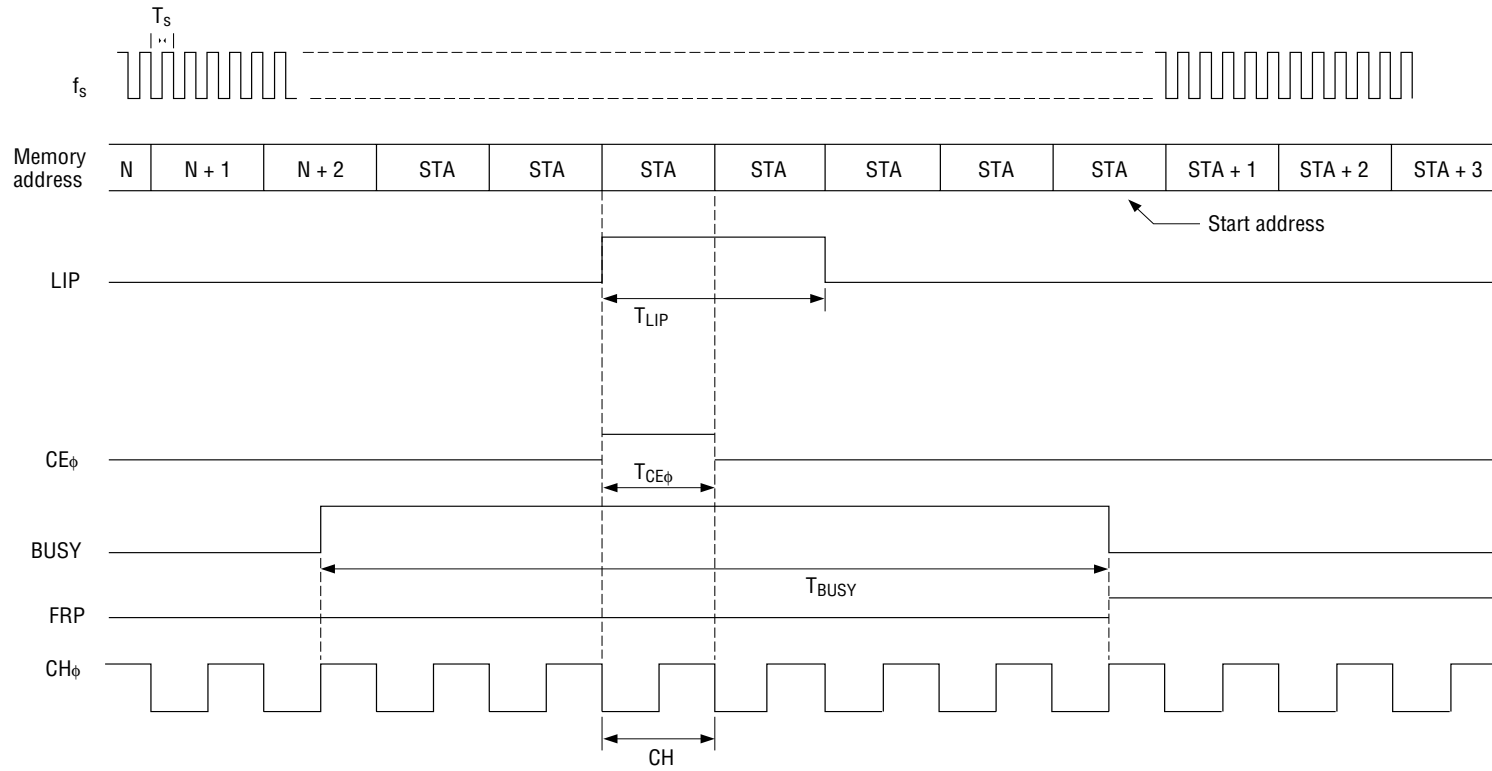
Fig. 13 System Configuration in Character Mode

Fig. 14 Timing Chart During Suspension of Shift Clock

Condition : 4-bit parallel output mode
$H_P = 5$

$CH = T_s \times Hp$
$T_{LIP} = 2CH$
$T_{CE\phi} = CH$
$T_{BUSY} = 7CH$
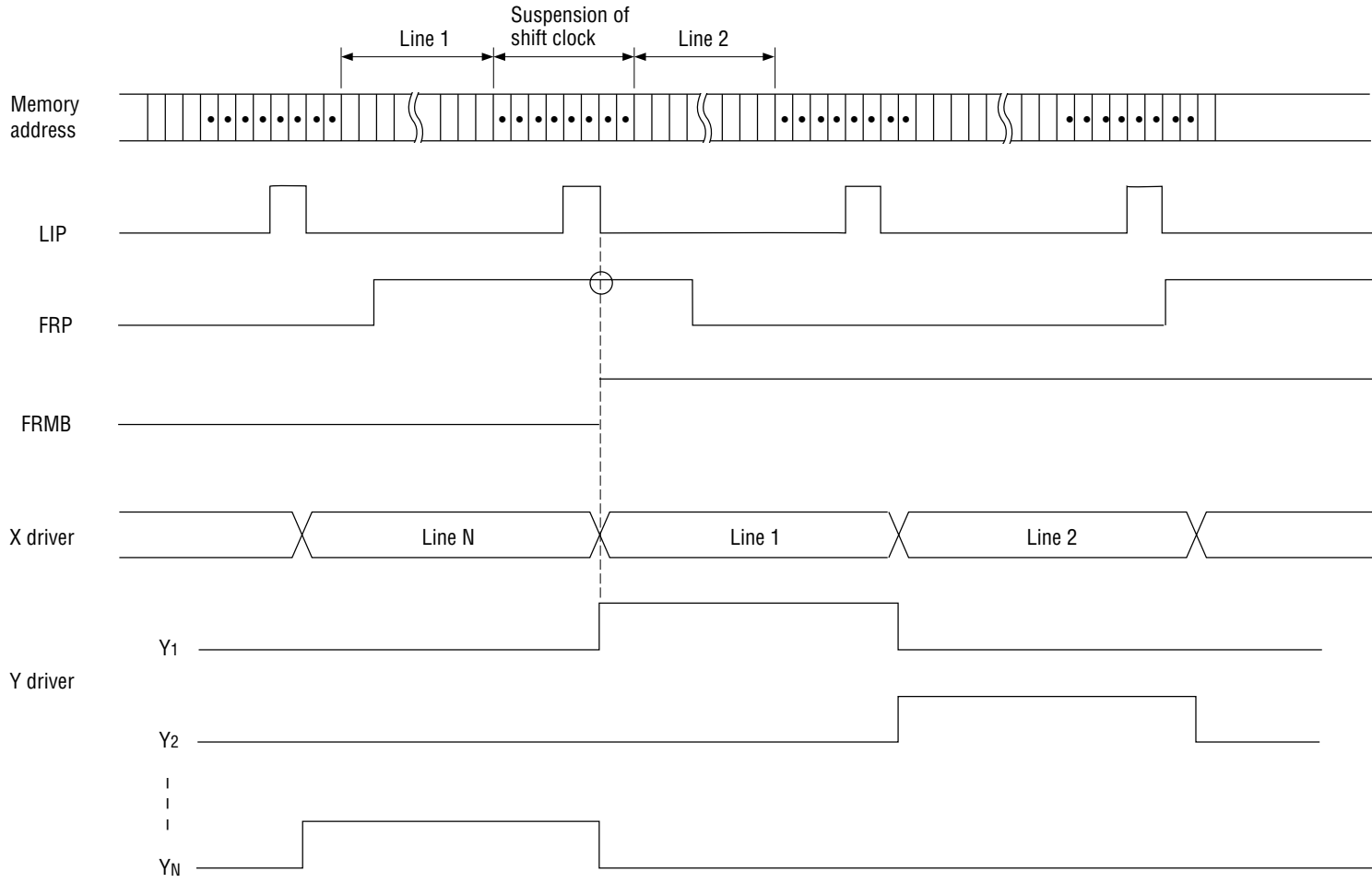
Fig. 15 Timing Chart of LIP, FRP and FRMB

Fig.16 Timing Chart of CLP and CEφ
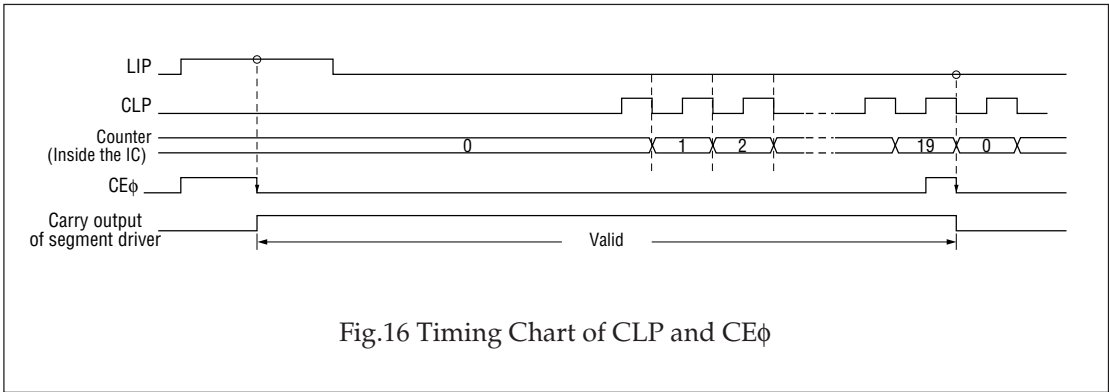
Figures 17-1, 17-2, and 18 show application circuits.
In these examples, the size of LCD module is 640 x 200 dots.
4-bit data transfer is applied and $H_p = 8$.
The synchronized access method is used as a method of access to the display VRAM.
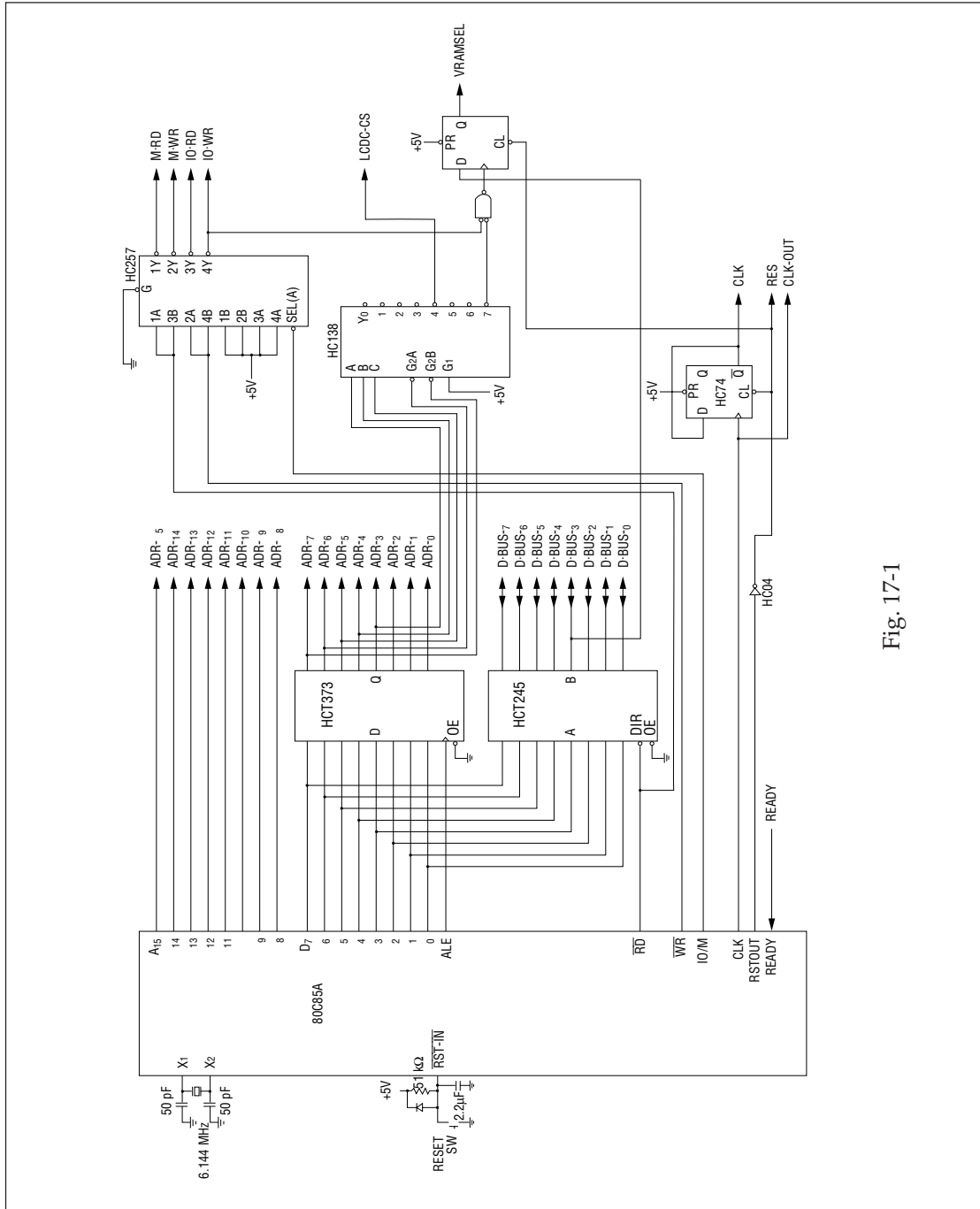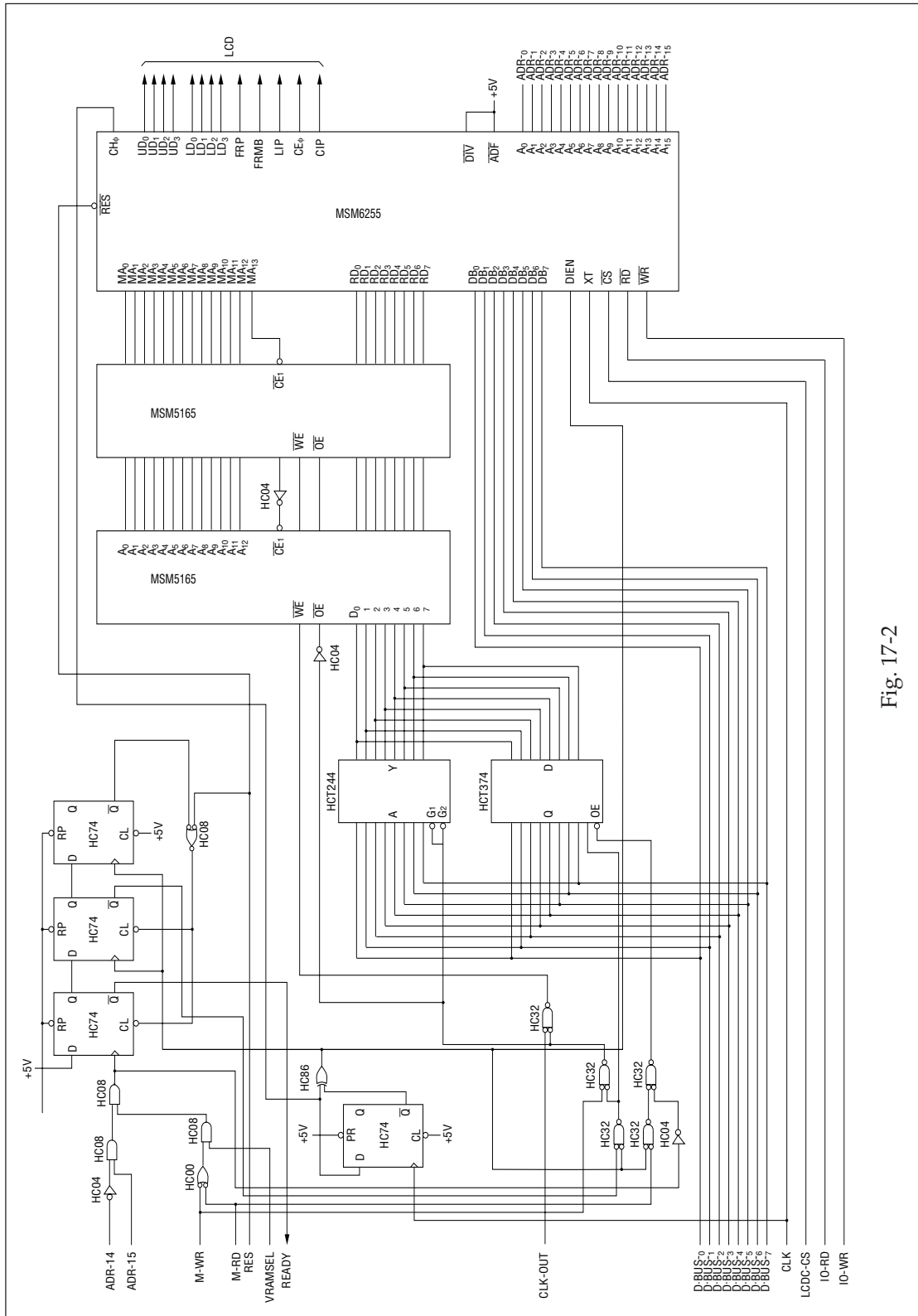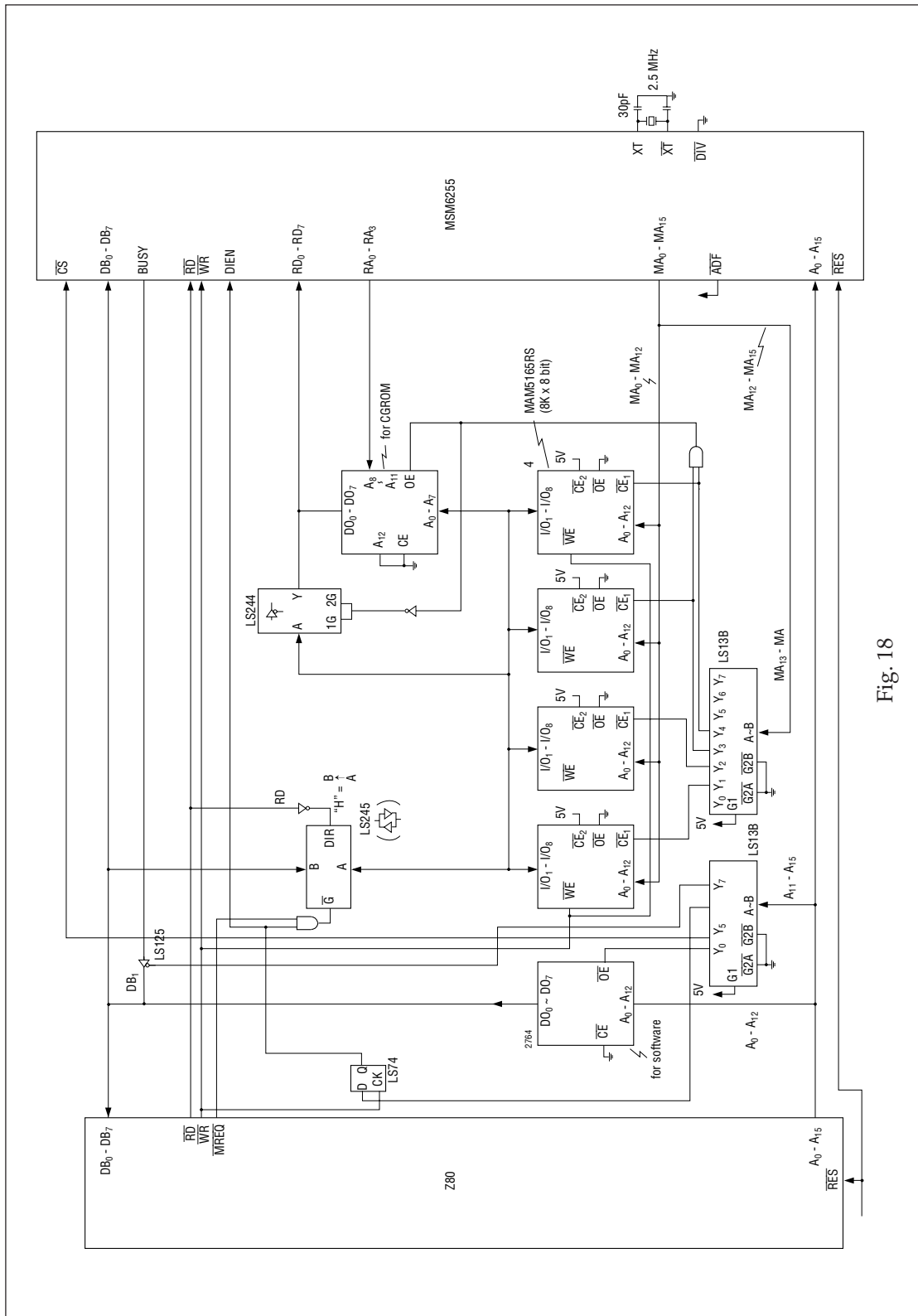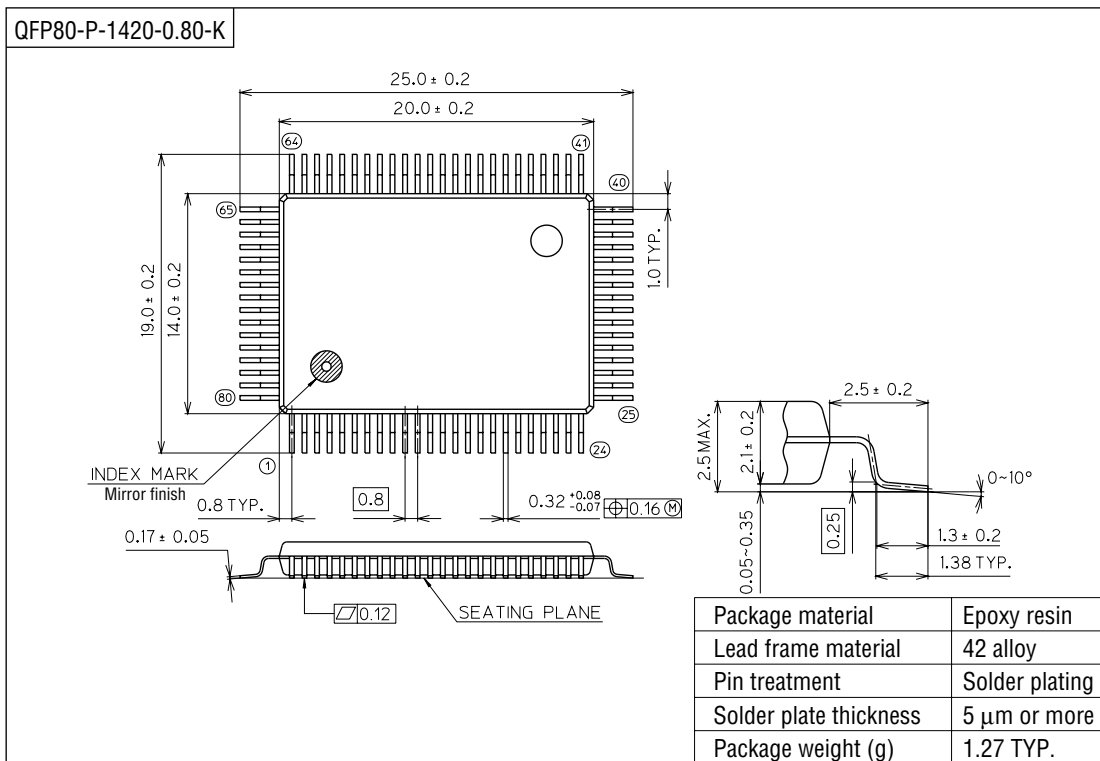

Fig. 17-1

Fig. 17-2

Fig. 18

PACKAGE DIMENSIONS

(Unit : mm)

QFP80-P-1420-0.80-K

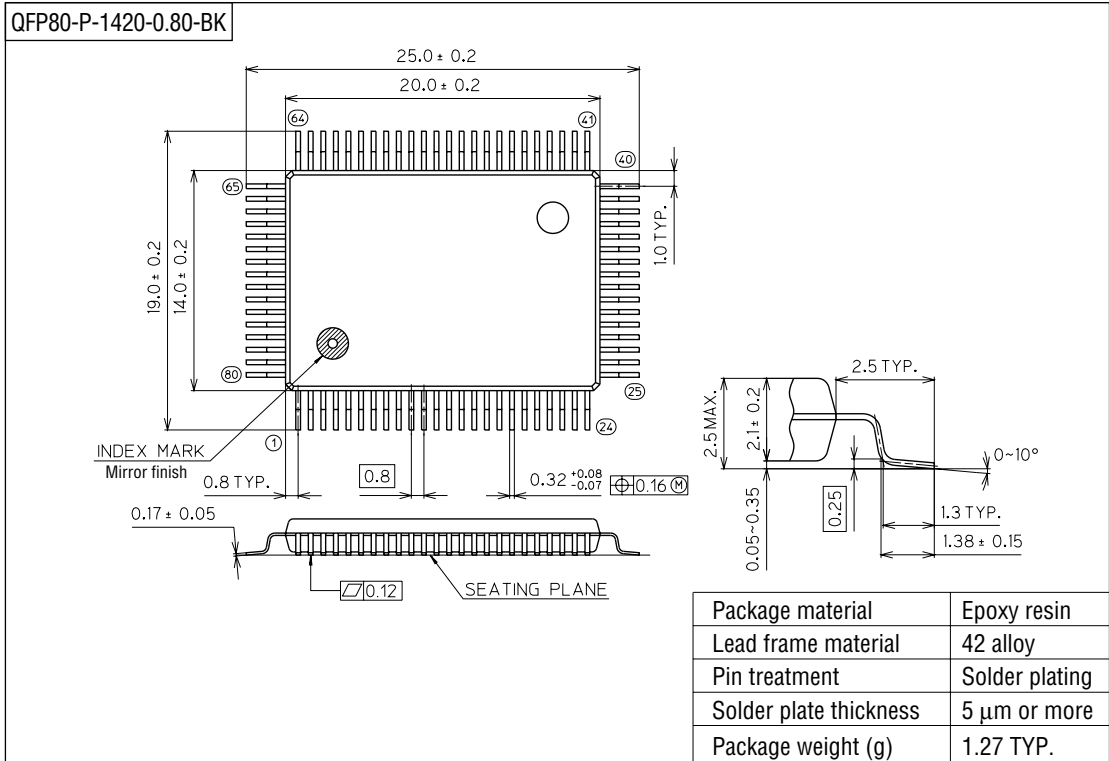| Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.27 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP80-P-1420-0.80-BK

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.27 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).