Review of Sub-1-V Bandgap Reference

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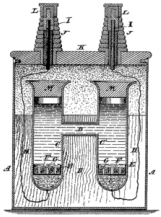
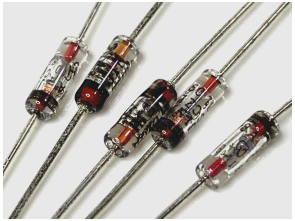
Voltage References

- Extremely important:
  - Bias circuits, signal conditioning, power regulation, VCO ...
- After the 1950s, Zener diodes began to replace the Weston standard cell [1, 2]
  - Miniaturized, but reduced lifetime [3]
- Manufacturing advancements led to highly-doped pn junctions, reducing their temperature dependence [4]
- The bandgap reference circuit leverages additional device properties to render the output voltage a function of only the material bandgap





Basic Bandgap Theory
PN Junction

- Current is related to V_f, which is linearly dependent on temperature
- The saturation current can be shown by approximating the temperature dependence of n_i [5]
- Normally, PN junctions don't behave this way due to surface effects & depeletion region generation / recombination [6]
- This ***does*** nicely describe the workings of a BJT

$$V_T = \frac{kT}{q} \approx 8.617 \times 10^{-5}\,\text{V/K} \tag{1}$$

$$I = I_s \left[\exp\left(\frac{V_f}{V_T}\right) - 1 \right] \tag{2}$$

$${n_i}^2 = C_0 T^3 \exp\left(\frac{-E_G}{kT}\right)$$

$$I_s \simeq C_{p^+n,n^+p} T^{\beta_{p,n}} \exp\left(\frac{-E_G}{kT}\right) \tag{3}$$

- Performing a Taylor series expansion on the formula for V_{BE} as a function of I_C yields this mess:

$$V_{BE} = \frac{kT_0}{q}\left\{\ln\left(\frac{I_C}{I_S T_0}\right) + \left[\ln\left(\frac{I_C}{I_S T_0}\right) - \left(\beta + \frac{E_{G_0}}{kT_0}\right)\right]\left(\frac{T}{T_0} - 1\right) - \frac{\beta}{2}\left(\frac{T}{T_0} - 1\right)^2 + \cdots + \frac{\beta(-1)^{(n-1)}}{n(n-1)}\left(\frac{T}{T_0} - 1\right)^n + \cdots\right\}$$

$$V_{BE} > 4V_T, \qquad T < 2T_0$$

  which neatly shows that as doping concentration increases, temperature dependence decreases [7]
- It is possible to choose a ratio of devices Θ to compensate this thermal relationship

$$\Theta = r\ln\left(\frac{I_{C_2}}{I_{S_2} T_0}\right) - m\ln\left(\frac{I_{C_1}}{I_{S_1} T_0}\right) \tag{4}$$

Basic Bandgap Theory
Thermal Compensation

- By properly selecting Θ, the first order temperature dependence of current density is eliminated
- Since E_{G_0} is much greater than ΦV_{T_0}, V_{ref} becomes primarily a function of the bandgap
- In a standard bandgap core, the temperature coefficient of $V_{BE} = -2\,\text{mV/°C}$ is cancelled by the ΔV_{BE} from the current density ratio [8, 9]

$$\Delta V_{BE} = V_T \ln\left(\frac{I_{C_2}}{I_{C_1}}\right), \quad I_C = I_{C_0}\left(\frac{T}{T_0}\right)$$
$$\Delta V_{BE} = V_T \ln\left(\frac{T_0}{T}\right) \tag{5}$$

- Many designs like those of Widlar, Kuijk, and Brokaw enhance the performance with additional error amplification and series regulation
- With $E_{G_{Si}} = 1.12\,\text{eV}$, standard bandgap topologies have a lower limit around 1.25 V, dependent on the threshold voltage of the devices used for its construction [10]

$$V_{ref} = V_{f_1} + \frac{R_2}{R_3} V_T \ln\left(\frac{R_2}{R_1} N\right) \tag{6}$$

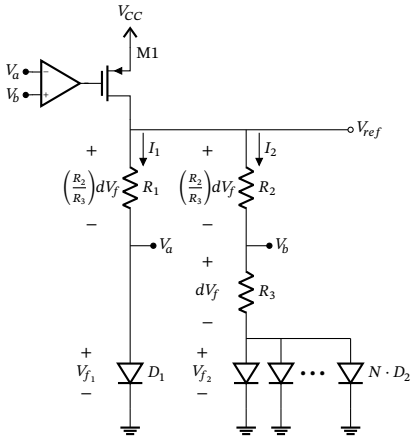


Figure 1: Conventional bandgap reference circuit schematic used for comparison. Redrawn from [11].

Banba et al. Design

- Presented at 1998 Symposium on VLSI Circuits
- Current-mode operation
- Resistive dividers placed in parallel with diode devices
- Additional current sources used in a current-mirror configuration
- Desired equilibrium: $I_1 = I_2 = I_3$

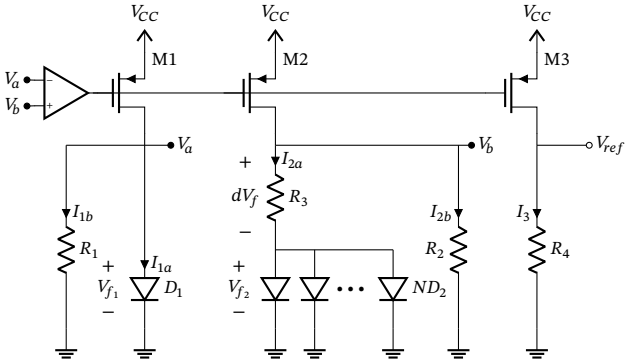


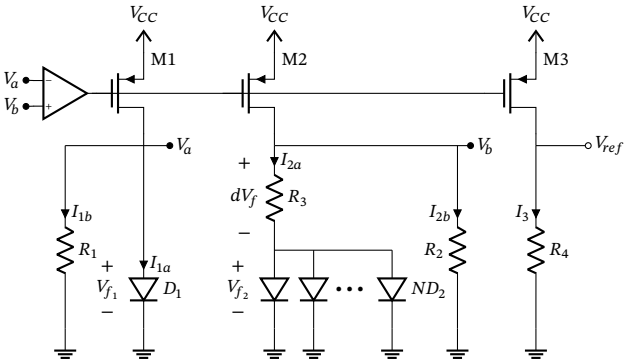
Figure 2: Proposed bandgap reference circuit schematic. Redrawn from [11].

Banba et al. Design

- All else equal, lower V_{ref} limit is reduced by a factor of $R2/R4$
- With $M_{1,2,3}$ in saturation V_{CC} can theoretically be lowered to V_f if $V_{ref} < V_f$

$$V_{ref,old} = V_{f_1} + \frac{R_2}{R_3} V_T \ln\left(\frac{R_2}{R_1} N\right)$$

$$V_{ref,new} = \frac{R_4}{R_2} V_{f_1} + \frac{R_4}{R_3} V_T \ln(N) \qquad (7)$$



Their Results

They did not manage to achieve operation under 1 V V_{CC}!

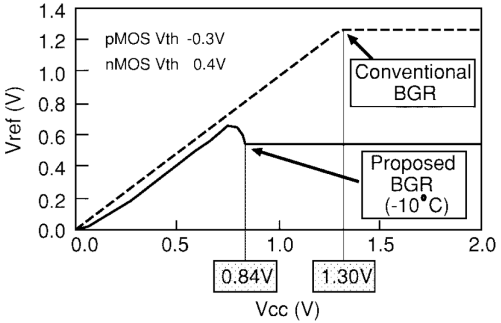


Figure 3: What they expected.

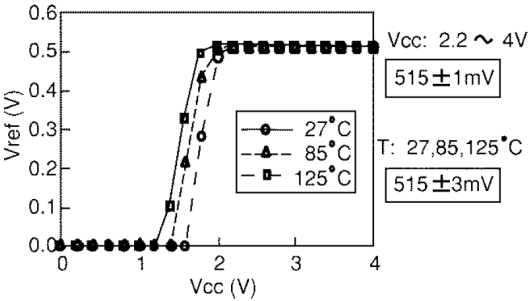


Figure 4: What they got.

Their Results
What Happened?

- Authors worked at Toshiba
- A 400 nm flash memory process was selected with very high threshold voltages
- This prevented their design from even turning on before 1 V V_{CC}, which they claimed operation under
- Native NMOS devices were used at the inputs of the op-amp to compensate for the poor threshold voltages
- Why this choice of fabrication process?

Simulation Process	Unknown Parameters
V_{th_p}	-0.3 V
V_{th_n}	0.4 V

Table 1: Simulated threshold voltages.

Flash Memory Process	0.4 µm P-sub CMOS 1 poly, 1 silicide, 2 metal
V_{th_p}	-1.0 V
V_{th_n}	0.7 V
$V_{th_n,nat}$	-0.2 V

Table 2: Fabricated threshold voltages.

Their Results
Significance

- Papers have collectively been cited over 800 times
- Obvious impact on the industry despite poor hardware results
- No real follow-up work from the authors
- PSRR was not reported
- In reporting distributions, the conventional design had 34 data points, whereas the new design only had 23
- Process parameters for the BJT devices may also have been useful

Recommendations

- Verify performance in a process designed for low voltage operation
- Use same number of data points for design comparison
- Low-tempco thin film resistors, trimmed resistors & BJTs [12, 13, 14]
- Substitute resistors with MOS devices [15]

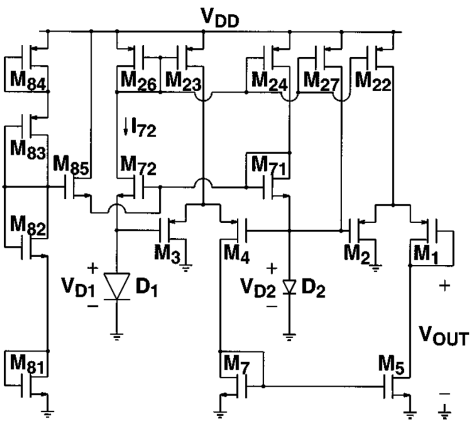


Figure 5: Schematic of resistorless bandgap circuit proposed in [15].

Recent Developments

- A group from the University of Pisa proposed a design in 2021 for supply volages down to 0.5 [16]
- Uses a “classic” all-CMOS bandgap core modified with low threshold and native devices in a 0.18 µm process
- Combined with a switched-cap integrator for offset cancellation and low-frequency noise reduction
- $V_{ref} = 220\,\text{mV}$ with sensitivity of 45 ppm/° C with current draw of 630 nA
- Considerable performance analysis shown in the paper

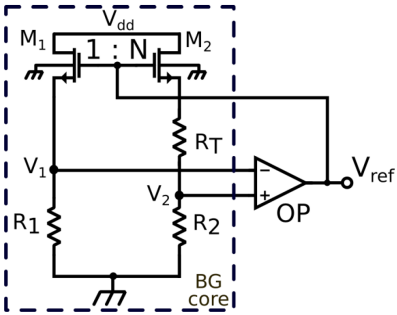


Figure 6: Schematic of all-CMOS design proposed in [16].

A Generic Approach

- Banba's design was constructed in the Cādence gpdk45_v5.0 to see its performance in a process that was designed for low voltage operation
- Its performance was compared with the stated conventional design, using the same device parameters
- All 1 V-LVT devices were used

gpdk45_v5.0	45 nm 1 s, 1 p, 11 m
V_{th_p}	−0.34 V
V_{th_n}	0.28 V

Table 3: 1 V-LVT threshold voltages, around the sizes simulated.

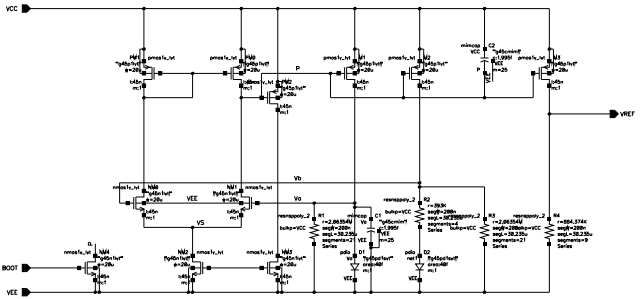
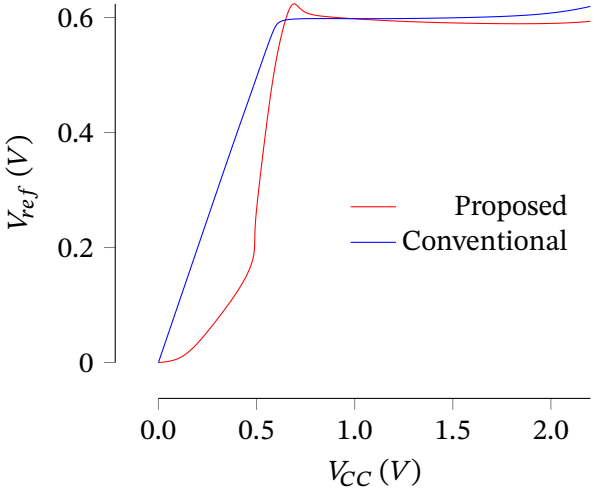


Figure 7: Schematic of the new bandgap as simulated in Cādence Virtuoso. Device sizing as suggested by Razavi, scaled for $l = 45\,\text{nm}$ [17].

It Works!

- Operation down to about 0.7 V was achieved for both designs
- Shows the devere dependence on the threshold voltage
- Proposed design is able to achieve much lower V_{ref} and lower temperature variation
- Startup behavior for the proposed design was consistently slower
- Often showed less stability in operating range
  - Could be due to lack of optimization and poor startup circuit implementation



It Works!

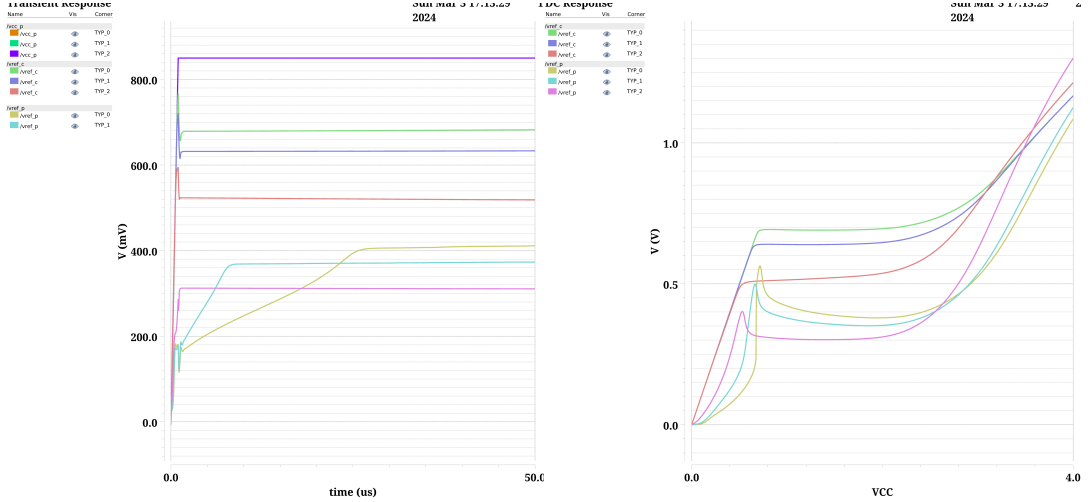


Figure 9: Simulated results over 0, 27, and 100 °C, transient and DC.

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