

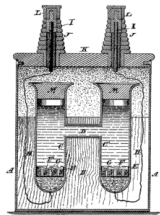
Review of Sub-1-V Bandgap Reference

Chris Biancone

EE726 Mixed-Signal IC Design
Electrical and Microelectronic Engineering
Rochester Institute of Technology

2024-03-04

- Extremely important:
 - Bias circuits, signal conditioning, power regulation, VCO ...
- After the 1950s, Zener diodes began to replace the Weston standard cell [1,2]
 - Miniaturized, but reduced lifetime [3]
- Manufacturing advancements led to highly-doped pn junctions, reducing their temperature dependence [4]
- The bandgap reference circuit leverages additional device properties to render the output voltage a function of only the material bandgap



Basic Bandgap Theory

PN Junction

- Current is related to V_f , which is linearly dependent on temperature
- The saturation current can be shown by approximating the temperature dependence of n_i [5]
- Normally, PN junctions don't behave this way due to surface effects & depletion region generation / recombination [6]
- This *does* nicely describe the workings of a BJT

$$V_T = \frac{kT}{q} \approx 8.617 \times 10^{-5} \text{ V/K} \quad (1)$$

$$I = I_s \left[\exp\left(\frac{V_f}{V_T}\right) - 1 \right] \quad (2)$$

$$n_i^2 = C_0 T^3 \exp\left(\frac{-E_G}{kT}\right)$$
$$I_s \simeq C_{p+n,p} T^{\beta_{p,n}} \exp\left(\frac{-E_G}{kT}\right) \quad (3)$$

- Performing a Taylor series expansion on the formula for V_{BE} as a function of I_C yields this mess:

$$V_{BE} = \frac{kT_0}{q} \left\{ \ln\left(\frac{I_C}{I_S T_0}\right) + \left[\ln\left(\frac{I_C}{I_S T_0}\right) - \left(\beta + \frac{E_{G0}}{kT_0}\right) \right] \left(\frac{T}{T_0} - 1\right) - \frac{\beta}{2} \left(\frac{T}{T_0} - 1\right)^2 + \dots + \frac{\beta(-1)^{(n-1)}}{n(n-1)} \left(\frac{T}{T_0} - 1\right)^n + \dots \right\}$$

$V_{BE} > 4V_T, \quad T < 2T_0$

which neatly shows that as doping concentration increases, temperature dependence decreases [7]

- It is possible to choose a ratio of devices Θ to compensate this thermal relationship

$$\Theta = r \ln\left(\frac{I_{C2}}{I_{S2} T_0}\right) - m \ln\left(\frac{I_{C1}}{I_{S1} T_0}\right) \quad (4)$$

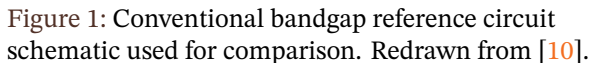
Basic Bandgap Theory

Thermal Compensation

- By properly selecting Θ , the first order temperature dependence of current density is eliminated
- Since E_{G_0} is much greater than ΦV_{T_0} , V_{ref} becomes primarily a function of the bandgap
- In a standard bandgap core, the temperature coefficient of $V_{BE} = -2 \text{ mV}/^\circ\text{C}$ is cancelled by the ΔV_{BE} from the current density ratio [8, 9]

$$\Delta V_{BE} = V_T \ln \left(\frac{I_{C_2}}{I_{C_1}} \right), \quad I_C = I_{C_0} \left(\frac{T}{T_0} \right)$$
$$\Delta V_{BE} = V_T \ln \left(\frac{T_0}{T} \right) \quad (5)$$

- $$V_{ref} = V_{f_1} + \frac{R_2}{R_3} V_T \ln \left(\frac{R_2}{R_1} N \right) \quad (6)$$



- Presented at 1998 Symposium on VLSI Circuits
- Current-mode operation
- Resistive dividers placed in parallel with diode devices
- Additional current sources used in a current-mirror configuration
- Desired equilibrium: $I_1 = I_2 = I_3$

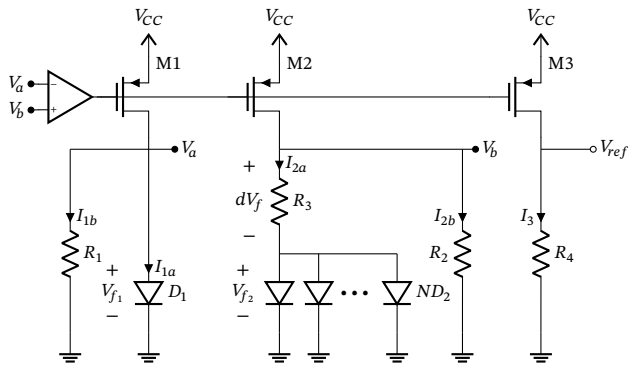
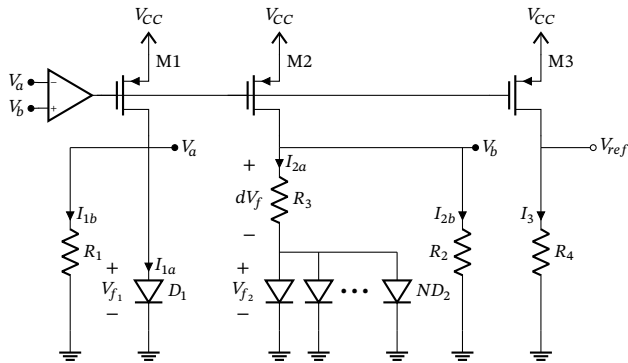


Figure 2: Proposed bandgap reference circuit schematic. Redrawn from [10].

- $$\begin{aligned} V_{ref,old} &= V_{f_1} + \frac{R_2}{R_3} V_T \ln \left(\frac{R_2}{R_1} N \right) \\ V_{ref,new} &= \frac{R_4}{R_2} V_{f_1} + \frac{R_4}{R_3} V_T \ln(N) \end{aligned} \quad (7)$$



They did not manage to achieve operation under 1 V V_{CC} !

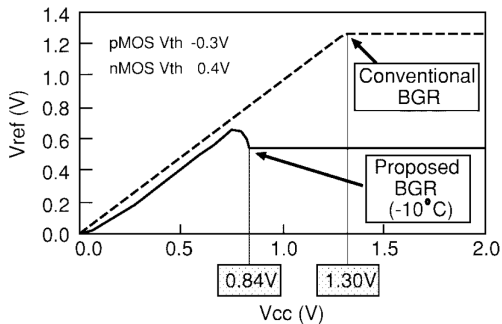


Figure 3: What they expected.

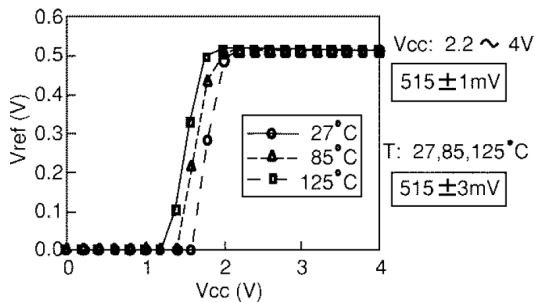


Figure 4: What they got.

Their Results

What Happened?

- Authors worked at Toshiba
- A 400 nm flash memory process was selected with very high threshold voltages
- This prevented their design from even turning on before 1 V V_{CC} , which they claimed operation under
- Native NMOS devices were used at the inputs of the op-amp to compensate for the poor threshold voltages
- Why this choice of fabrication process?

Simulation Process	Unknown Parameters
V_{thp}	-0.3 V
V_{thn}	0.4 V

Table 1: Simulated threshold voltages.

Flash Memory Process	0.4 μ m P-sub CMOS 1 poly, 1 silicide, 2 metal
V_{thp}	-1.0 V
V_{thn}	0.7 V
$V_{thn,nat}$	-0.2 V

Table 2: Fabricated threshold voltages.

Their Results

Significance

- Papers have collectively been cited over 800 times
- Obvious impact on the industry despite poor hardware results
- PSRR was not reported
- In reporting distributions, the conventional design had 34 data points, whereas the new design only had 23
- Process parameters for the BJT devices may also have been useful



- [illegible]

◀ ◻ ▶ ◀ ◻ ▶ ◀ ≡ ▶ ◀ ≡ ▶ ≡ ↺ 🔍 ↻

- A group from the University of Pisa proposed a design in 2021 for supply volages down to 0.5 [15]
- Uses a “classic” all-CMOS bandgap core modified with low threshold and native devices in a 0.18 μm process
- Combined with a switched-cap integrator for offset cancellation and low-frequency noise reduction
- $V_{ref} = 220 \text{ mV}$ with sensitivity of $45 \text{ ppm}/^\circ\text{C}$ with current draw of 630 nA
- Considerable performance analysis shown in the paper

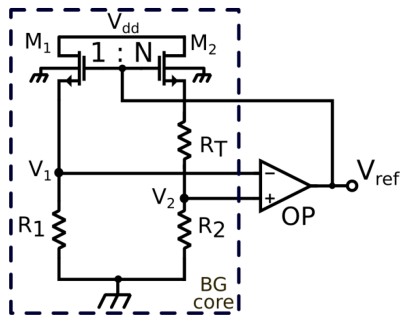


Figure 6: Schematic of all-CMOS design proposed in [15].

- Banba's design was constructed in the Cadence gpd45_v5.0 to see its performance in a process that was designed for low voltage operation
- Its performance was compared with the stated conventional design, using the same device parameters
- All 1 V-LVT devices were used

gpd45_v5.0	45 nm 1 s, 1 p, 11 m
V_{thp}	-0.34 V
V_{thn}	0.28 V

Table 3: 1 V-LVT threshold voltages, around the sizes simulated.

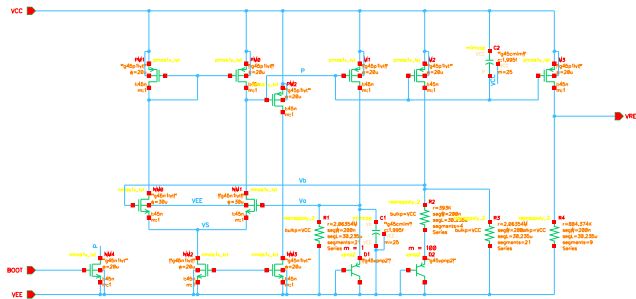
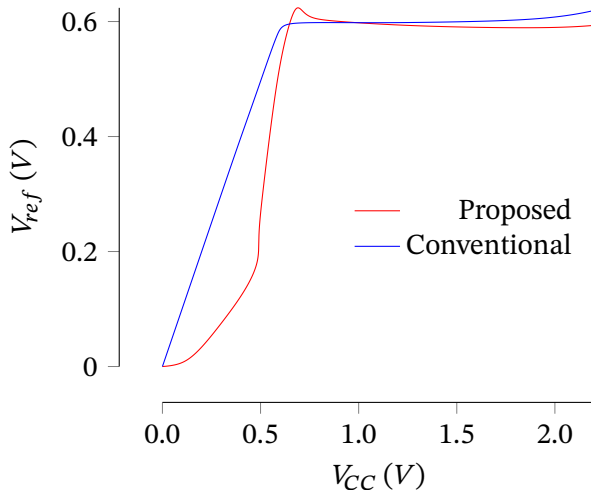

















Figure 7: Schematic of the new bandgap as simulated in Cadence Virtuoso.

- Operation down to about 0.7 V was achieved for both designs
- Shows the device dependence on the threshold voltage
- Proposed design is able to achieve much lower V_{ref} and lower temperature variation
- Startup behavior for the proposed design was consistently slower
- Often showed less stability in operating range
 - Could be due to lack of optimization and poor startup circuit implementation



-  E. Weston, “Voltaic cell,” US Patent US494 827A, 1893. [Online]. Available: <https://patents.google.com/patent/US494827>
-  C. Zener and H. H. Wills, “A theory of the electrical breakdown of solid dielectrics,” *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character*, vol. 145, pp. 523–529, 7 1934. [Online]. Available: <https://doi.org/10.1098/rspa.1934.0116>
-  R. P. Baker and J. Nagy, “An investigation of long-term stability of zener voltage references,” *IRE Transactions on Instrumentation*, vol. I-9, pp. 226–231, 9 1960. [Online]. Available: <https://doi.org/10.1109/IRE-I.1960.5006922>
-  D. Hilbiber, “A new semiconductor voltage standard.” IEEE, 1964, pp. 32–33. [Online]. Available: <https://doi.org/10.1109/ISSCC.1964.1157541>
-  J. Brugler, “Silicon transistor biasing for linear collector current temperature dependence,” *IEEE Journal of Solid-State Circuits*, vol. 2, pp. 57–58, 6 1967. [Online]. Available: <https://doi.org/10.1109/JSSC.1967.1049790>

-  C. tang Sah, R. Noyce, and W. Shockley, “Carrier generation and recombination in p-n junctions and p-n junction characteristics,” *Proceedings of the IRE*, vol. 45, pp. 1228–1243, 9 1957. [Online]. Available: <https://doi.org/10.1109/JRPROC.1957.278528>
-  C.-T. Sah, “Effect of surface recombination and channel on p-n junction and transistor characteristics,” *IRE Transactions on Electron Devices*, vol. 9, pp. 94–108, 1 1962. [Online]. Available: <https://doi.org/10.1109/T-ED.1962.14895>
-  R. Widlar, “An exact expression for the thermal variation of the emitter base voltage of bi-polar transistors,” *Proceedings of the IEEE*, vol. 55, pp. 96–97, 1 1967. [Online]. Available: <https://doi.org/10.1109/PROC.1967.5396>
-  R. Pease, “The design of band-gap reference circuits: trials and tribulations.” IEEE, 1990, pp. 214–218. [Online]. Available: <https://doi.org/10.1109/BIPOL.1990.171166>
-  H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, “A cmos bandgap reference circuit with sub-1-v operation,” *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 670–674, 5 1999. [Online]. Available: <https://doi.org/10.1109/4.760378>

-  A. Brokaw, “A simple three-terminal ic bandgap reference,” *IEEE Journal of Solid-State Circuits*, vol. 9, pp. 388–393, 12 1974. [Online]. Available: <https://doi.org/10.1109/JSSC.1974.1050532>
-  P. Malcovati, F. Maloberti, C. Fiacchi, and M. Pruzzi, “Curvature-compensated bicmos bandgap with 1-v supply voltage,” *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1076–1081, 7 2001. [Online]. Available: <https://doi.org/10.1109/4.933463>
-  P. Mok and K. N. Leung, “Design considerations of recent advanced low-voltage low-temperature-coefficient cmos bandgap voltage reference.” IEEE, 2004. ISBN 0-7803-8495-4 pp. 635–642. [Online]. Available: <https://doi.org/10.1109/CICC.2004.1358907>
-  A. Buck, C. McDonald, S. Lewis, and T. Viswanathan, “A cmos bandgap reference without resistors,” *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 81–83, 1 2002. [Online]. Available: <https://doi.org/10.1109/4.974548>
-  A. Ria, A. Catania, P. Bruschi, and M. Piotto, “A low-power cmos bandgap voltage reference for supply voltages down to 0.5 v,” *Electronics*, vol. 10, p. 1901, 8 2021. [Online]. Available: <https://doi.org/10.3390/electronics10161901>