



EEEE 726: Project 2

RTR StrongARM Comparator

From: Chris Biancone
To: Dr. Mark Pude
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Abstract

The purpose of this project is to design a comparator to given specifications for subsequent use in flash and SAR ADC projects. A comparator based on the established StrongARM topology and modified for rail-to-rail operation has been constructed in the Cadence gpdk045_v5.0 PDK using 2 V CMOS devices. The comparator is followed by an SR latch to produce a valid output for the entire clock cycle, with appropriate buffering to drive a 1 pF load. The presented design achieves a nominal 16.44 mV hysteresis with 1.22 mV resolution and 1.426 ns propagation delay when sampling at the given target of 12 MHz for schematic level simulations. These results are achieved at a quiescent current draw of 258 pA for the entire design after stabilizing, with 29.3 pA contributed by the comparator itself. The design consumes an approximate 1.06 pW per decision. The performance is verified with minimal degradation in performance post-RC extraction across 60 PVT corners with 95% yield in monte carlo mismatch simulation.

1 Design Methodology

1.1 Circuit Topology

The StrongARM dynamic comparator is a popular power-saving comparator circuit design, known to be suitable for all seasons. By incorporating a clock at this stage in the signal chain, either all NMOS or PMOS sources are turned off for half of the input clock cycle, thereby minimizing quiescent power draw. Its comparison performance relies almost entirely on careful design of its constituent devices' parasitic capacitances [1]. During the reset phase of operation, all 4 internal nodes (X_1 , X_2 , O_1 , and

O_2) are charged up to VDD . At the beginning of the decision phase on the rising clock edge, the input pairs begin to turn on, a differential in voltage ΔV_X is produced relative to the voltage differential at the inputs and the resulting discharge path resistance at (X_1 and X_2). The relationship of this change to the input device parameters is shown in Eq. (1.1.1), omitting an additional term for non-ideal reset voltage (< VDD).

$$\Delta V_{X(ideal)} = \frac{-g_m r_o + sC_{gd}r_o}{1 + s\tau_a} \Delta V_{in}, \quad \tau_a = r_o(C_{gd} + C_{gs}) \quad (1.1.1)$$

As the nodes continue to drop, the cross-coupled (XCP) NMOS pair turns on and produces a ΔV_O . These nodes begin to fall as well with ΔV_O rapidly increasing, finally turning on the PMOS cross-coupled pair. The positive feedback from the XCPs takes hold of the voltage difference and snaps the output nodes O_1 and O_2 to the appropriate voltage rail. The reset/regen phase then serves to charge up the parasitic capacitances back to VDD , ready to make the next decision.

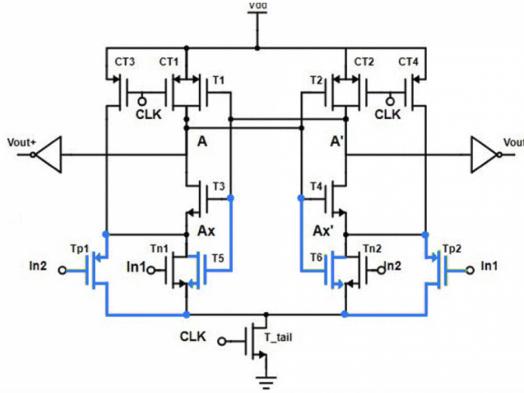


Figure 1.1.1: StrongARM comparator with additional devices to achieve rail-to-rail operation, reproduced from [2].

The design presented here is based largely on the recent work of M. A. Al-Qadasi et. al [2], which adds a complementary PMOS input pair to handle signals with a common mode voltage below the processing capability of the NMOS input pair, as shown in Fig. 1.1.1. Additionally, two NMOS devices are added in parallel with the input and attached to the cross-coupled devices, such that as ΔV_X grows, the NMOS device acts as a shunt to shut off the discharge path through the PMOS device that is on and prevent undetermined behavior. The NMOS devices are ideally of a lower threshold, to avoid operation specifically when only the PMOS devices are processing an input, but no 2V-LVT devices are available in the gpdk045.

Since this comparator makes a decision on each rising clock edge and resets on the falling edge, its output is invalid for half of the clock period. To remedy this, the output is fed to a standard SR latch with a logic buffer in between for decoupling the sensitive parasitic capacitances of the comparator. The output of this then mimics the behavior of a standard continuous-time design from the viewpoint of a receiving circuit.

1.2 Calculations

This design's reliance on the charging and discharging of parasitic capacitances, instead of the current steering of a standard comparator, provides atypical complexities when designing to specifications laid out for a continuous-time comparator. Notably, there is no DC operation of the dynamic comparator, so any DC characteristics like hysteresis must be estimated from a transient simulation. Meanwhile, standard device sizing methodologies like g_m/I_D do not apply as heavily as the design moves toward the digital realm. Few published works detail a concrete calculation of hysteresis voltage for a dynamic comparator, likely due to a pseudo-hysteresis implemented simply through the use of a clock to take discrete samples; Leïla Khanfir's recent publications surrounding her work on dynamic comparators with adjustable hysteresis provided a large basis of understanding for creating this design [3, 4, 5, 6].

For a linearly varying input, it can be shown that the hysteresis of the comparator is dependent on no less than 4 variables: T_{reset} (clock low), input voltage slope a , V_{cm} , and transistor parameters:

$$V_{HY} \Big|_{\Delta v_{in}(t)=at} = 2 \left[\frac{C_{IX} + C_{XB}}{C_{int}} \Delta V_{tc0,X} \exp\left(\frac{-t_{c1}}{\tau_a}\right) + \frac{C_{OB}}{C_{int}} \Delta V_{tc0,O} \right] + 2a \frac{g_m \tau_a \tau_b}{C_{int}} \left(1 - \exp\left(\frac{-t_{c1}}{\tau_a}\right) \right) \quad (1.2.1)$$

where C_{int} is a function of internal capacitors and t_{c1} is the time at which the comparator starts operating. Substituting the defined function for C_{int} allows finding V_{HY} as a function of these internal capacitances, which shows a greater sensitivity to the capacitances introduced at (X_1, X_2 (and their charging rates). This becomes useful when determining where to increase device sizes to increase yield over monte carlo simulations.

With a 12 MHz clock as a reference point, minimum device sizes are selected wherever possible, to allow for the fastest device operation and the ability to apply the final design to faster ADC circuits. While the StrongARM architecture has been proven in the gpdk045, this was done with 1 V devices that feature a minimum length of 45 nm [7]. The minimum length of 150 nm for 2V devices is already sizeable at 150 nm, and will contribute to slowing down the discharge of the capacitors due to the increased resistance seen at each node of the circuit. For matching, the input NMOS are selected to have 4 320 nm fingers of minimum size, so that the input PMOS devices and corresponding NMOS shunt devices may be half their size to avoid undetermined behavior. The tail switch and NMOS XCP devices are chosen to have 6 fingers, for resistance matching to the equivalent input stage. All of the PMOS sources are chosen to be minimum size with 2 fingers.

For the inverters and SR latch, all devices were initially conceived with 2 fingers at minimum size, which continued to work throughout simulation analysis. Shown in Fig. 1.2.1, the lengths of the input devices were increased to 1 μ m following monte carlo simulations and a sensitivity analysis, to increase yield. The full schematic is shown in Fig. 1.2.2.

2 Schematic Level Simulations

Schematic simulations were performed over PVT corners and monte carlo analysis. The process corners used were tt, ss, sf, fs, and ff, temperatures of 0, 27, 40, and 85 °C, and supply voltages of 1.8, 2.0, and 2.2 V. The schematic was captured and simulated using Cadence Virtuoso.

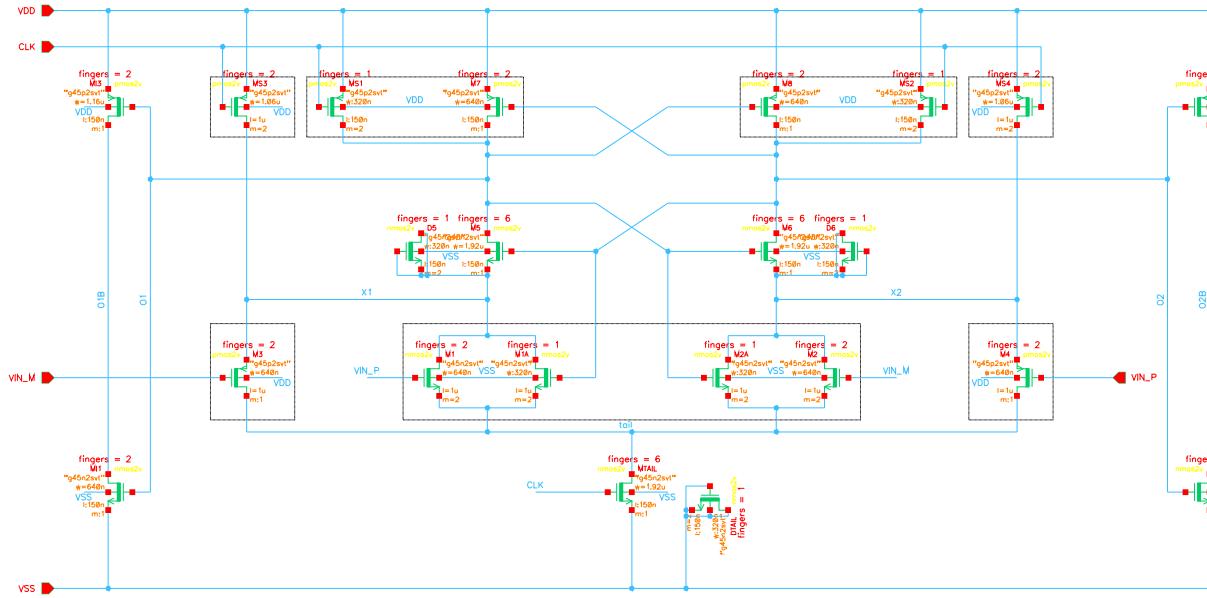


Figure 1.2.1: Schematic of RTR StrongARM comparator.

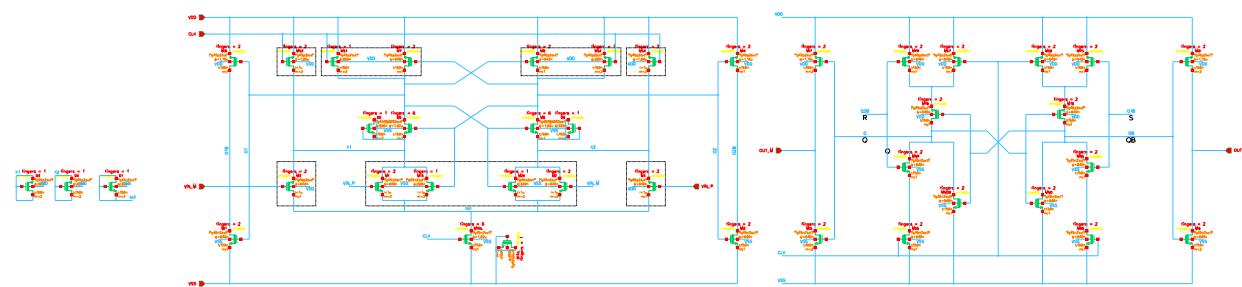


Figure 1.2.2: Schematic showing the comparator, inverters, and SR latch. Dummy devices used for layout are shown.

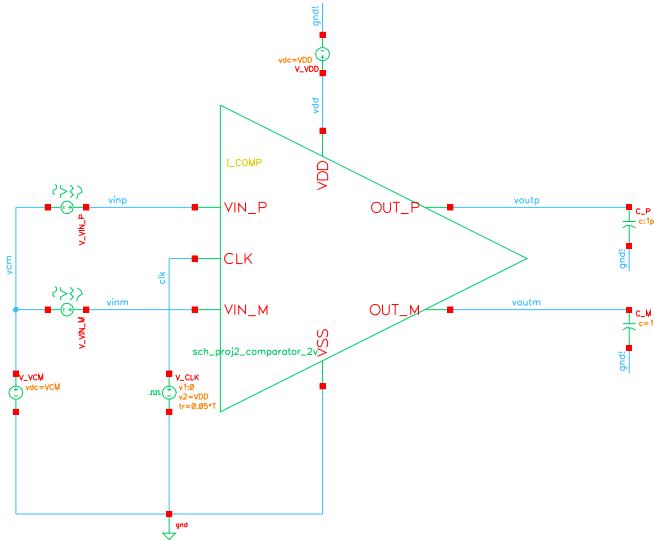


Figure 2.1.1: Testbench setup used for all analyses.

2.1 Hysteresis Testbench

As mentioned, all aspects of this comparator must be analyzed using a transient simulation due to its clocked operation. Testbenches were set up using the same schematic shown in Fig. 2.1.1, but varying the input *vsource* and clock period. The clock was simulated using an ideal pulse with 5% rise and fall time. Based on the work done in [5], a differential linear ramp was selected at a slope of 200 mV/ μ s to function as a slowly-varying input compared to the 12 MHz clock source.

The voltage at the positive input of the comparator was measured when the positive output both rose and fell, and the difference in the input voltage was determined to be the hysteresis.

2.2 Propagation Delay and ICMR Testbench

To analyze propagation delay, the piece-wise linear inputs were changed to pulse inputs of 12.5 mV magnitude, resulting in a total differential of 25 mV. The inputs were arranged such that the crossover occurred just before the clock rising edge. Since the testbench was set up with a DC common mode voltage source, this was varied using parametric simulation to determine that the rail-to-rail operation was achieved and estimate the range. An example waveform is shown in Fig. 2.2.1.

As mentioned previously, the hysteresis of the dynamic comparator is known to be dependent on the reset time given to it. Often, this is achieved by simply running the comparator near its maximum speed, but to avoid the extra power consumption required to do this, using a PWM clock to dynamically change the hysteresis was explored in simulations. The ability to achieve a nearly 120 mV range of hysteresis was found; however, this required tight control of the clock pulse width near 90% duty cycle. This was an interesting finding, but beyond the scope of this project for now. This principle is somewhat supported by [3, 6], where a 4-bit clock delay is implemented for the output buffers of the comparator to form a pseudo-schmitt trigger, but further investigation is needed on the viability of PWM clocking.

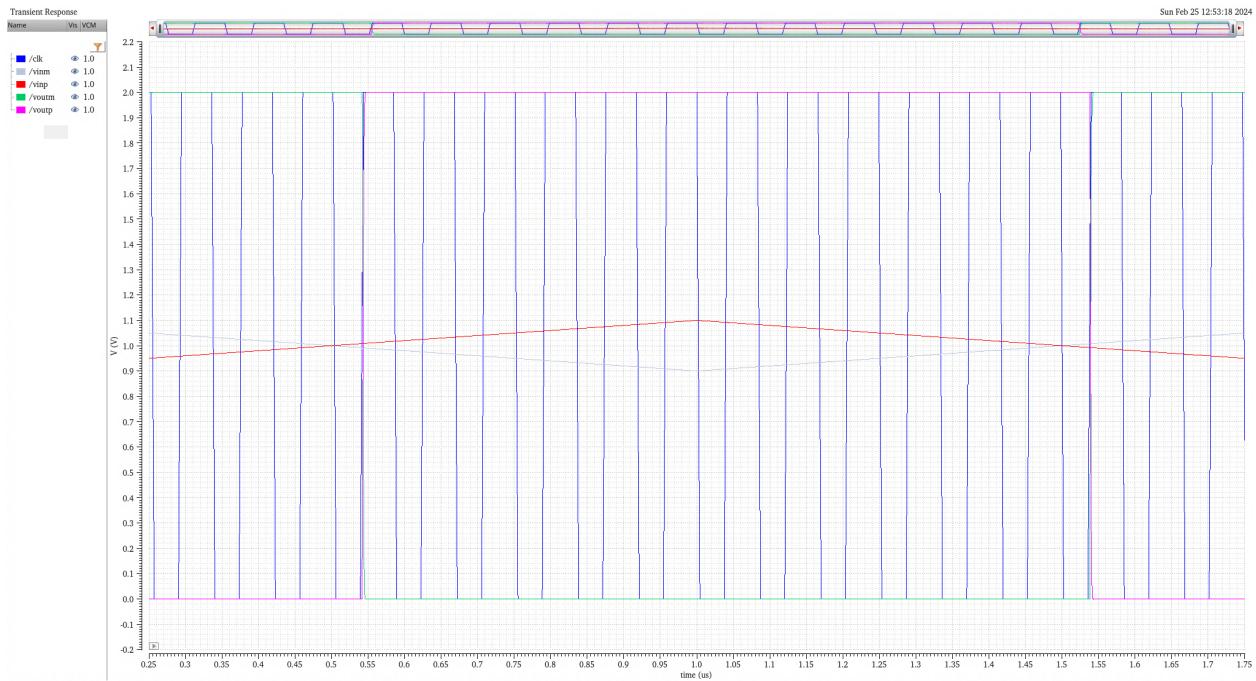


Figure 2.1.2: Hysteresis waveform.

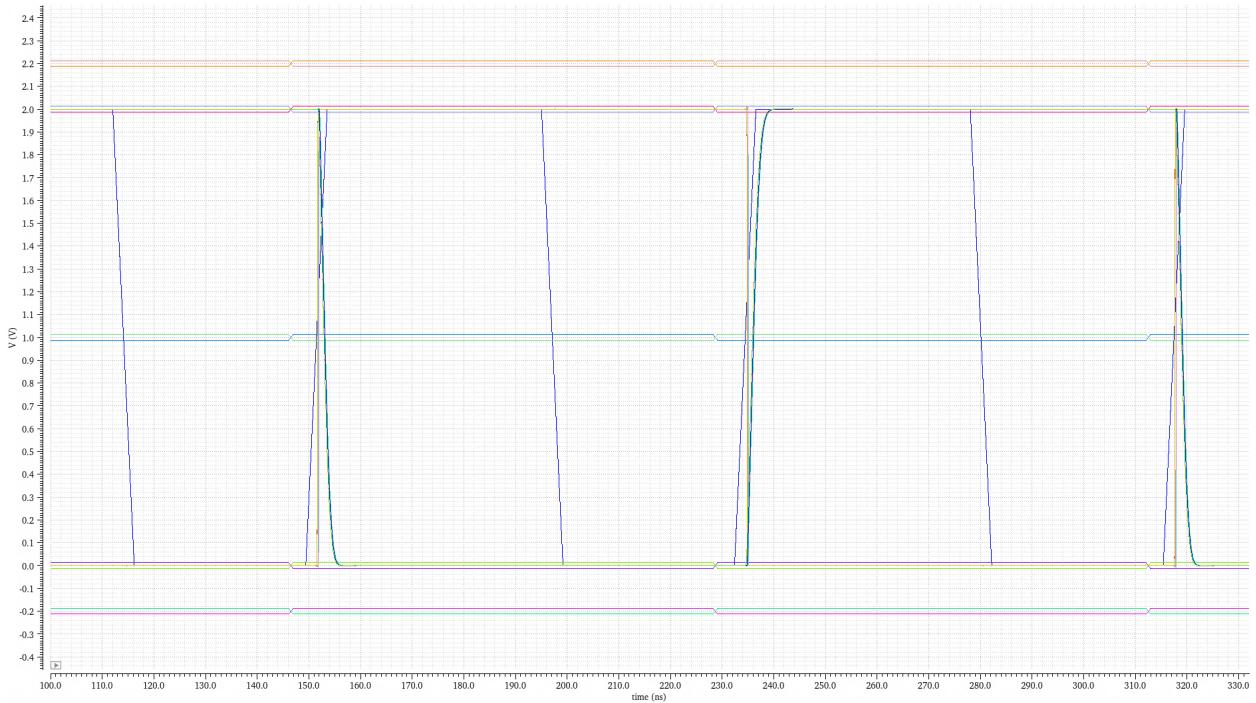


Figure 2.2.1: Propagation delay test output, showing varied input common mode voltage.

2.3 Resolution

Resolution was determined alongside the maximum reliable operation frequency the comparator could operate at. This was achieved simply by reducing the period of the clock within the hysteresis

Parameter	Units	Spec	Nominal	Min	Max
Hysteresis	mV	10-20	16.4434	16.31	16.7834
Prop. Delay (1 pF)	ns	10	1.5184	1.1999	2.3522
Prop. Delay (1 ff)	ps	-	395.17	203.73	645.72
Resolution	mV	<25	1.21953	0.546049	3.49453
DC Current	nA	minimize	0.25816	0.087434	9.0544
W/decision	pW	-	1.0667	0.4653	2.3157
ICMR	mV	-	-	-200	2200
Layout Area	μm^2	-	180	-	-

Table 1: PVT corner results.

Parameter	Units	Mean	Min	Max	Std Dev
Hysteresis	mV	16.6463	16.4731	33.0679	1.65875
Prop. Delay (1 pF)	ns	1.6106	1.5978	1.6346	0.0055696

Table 2: Monte carlo results.

testbench setup.

2.4 Results

After sizing the devices and performing initial simulations, a sensitivity analysis for random mismatch was run to determine the biggest contribution to poor monte carlo results. Fig. 2.4.2 shows that the circuit was most sensitive to variations in the input devices and PMOS switches MS3 and 4, which aligns with the expectation in Eq. (1.2.1) as these contribute to the capacitance and resistance at X_1 and X_2 . Increasing the lengths of these devices to 1 μm greatly increased the yield, and simulations were continued with these new values.

The comparator was able to easily achieve all design specification across corners at the schematic level. The schematic PVT corner results are summarized in Table 1.

The monte carlo mismatch analysis resulted in an overall yield of 98%, with details shown in Table 2.

3 Layout

Layout of the comparator was successfully accomplished with clean LVS and DRC - no errors in either. Much struggle was had while using the gpdk pcells, they resulted in many off-grid errors seemingly caused by themselves moving by 1 nm in random directions, which then pushed routes off by the same amount. Additionally, the dummy devices for the PMOS input pair were generated without contact cuts, and when abutted with the active devices, actually removed the contacts from the active devices. This was not caught for a while due to initially having M1-M2 contacts covering these areas. The final layout is shown in Fig. 3.0.1. The design is 16.1 μm by 9.96 μm .

A solid guard ring is placed around the comparator PMOS and NMOS devices to shield these devices from noise, which did substantially complicate the routing. Metal 3 was used sparingly for the inputs and to bridge two nodes shared within the SR latch.

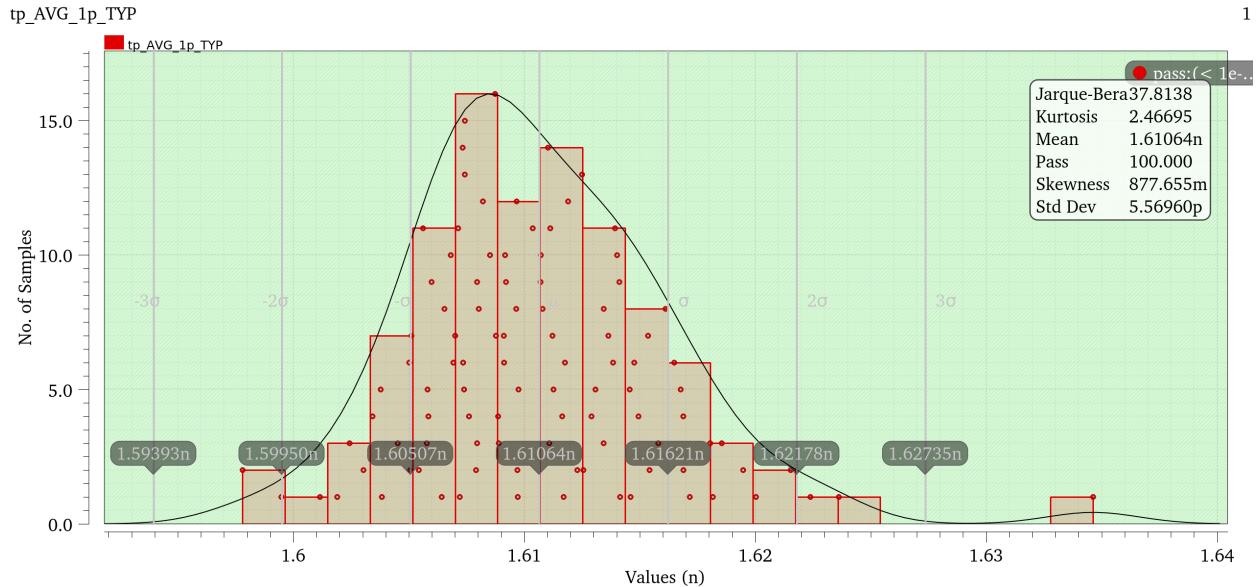


Figure 2.4.1: Propagation delay monte carlo histogram.

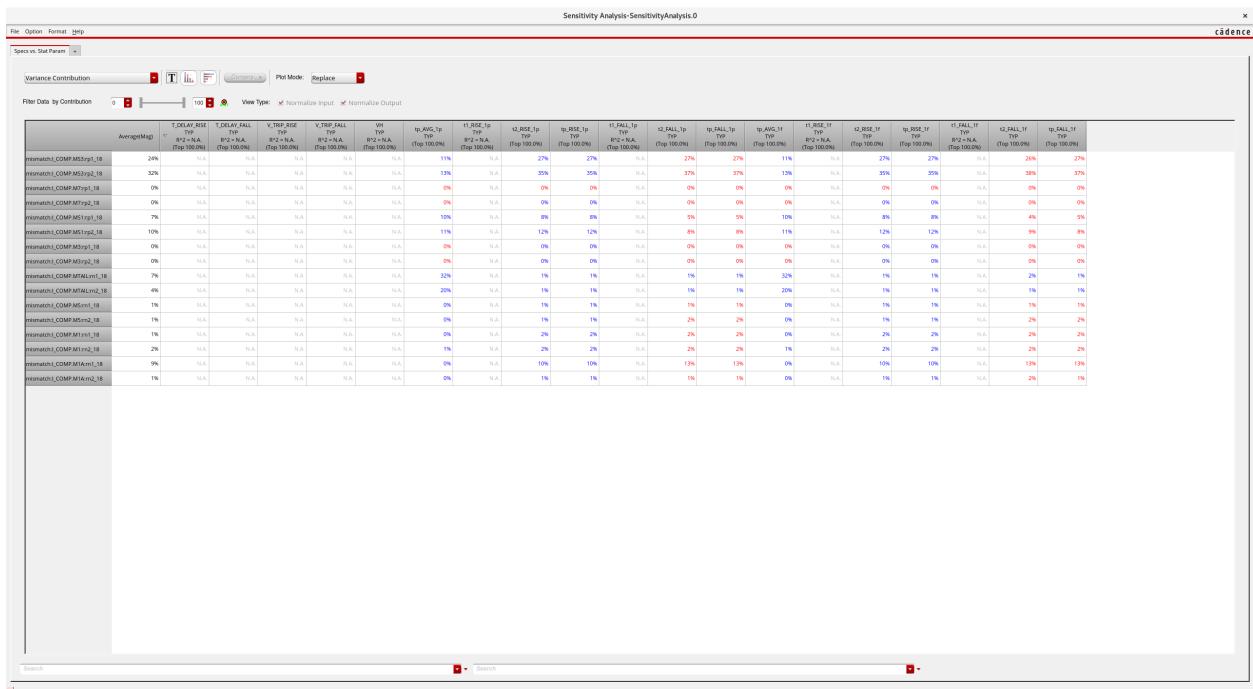


Figure 2.4.2: Sensitivity analysis to monte carlo mismatch.

4 Extracted Results

Layout parasitic extraction was performed using Quantus PVS, using the typical RCx setting with decoupled capacitance referenced to VSS. The resolution testbench could not be simulated across corners due to the amount of time it was taking; however, the hysteresis and propagation delay tests were simulated with close agreement to the schematic level simulations, verifying the robustness of

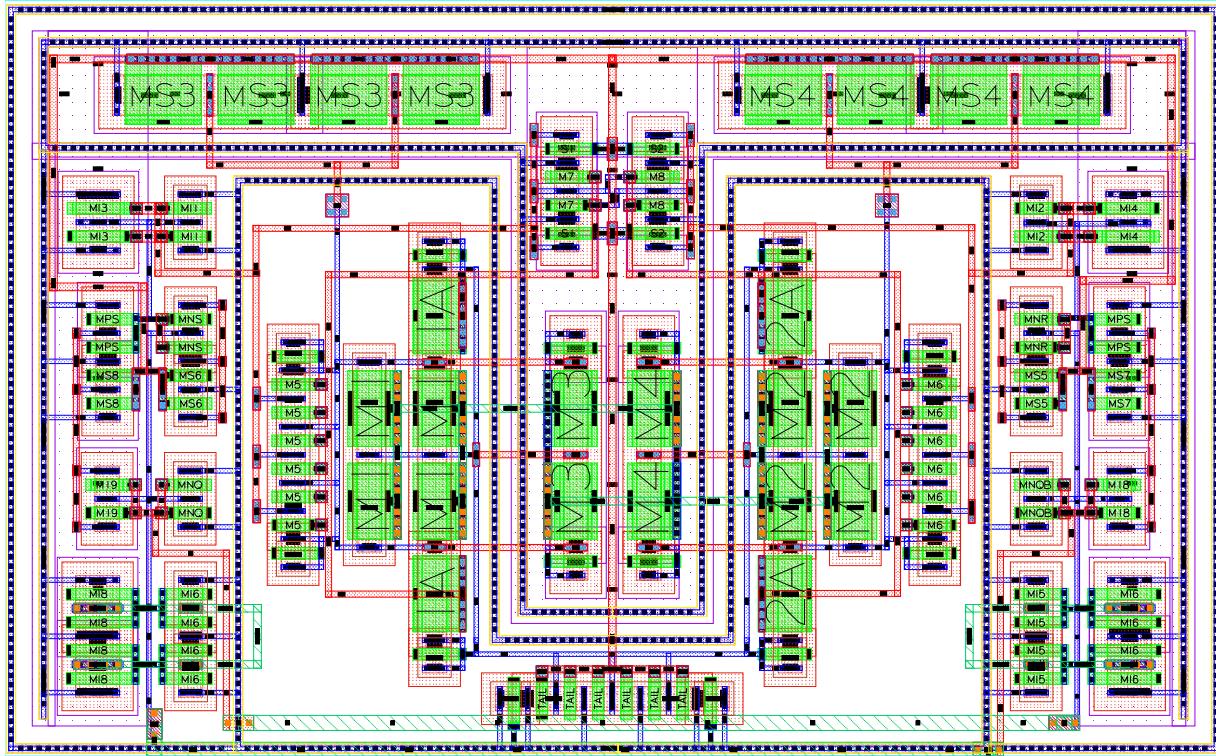


Figure 3.0.1: Comparator layout. The modified StrongArm buffer is centered, while the SR latch and buffer transistors are placed along the left and right sides.

Parameter	Units	Spec	Nominal	Min	Max
Hysteresis	mV	10-20	16.5203	16.3701	16.9196
Prop. Delay (1 pF)	ns	10	1.709	1.3403	2.6746
Prop. Delay (1 fF)	ps	-	558.45	344.51	915.93
DC Current	nA	minimize	0.36671	0.20815	9.5295
W/decision	pW	-	1.1326	0.5327	2.3975
ICMR	mV	-	-	-200	2200
Layout Area	μm^2	-	160	-	-

Table 3: Extracted corner results.

Parameter	Units	Mean	Min	Max	Std Dev
Hysteresis	mV	17.04	16.5334	33.1274	2.84316
Prop. Delay (1 pF)	ns	1.7592	1.7443	1.8072	0.010835

Table 4: Extracted monte carlo results.

the layout. These results are summarized in [Table 3](#).

Post-layout monte carlo simulation showed a 95% yield for 3σ variation, which was quite acceptable for this project's requirements. Results are summarized in [Table 4](#).

Waveforms for extracted simulations are shown in [Figs. 4.0.1 to 4.0.3](#).

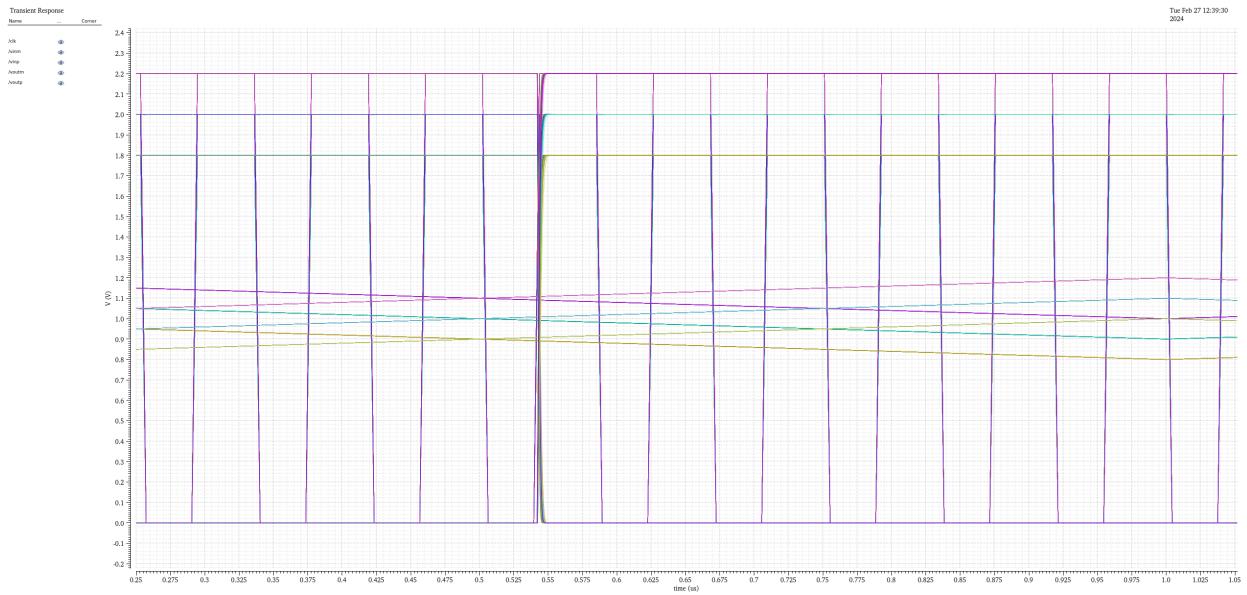


Figure 4.0.1: Extracted hysteresis waveform.

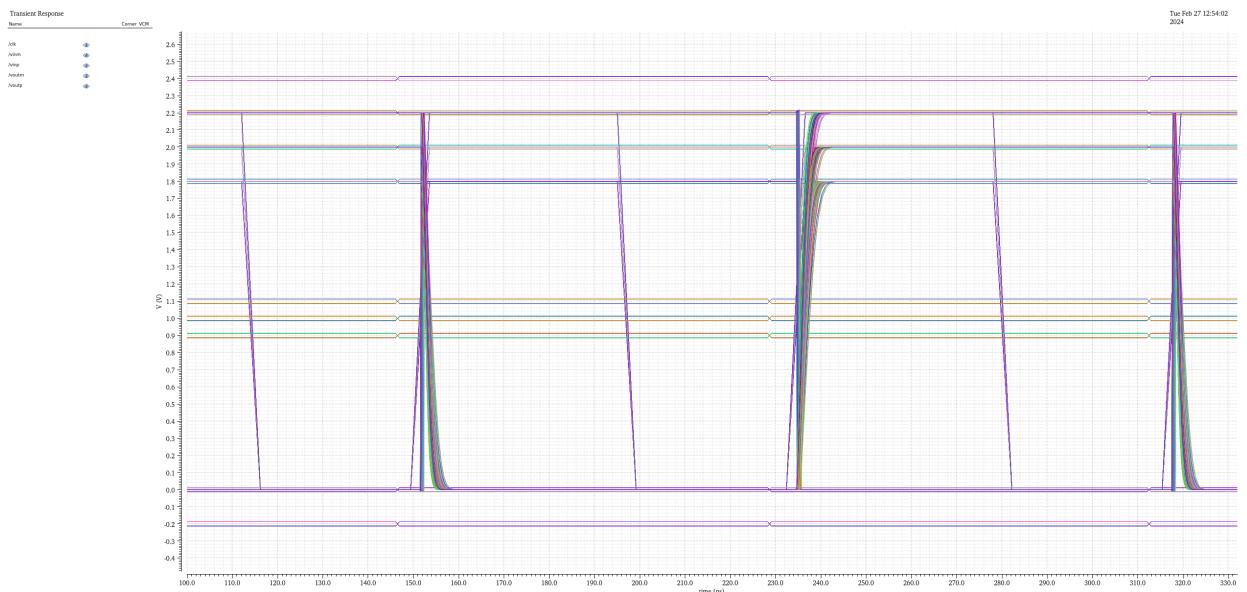


Figure 4.0.2: Extracted propagation delay waveform.

5 Conclusion

This comparator design met all design specifications across corners post-layout, exceeding initial expectations. Adding the additional capability to process signals up to and exceeding the supply rails does not seem to be a thoroughly researched area for dynamic comparators, but the results from this experiment are very promising. This will prove to be a fortuitous addition for subsequent lab exercises, where this comparator will be implemented in a flash ADC requiring processing at $\frac{VDD}{2^4}$ increments. This comparator can be employed for each voltage level instead of using separate NMOS

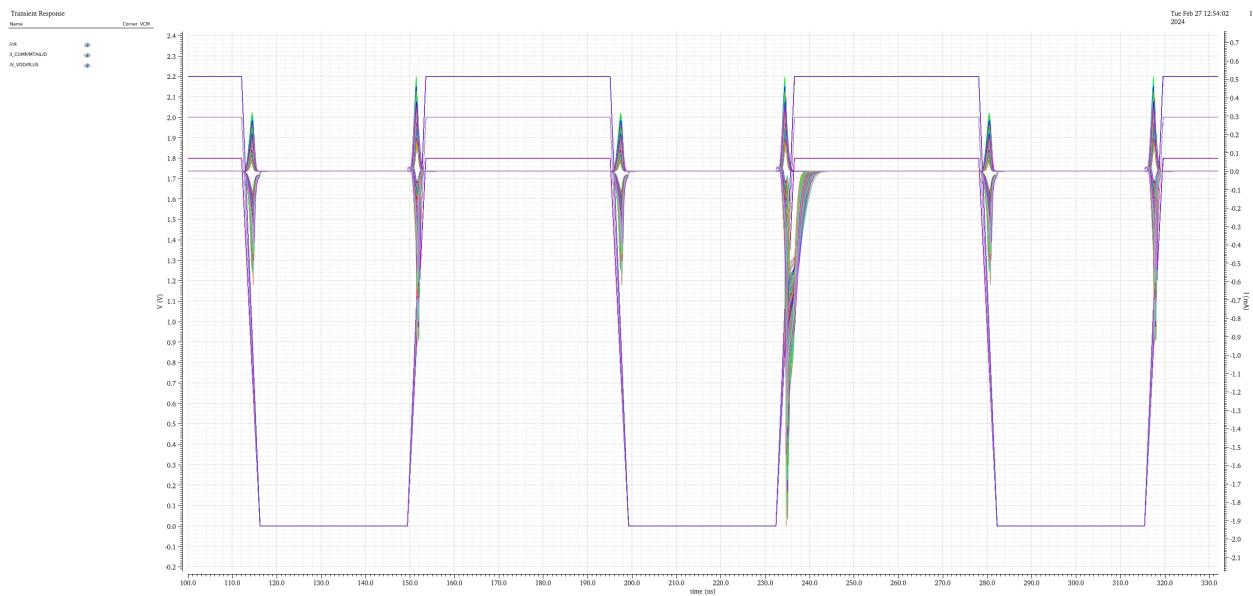


Figure 4.0.3: Extracted transient current draw waveform.

and PMOS input architectures, which should ensure better performance across the voltage range and from ADC to ADC.

References

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