

EEEE 726: Project 3

4-Bit StrongARM Flash ADC

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Subject: Project 3

Abstract

The purpose of this project is to design a flash ADC incorporating the previously designed comparator. The RTR StrongARM-based comparator is refined to enhance the performance in this application. A 4-bit design is chosen based on the requirement for <25 dB SQNR and each binary output is designed to drive a 1 pF capacitive load. This ADC has been tested to work in a rail-to-rail configuration with a reference voltage of 2 V, equal to the nominal supply voltage. In schematic-level simulations, a DNL of 20.848 mLSB, INL of 1.2009 mLSB, and propagation delay of 2.7531 ns are achieved at $V_{LSB_{eff}} = 133$ mV.

1 Design

The design of an N -bit flash ADC is geared toward brute-force comparison, where $N - 1$ comparators are biased at equal divisions within the range of the ADC reference voltage, such that if the input V_{in} to the positive input of each ADC is higher than the reference at its negative input, the comparator trips its output high. While this topology requires high power due to the quiescent draw of a reference generator for each comparator on top of the transient requirements of $N - 1$ comparators, it is robust and allows for very fast operation at 1 conversion per clock cycle.

1.1 SQNR

It is known that SQNR in an ADC system is a function of the bit depth of the ADC, since quantization noise is determined by the effective V_{LSB} , shown in Eq. (1.1.2).

$$\text{SQNR} = 20 \log\left(\frac{V_{in,rms}}{V_{Q,rms}}\right) , \quad V_{Q,rms} \triangleq \frac{V_{LSB}}{\sqrt{12}} \quad (1.1.1)$$

$$\text{SQNR} \approx 6.02N + 1.76 \text{ dB} \quad (1.1.2)$$

Thus, selecting $N = 4$ yields an $\text{SQNR} = 25.84 \text{ dB}$, satisfying the design requirement of 25 dB . While this figure has little margin, SQNR is only a function of fundamental design aspects of the ADC as shown and will not vary with environmental conditions like noise or even reference voltage ranges.

1.2 Top-Level

A basic resistor ladder configuration was adopted for this ADC design to divide the reference voltage into individual references for each comparator. The resistors are arranged in an $R : 2R : \dots : 2R : R$ configuration from top to bottom to divide the range into 2^N ranges with $2^N - 1$ voltages. Non-salicided p^+ polysilicon resistors are chosen for their high sheet resistance to minimize layout area and relatively low temperature coefficient, and dummy resistors are enabled for manufacturing. R for these resistors is selected to be 800Ω , which provides a balance of minimizing current draw from this stage and maintaining a reduced time constant when coupled with input capacitance of the comparators. This is necessary for kickback current noise that appears from the comparators – which couples through the parasitic capacitance at the inputs – to settle before their next sample. If the kickback voltage is significant compared to the voltage for each code, due to a high R value, this can result in glitches in the output. This can be characterized in the worst case by observing kickback at the middle of the ADC reference range, where the Thevenin equivalent resistance of the reference ladder is greatest and kickback will be worst. The downside to this configuration is that there is no way to correct for voltage variation that appears from variation in the global reference voltage, PVT variation, or process-induced mismatch; there is also no intrinsic kickback suppression, which is an important consideration when using dynamic comparators as proposed in this design. As such, a trade-off has to be struck between accuracy and preserving the low-power nature of the design provided by the comparator topology used. Fig. 1.2.1 shows the full top-level schematic of the flash ADC, which consists mainly of the resistor network, comparators, and a thermometer-to-binary encoder for digitizing the comparator outputs. Since the comparators are dynamic and do not require current biasing, the provided $10 \mu\text{A}$ reference current is not used. More discussion is included later in this report on the instances shown at the top left of Fig. 1.2.1.

1.3 Comparator

The StrongARM comparator employed in this ADC is designed to process rail-to-rail common mode signals, allowing the same exact comparator design to be used for every position. This avoids any mismatch in input capacitance throughout the range and should contribute toward gain linearity across the common mode range. The schematic design of this comparator has remained unchanged from Project 2, as shown in Fig. 1.3.1, but the layout has been reworked to simplify routing with the intent of reduced parasitics and decreased layout area, detailed later in this report.

The performance of the revised layout was verified through extracted simulations, and was found to work to the previous design specifications up to a speed of about 1.1 GHz . Above this speed, hysteresis began to rise to values greater than would have been acceptable for the ADC, as any amount of hysteresis contributes to nonlinearity of the flash ADC due to differences in rising and falling

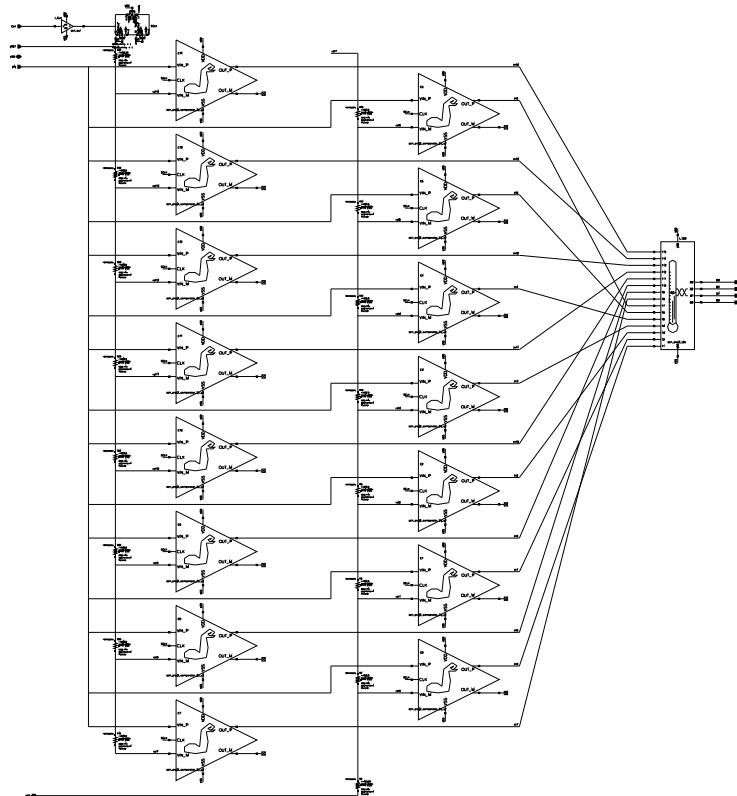


Figure 1.2.1: Top-level schematic of the flash ADC.

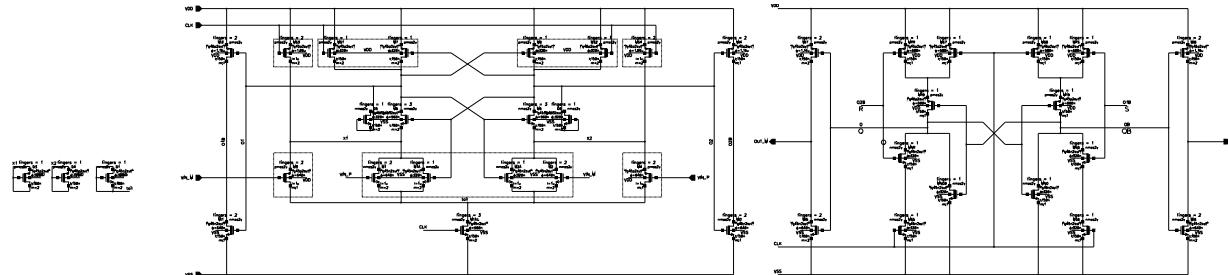


Figure 1.3.1: Schematic of the RTR StrongARM comparator as employed in this flash ADC design and its associated SR latch.

trip voltages. While not simulated with noise sources, less than 15 mV of hysteresis is designed into the comparator in extracted simulations at the provided clock speed of 12 MHz, providing a balance between linearity and stability with a noisy input source. Further reduction of hysteresis and increase of speed was found to be difficult due to the limits imposed by the use of the 2 V device in the gpdk_045, which have a minimum length of 180 nm and finger width of 320 nm. The performance is detailed in [Table 1](#).

1.3.1 Threshold Modification

Incidentally through some simulations, it was found that varying the input device sizes for this comparator design yielded control over the trip voltage, and this could be exploited to achieve adjustment

Parameter	Units	Nominal
Hysteresis	mV	14.64
Prop. Delay (1 pF)	ns	1.5778
Prop. Delay (1 fF)	ps	414.07
DC Current	nA	1.2868
W/decision	pW	1.067
Layout Area	μm^2	119.79

Table 1: Comparator performance with extracted parasitics from layout.

over the entire supply range. With this in mind, tuning different comparator design was explored as a possibility to create a flash ADC without the use of a resistor biasing string, creating an ultra low power and layout area design. Simulations were run to determine the trip voltage for some initial coarse device sizing, with the intent of producing an experimental curve to further refine the choice of sizes. While sizing to process the entire lower half of the input range was achieved, the relationship to trip voltage was found to be very nonlinear, which would likely negatively impact mismatch results and could have other implications. This method would have also presented different input capacitances at each level of the input range, which may introduce nonlinearity as well. While this idea may still benefit from some future work, the time dedication did not fit within the scope of this project and the previously mentioned reference generation scheme was used.

1.4 Encoder

Some form of encoder subsystem is necessary in the flash ADC to translate the “thermometer”-coded output of the 15 comparators into 4-bit binary. Various methods have been explored in industry and literature, including Wallace tree, Fat-tree, ROM, and MUX based designs. Other algorithms sometimes perform a conversion to gray code before binary to provide robustness against “bubble errors” caused by a comparator improperly evaluating as 0 below one that has evaluated as 1. Additional logic to perform this correction can also be added onto the other encoding methods as well. A MUX-based “priority” encoder design based on [1] is used for its low-power operation and high speed at the cost of high device count, shown in Fig. 1.4.1. No bubble correction was implemented in this design, as the low bit-depth of this ADC compared with the resolving capability of the comparators used should additional power savings and reduction in the number of required devices is provided through the use of transmission gate-based MUXs shown in Fig. 1.4.2, which use half the number of devices as active CMOS multiplexers. To provide delay time correction for the MSBs of the encoder, additional self-selected MUXs are added to each to match the critical path for the LSB. This minimizes glitches due to different bit arrival times and the self-selecting MUXs should add enough consecutive delay to allow the LSB to arrive first, minimizing the magnitude if a glitch occurs. The additional devices needed to provide this functionality are not viewed as a significant penalty due to the device savings from using TG MUXs.

2 Schematic Level Simulations

Schematic simulations were performed over PVT corners and monte carlo analysis. The process corners used were tt, ss, sf, fs, and ff, temperatures of 0, 27, 40, and 85 °C, and supply voltages of 1.8, 2.0, and 2.2 V. The schematic was captured and simulated using Cadence Virtuoso.

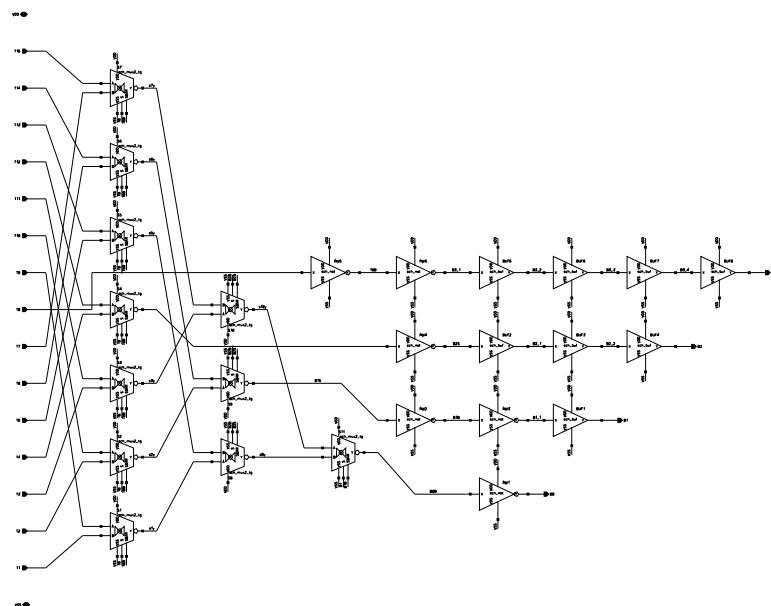


Figure 1.4.1: Schematic view of encoder design.

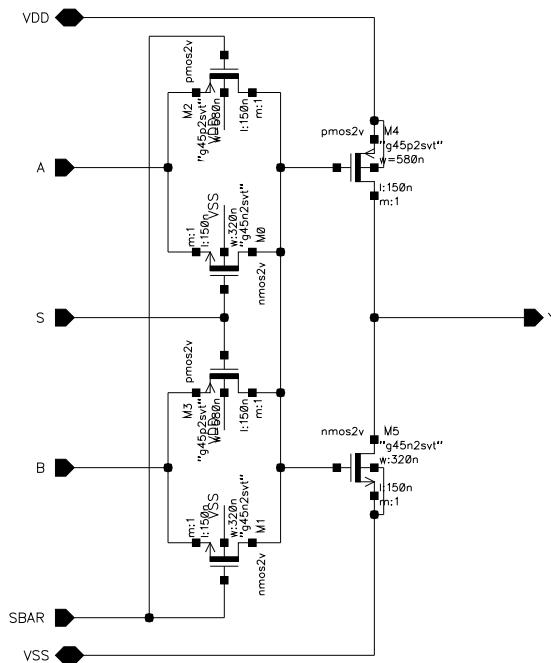


Figure 1.4.2: Schematic of transmission-gate based MUX that provides the functionality of the proposed encoder design. The outputs are inverted for logic purposes and increased drive strength.

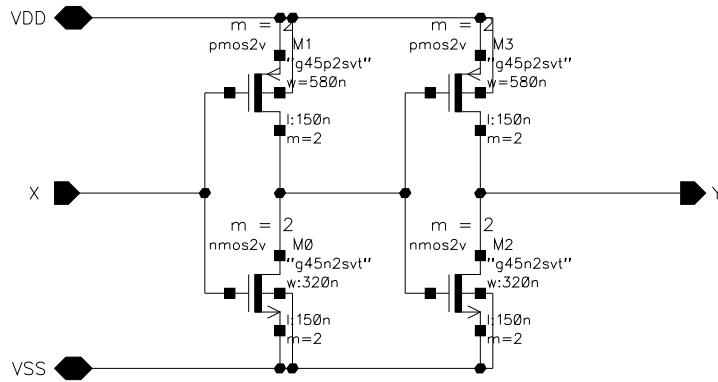


Figure 1.4.3: Schematic of buffer highlighting device sizes, which are also used in the inverter design.

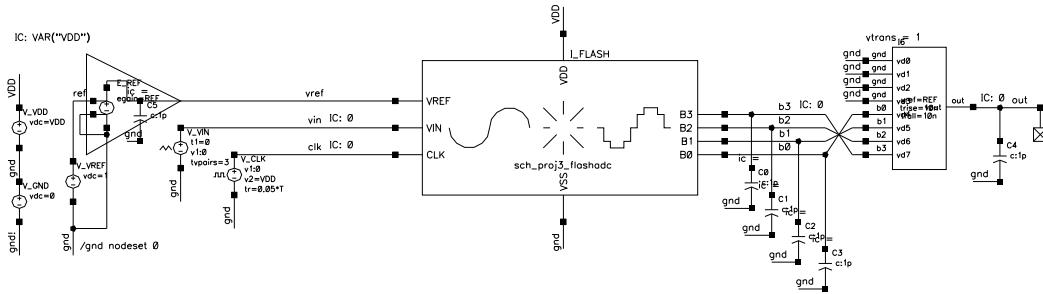


Figure 2.1.1: Testbench setup used for INL and DNL analysis.

2.1 INL and DNL Testbench

A simple testbench schematic was set up for the flash ADC as shown in Fig. 2.1.1. The local ground for this design is decoupled from the global ground using a 0 V source, and currently a VCVS is used to increase the given reference voltage of 1 V up to 2 V for testing rail-to-rail operation. In a full system, a reference voltage at the power supply would likely need to be supplied by an LDO and possibly assisted by a charge pump. The supplied 12 MHz clock is realized by a pulse source with 5% rise and fall times, and the input triangle ramp is supplied by a piecewise-linear source.

For the voltage reference, a 1 V DC supply is used as a given reference per design specifications. To enable testing at a reference of 2 V to evaluate rail-to-rail operation, a vcvx was used to step up the voltage. This was done under the assumption that a stable reference is being provided

Each output bit from the encoder drives a 1 pF load as specified, and are also sent into an ideal 8-bit DAC provided by the *ahdLib*. This DAC is intended to translate the binary ADC output into a stepped ramp output for comparison with the ideal stepped ramp output with idealized trip voltages. Once normalized for any gain and offset error using the first and last transitions to find a $V_{LSB_{eff}}$, the difference in code widths for the output of the ADC compared to the ideal version defined by variables in the ADE Assembler Environment allows for quantification of differential nonlinearity (DNL). The summation of these differences across the range provides the integral nonlinearity (INL). This simulation setup provides a similar feel to evaluating these specifications for a continuous time comparator, but instead of the precision being defined by the number of voltage steps per digital code, it is defined by the number of clock cycles per code. Therefore, the testbench setups were completely parametrized around this figure to allow for quick changes if necessary.

The achieved results for INL and DNL at typical corner are shown in ???. $V_{LSB_{eff}}$ was calculated to be 133 mV.

Test	Output	Spec	Weight	Pass/Fail	Min	Max	TYP
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
TB_FLASH	/vin						
TB_FLASH	/b0						
TB_FLASH	/b1						
TB_FLASH	/b2						
TB_FLASH	/b3						
TB_FLASH	/out						
TB_FLASH	/vref						
TB_FLASH	bin1				-2.02 mLSB	-2.02 mLSB	-2.02 mLSB
TB_FLASH	bin2				7.4 mLSB	7.4 mLSB	7.4 mLSB
TB_FLASH	bin3				7.4 mLSB	7.4 mLSB	7.4 mLSB
TB_FLASH	bin4				-20.8 mLSB	-20.8 mLSB	-20.8 mLSB
TB_FLASH	bin5				-11.4 mLSB	-11.4 mLSB	-11.4 mLSB
TB_FLASH	bin6				-2.02 mLSB	-2.02 mLSB	-2.02 mLSB
TB_FLASH	bin7				-2.02 mLSB	-2.02 mLSB	-2.02 mLSB
TB_FLASH	bin8				7.4 mLSB	7.4 mLSB	7.4 mLSB
TB_FLASH	bin9				-11.4 mLSB	-11.4 mLSB	-11.4 mLSB
TB_FLASH	bin10				-2.02 mLSB	-2.02 mLSB	-2.02 mLSB
TB_FLASH	bin11				-2.02 mLSB	-2.02 mLSB	-2.02 mLSB
TB_FLASH	bin12				7.4 mLSB	7.4 mLSB	7.4 mLSB
TB_FLASH	bin13				7.4 mLSB	7.4 mLSB	7.4 mLSB
TB_FLASH	bin14				16.8 mLSB	16.8 mLSB	16.8 mLSB
TB_FLASH	bin15				16.8 mLSB	16.8 mLSB	16.8 mLSB
TB_FLASH	DNL	< 0.5		pass	20.848 mLSB	20.848 mLSB	20.848 mLSB
TB_FLASH	INL	< 1		pass	1.2009 mLSB	1.2009 mLSB	1.2009 mLSB

Figure 2.1.2: INL and DNL results at typical.

2.2 Propagation Delay Testbench

To analyze propagation delay, the same testbench setup was used but with a modified PWL input to step nearly instantaneously right before each evaluation at the clock rise. This was intended to have all the comparators slam high or low at once, and the last output bit to fall into place was measured for propagation delay. The outputs were evaluated at both rising and falling inputs, and the maximum time for any of the bits to transition was measured, giving a worst-case delay figure. The results are shown in ??.

Test	Output	Spec	Weight	Pass/Fail	Min	Max	TYP
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
TB_PROP	/vin						
TB_PROP	/clk						
TB_PROP	/b0						
TB_PROP	/b1						
TB_PROP	/b2						
TB_PROP	/b3						
TB_PROP	/out						
TB_PROP	t1_rise				22.916 ns	22.916 ns	22.916 ns
TB_PROP	t2_rise				25.669 ns	25.669 ns	25.669 ns
TB_PROP	tp_rise	< 30n		pass	2.7531 ns	2.7531 ns	2.7531 ns

Figure 2.2.1: Propagation delay results at typical.

2.3 Issues Faced

Simulating the performance of this ADC design proved to be a significant challenge from both the standpoint of computational intensity and unexpected inconsistencies from one run to the next. Testing was initially performed using only a single defined TYP corner, due to the simulation time needed to see the effect of changes made to the design. To aid the solutions, initial conditions and node-set values were provided for appropriate top-level nodes for transient and DC simulations to use respectively. Pivoting was enabled for DC simulations using the gear2 method. Initially, Spectre APS was used with `++aps` enabled and conservative error preset for both testbenches, and then an explicit `+mt=8` was added. For the propagation delay analysis, sometime during testing, the comparator outputs all began solving improperly, rising at the beginning of the simulation before

the first clock edge. It was found that disabling `++aps` resolved this issue. (Further discussion with classmates provided insight that it may be beneficial to enable options in Spectre to explicitly prevent it from using prior run data to inform the solution of the current run, which may have effectively been what happened by changing the simulator settings here.) Using Spectre X with AX preset, AX parasitic optimization, and 8 threads decreased the INL/DNL testbench simulation time from 4:15 min to 2:30 min with no apparent change in accuracy, so this was implemented for the final results. For the INL/DNL testbench, MS simulation was also enabled with the encoder selected as a digital instance and the comparators and clock buffer selected as analog instances; the propagation delay testbench remained with MS simulation disabled. While the 21.3 version of Spectre used offers massively parallel GPU simulation capability, the license available does not have access to this feature.

Monte carlo simulations also proved to be a sticking point, and at the point of writing it is still unclear if the results obtained for DNL in these simulations are accurate, both due to the low LSB precision and number of monte carlo points required to complete any simulations before the submission was due, and the large disparity in yield with the comparator results, which makes up the bulk of the devices in the ADC.

The stated simulation times are for 10 clock cycles per digital code, giving a maximum evaluation precision of 0.1 LSB. To truly quantify the performance of the ADC itself, a precision of 1 mLSB was desired, but this did increase the simulation time for each test tenfold. As such, a balance between quantifying performance and quantifying the design's ability to meet specifications had to be struck, and the accuracy for the results will be noted.

At some point during testing, tests were rerun after reopening Cadence and the INL/DNL testbench results were much worse than before. DNL has increased from around 20 mLSB to well over 1 LSB and INL increased from around 8 mLSB to around 100 mLSB. At this point, 13 k Ω resistors were being used for power savings. It is believed that something changed in the evaluation of the kickback voltage presented at each comparator's reference input, as it was eventually found that decreasing the resistor ladder values provided small improvements to INL and DNL; this change would have reduced the discharge time constant at the nodes through the overall reduced Thevenin equivalent resistance, providing less of a severe impact on the transition voltages. Something of note is that this was most severely affecting the bottom of the range, whereas the worst reference disturbance would be expected to be in the middle where the Thevenin resistance would be highest. While the root cause of the new disappointing results could not be determined, further reduction of the resistor values did improve INL and DNL values to acceptable levels.

To further reduce nonlinearity to meet spec by a reduction of kickback, a quasi-adiabatic drive system was constructed. This involves simply adding an RC time constant to the local clock line to reduce the slew rate of the clock signal; a more slowly ramping clock reduces kickback since the current noise coupled back to the comparator input is related to the discharge rate of the StrongARM's internal nodes, as shown in Eq. (2.3.1), where dV_A is the time-varying voltage at the sources of the input transistors and dV_P is the time-varying voltage at the drains [2].

$$I_{kickback} = -\left(\frac{2}{3}WL C_{ox} + C_{GS_{tot}} \frac{dV_A(t)}{dt} - C_{GS_{tot}} \frac{dV_P(t)}{dt}\right) \quad (2.3.1)$$

Also shown by this relationship, kickback is increased in the comparators used due to both the large minimum size of the 2 V transistors used and the inclusion of parallel NMOS and PMOS input devices for RTR operation.

Parameter	Units	Max	Nominal	Min
DNL	mLSB	4821.7	153.8	60.21
INL	mLSB	16.009	9.2979	2.3985
Max Prop. Delay	ns	13.253	7.4131	5.7102
Timing difference	ps	213.44	148.72	18.045
Reference DC Current	μ A	192.95	148.72	123.55
Max Transient Current	mA	15.358	8.4772	3.502
W/conversion	pW	101.38	63.452	37.654

Table 2: Flash ADC performance results across PVT corners, with a precision of 10 mLSB for DNL and INL measurements.

The quasi-adiabatic drive is implemented in this design by employing a transmission gate to provide separately tunable effective resistance for both clock edges, which couples with the input capacitance of the comparators to round off the rising and falling edges of the clock. Since kickback noise generated on the falling clock edge does not impact the comparator evaluation, as long as the fluctuation does not last until the rising edge of the clock, a smaller NNOS device is used, while 640 nm length PMOS devices are used to round the clock more. A local clock buffer is provided to decouple the transmission gate from the ideal clock source used, and is beneficial to have in the final ADC layout; these are shown in the top left of Fig. 1.2.1. While the use of metal resistors would provide better uniformity across corners, the transmission gate structure offers beneficial dynamic response for this circuit, and additional variation robustness can be provided by increasing the size of these devices. Another important consideration is that this approach makes the comparator decision more and more asynchronous with the system clock as more smoothing is designed, causing an effective increase in propagation delay.

Some other ideas were investigated to reduce the kickback voltage, such as increasing the capacitance at each of the reference steps and even instantiating an inductor on the reference line for the middle comparator, to function as a choke where the kickback is greatest. While the capacitances were not enough to provide significant benefit, the inductor performed surprisingly well initial simulations, bringing INL and DNL below measurement precision instantly. Across corners, however, a sinusoidal-shaped output plot in the codes surrounding the middle reference began to appear, suggesting that the choke began to act more like a tuning fork. Combined with the comically large size of the inductor pcells and the added manufacturing cost of the top metal layers needed, this solution provided little benefit for real implementation.

2.4 Schematic Level Results

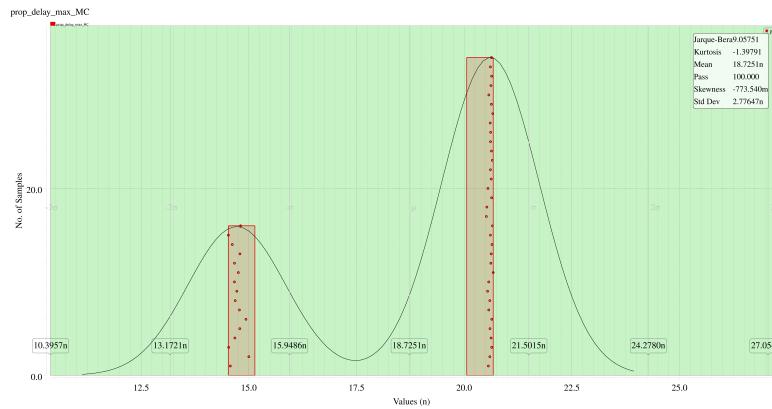
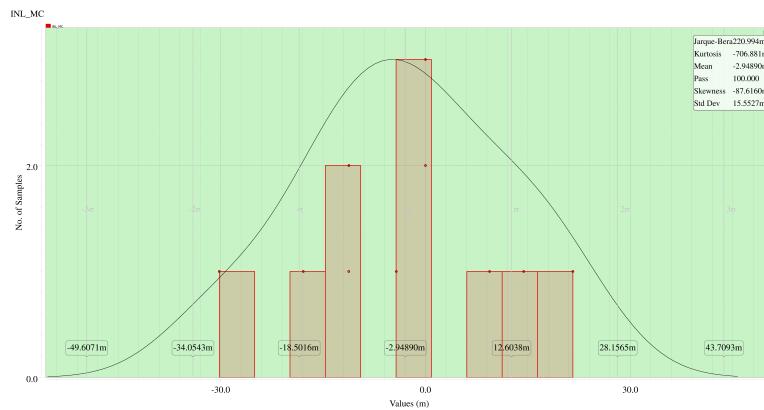
The ADC design passed the 30 ps propagation delay and 1 LSB INL specifications with flying colors across corners, and passed the 500 mLSB DNL in 50/60 corners for the given 1 V reference. This is most likely due to some more kickback suppression needed to account for the worst corners as these failures all occur at low supply voltages, with the worst DNL occurring always in the middle of the range. A solution was not able to be implemented at the time of writing due to the issues faced and time needed to wait for the simulations to run. The results captured in Table 2 are obtained with 10 clocks per code giving a precision of 100 mLSB, and should not be taken as a quantitative maximum performance evaluation of the ADC. A simulation was run at the typical corner with 1000 clocks per code, to hopefully get a sense of the true performance of the ADC, which may be cautiously extrapolated across the corner results; this is presented in Table 3.

Parameter	Units	Nominal
DNL	mLSB	115.61
INL	mLSB	7.2199
$V_{LSB_{eff}}$	mV	66.4

Table 3: Flash ADC DNL & INL results at the typical corner, with a precision of 1 mLSB.

Interestingly, the worst codes for DNL in this simulation are at the extents of the reference range, with single-digit mLSB DNL seen in the middle of the range.

Monte carlo simulations for this design are unknown to be properly simulated. Propagation delay resulted in a 100% yield over 3σ variation, but the histogram shown in Fig. 2.4.1 has a very unusual distribution characteristic. Nonlinearity testing had to be conducted with fewer points, and INL testing produced 100% yield with a more normal histogram shown in Fig. 2.4.2. DNL measurements produced no usable results with only quantities in aLSB or around 12-14 LSB given. This gives pause as to the validity of the INL measurements as well, due to its reliance on properly evaluated DNL.

**Figure 2.4.1:** Propagation delay monte carlo histogram.**Figure 2.4.2:** Integral nonlinearity monte carlo histogram.

A sensitivity analysis was run over the course of a day to see if a trend could be found in what contributed to the spread of DNL measurements, but the results from this were unclear as well. Shown in Fig. 2.4.3, no device had considerable contribution to DNL variation in the entire design.

This is somewhat expected due to the sheer number of devices in the design; however, no pattern is observed in the top contributors either. It was expected to see a consistent device within all of the comparators contributing mostly to DNL variation, but this was very much not the case. Further investigation into this issue is needed to quantify the design's performance under mismatch.

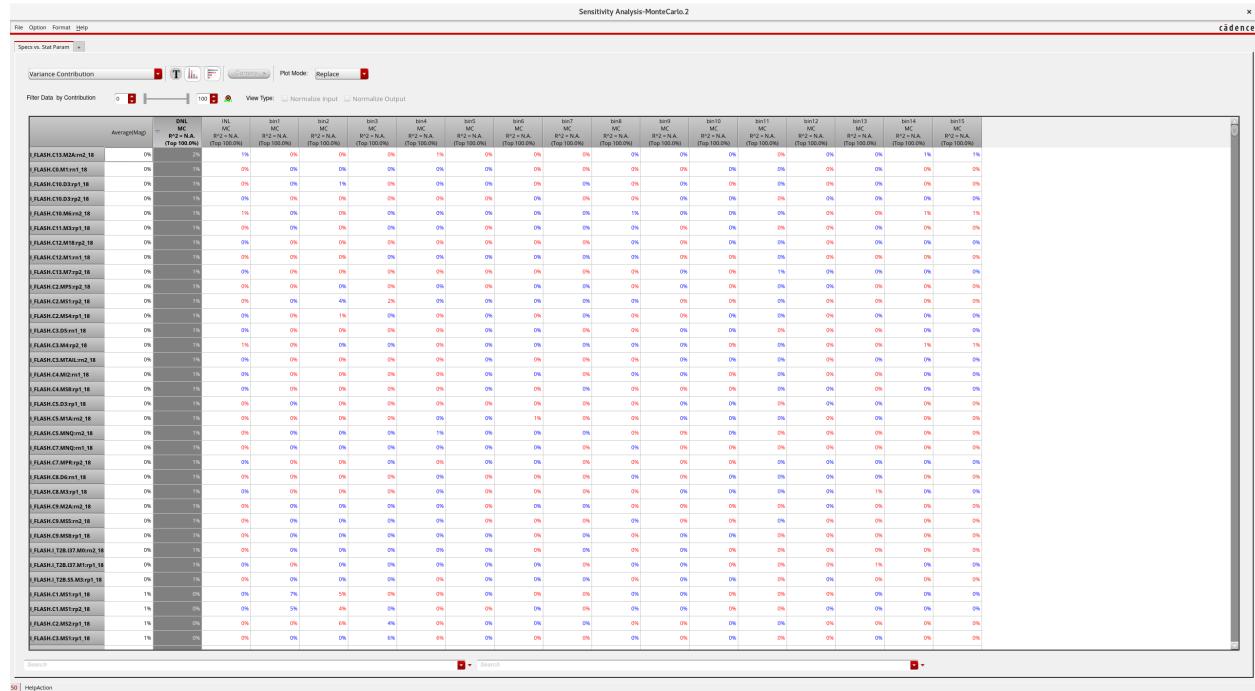


Figure 2.4.3: Sensitivity analysis results ordered in highest contribution to DNL variation.

3 Layout

The first layout completed for this design was the comparator shown in Fig. 3.0.1, since this had to be modified and then verified as it is the center of the ADC operation. Moving the large PMOS switches to the center of this design now line up their drain routing with the input transistors, which greatly simplifies much of the overall routing of this design. This also further increases the symmetry of the overall layout, and should enhance the matching of the input transistors as well. Cross-coupled devices M5 and M6, and the other PMOS switches are now also split and common-centroided alongside the input devices. The majority of the internal guard rings are removed, to allow for tighter spacing between the NMOS and PMOS devices. Metal 4 is used for connections external to the comparator, which allows for routing a few more long-range connections on Metal 3 to reduce capacitance to other signals.

After this, the low-level digital blocks needed were laid out, with a design that enables them to be instantiated as a long row in the upper level layout to allow for simpler power rail routing, shown in Fig. 3.0.2.

With the MUXs and inverters completed, the full layout of the encoder was completed. The design takes advantage of the rail configuration of the digital blocks, and is completed in two horizontal rows, with power rails on the sides and in the middle. The auto-routing feature within Cadence Virtuoso was employed to route this block for time considerations, since the digital circuitry is more

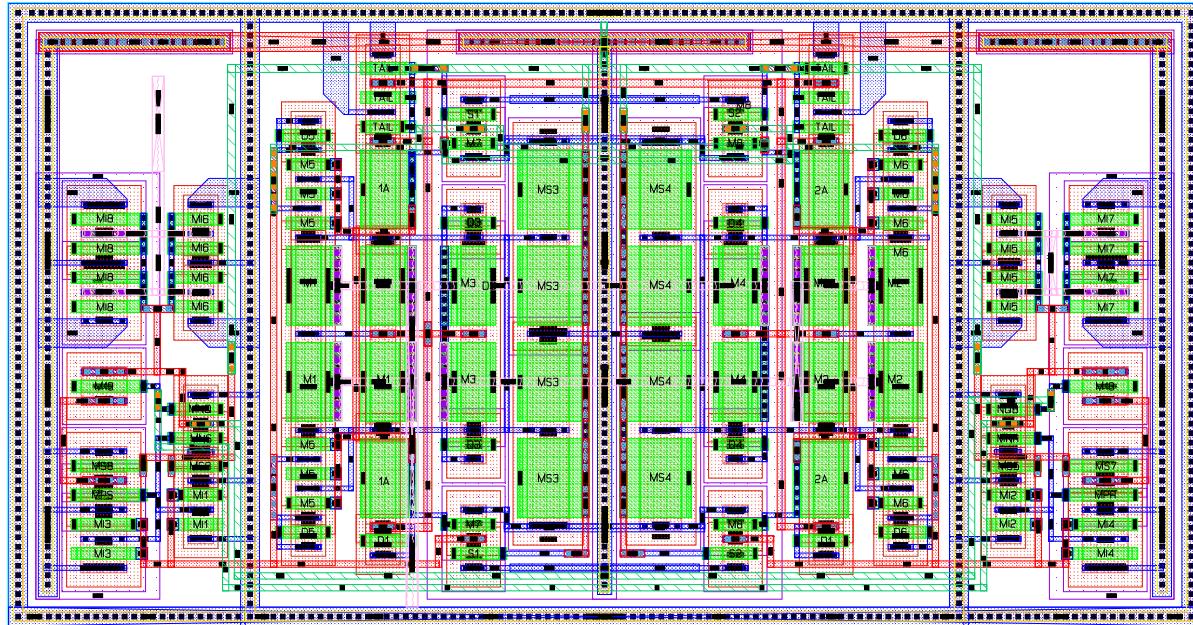


Figure 3.0.1: Comparator layout, version 2.

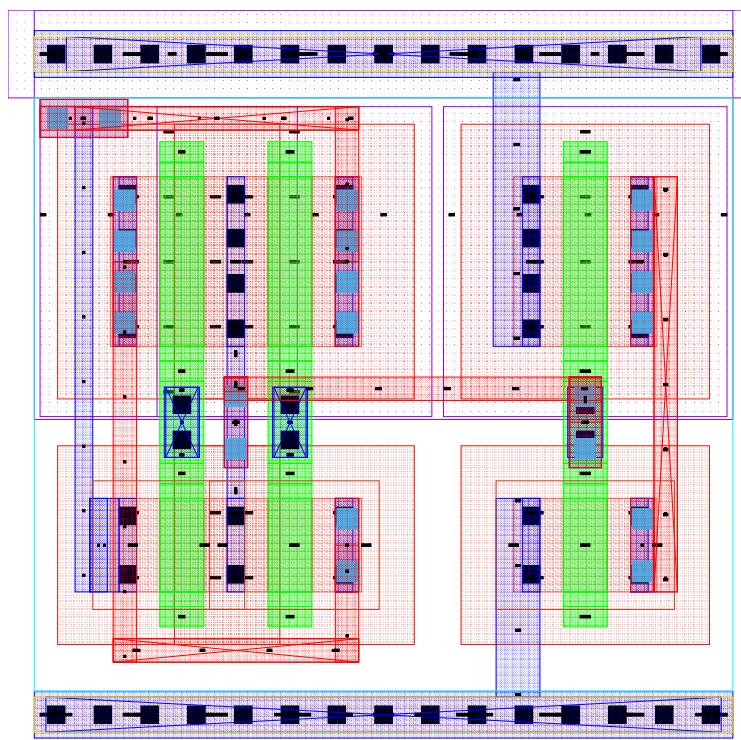


Figure 3.0.2: Transmission gate MUX2 with inverter layout.

immune to routing decisions made by an algorithm such as this. Routing was allowed on metals 2 to 4 with 2 and 3 preferred, and was done using the ASIC preset. The results are shown in [Fig. 3.0.3](#).

The overall comparator layout began with floor plan to have two columns of comparators with re-

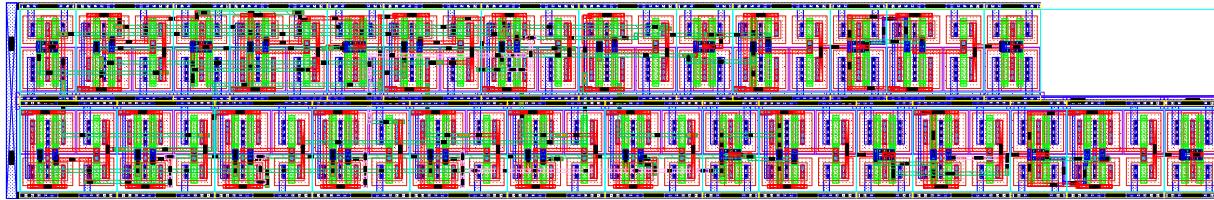


Figure 3.0.3: Thermometer to binary encoder layout.

sistors located in the middle, to ensure better matching between the resistors which is critical for the flash topology. Due to the short nature of the encoder block, it could be placed within the space left due to having 15 comparators, and the adiabatic drive devices could find a home in the middle.

Routing of the full ADC was done by hand to ensure symmetry, and once all signals were routed the clock line to all of the comparators was auto-routed using the same settings as before. VDD and VSS lines to the comparators were overlapped as much as possible on metals 1 and 2 to provide as much capacitance as could be easily obtained. The final result is shown in Fig. 3.0.4. The final ADC layout size is $59.25 \mu\text{m}$ by $68.265 \mu\text{m}$ for a total area of $4044 \mu\text{m}^2$. Both DRV and LVS evaluated clean on this layout.

4 Extracted Results

At the time of writing, extracted simulations have not been run across corners due to the simulation time required and a desire to iron out more of the simulation tool kinks before doing so.

5 Conclusion

A lot has been learned through the completion of this project, both about the creation of a flash ADC and about simulation and verification of mixed signal circuit designs. The simulation tools have definitely shown their learning curve, and a lot of new approaches had to be explored due to this non-traditional design with dynamic comparators. The ADC design itself was mostly successful, and there is a clear path to be taken to resolve the operation at failed PVT corners. The monte carlo results are less clear, and more investigation is needed to see if the results are valid or what can be done to improve their evaluation.

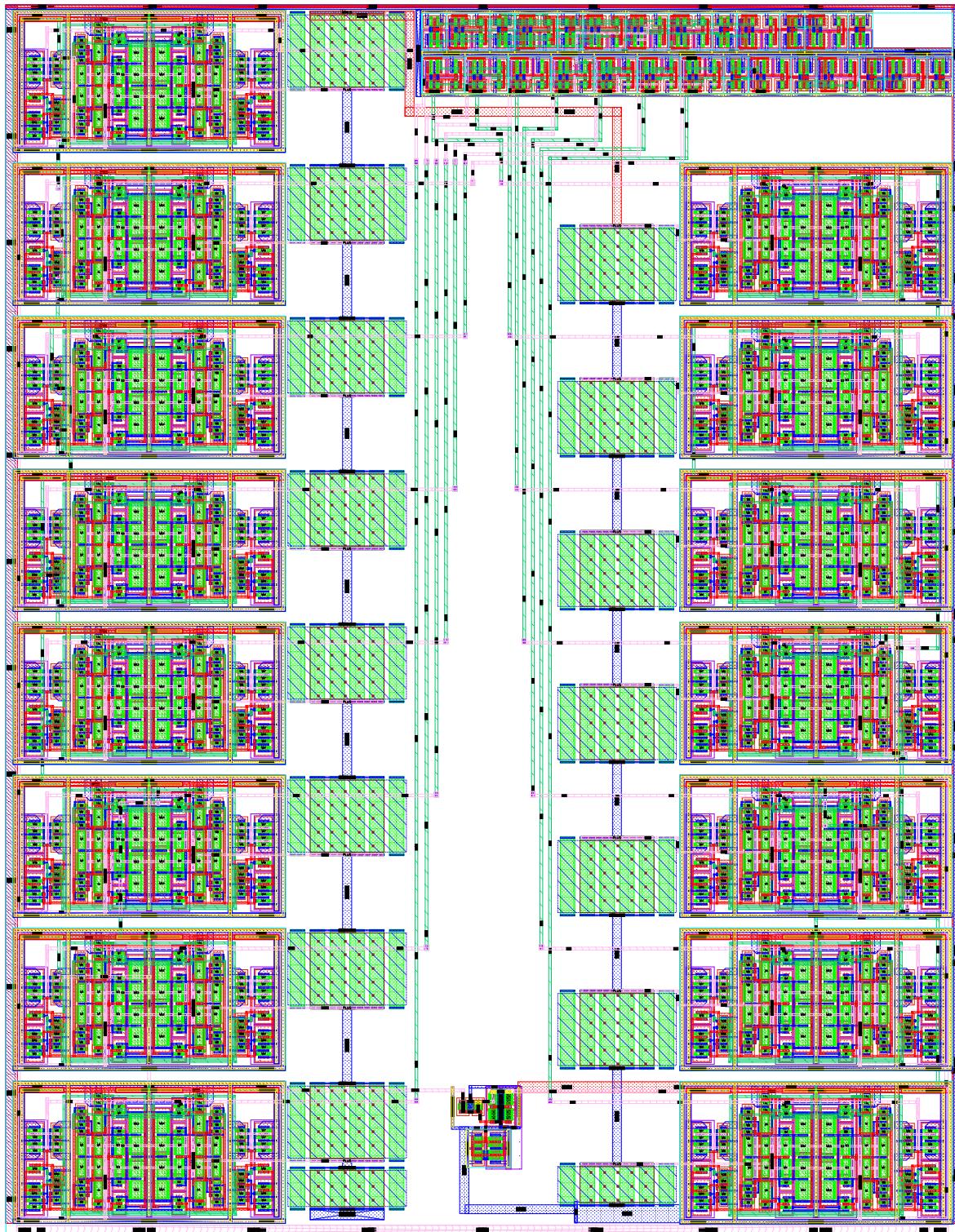


Figure 3.0.4: Full flash ADC layout.

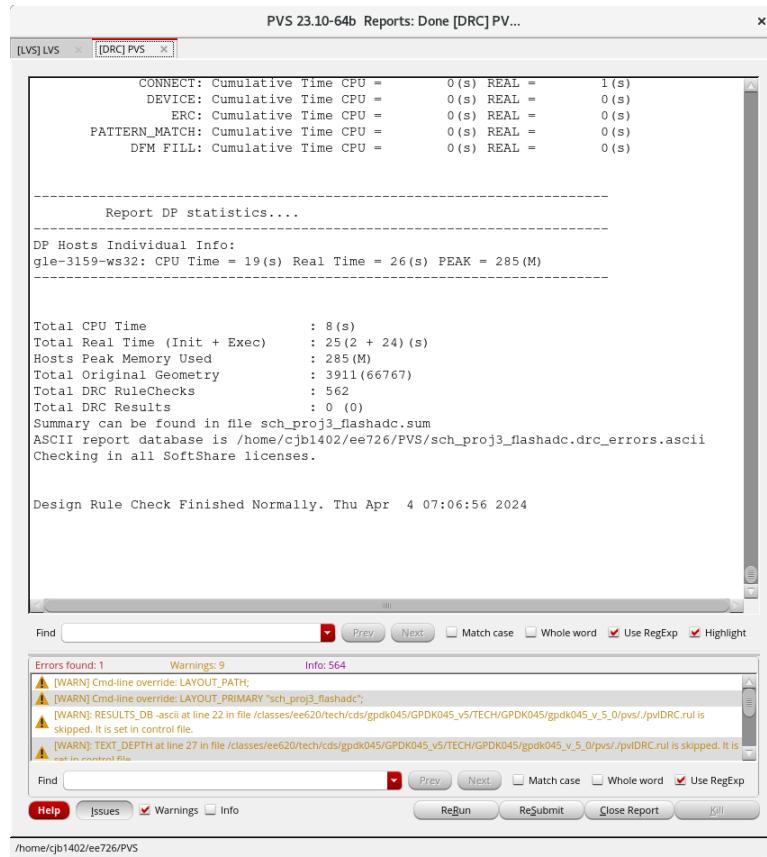
References

- [1] E. Säll and M. Vesterbacka, "Thermometer-to-binary decoders for flash analog-to-digital converters," *European Conference on Circuit Theory and Design 2007, ECCTD 2007*, pp. 240–243, 2007.

doi: [10.1109/ECCTD.2007.4529581](https://doi.org/10.1109/ECCTD.2007.4529581)

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Appendix



PVS 23.10-64b Reports: Done [DRC] PV...

[LVS] LVS [DRC] PVS

```

CONNECT: Cumulative Time CPU = 0(s) REAL = 1(s)
DEVICE: Cumulative Time CPU = 0(s) REAL = 0(s)
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)

-----
Report DP statistics...
-----
DP Hosts Individual Info:
gle-3159-ws32: CPU Time = 19(s) Real Time = 26(s) PEAK = 285(M)

Total CPU Time : 8(s)
Total Real Time (Init + Exec) : 25(2 + 24)(s)
Hosts Peak Memory Used : 285(M)
Total Original Geometry : 3911(66767)
Total DRC Rulechecks : 562
Total DRC Results : 0 (0)
Summary can be found in file sch_proj3_flashadc.sum
ASCII report database is /home/cjb1402/ee726/PVS/sch_proj3_flashadc.drc_errors.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Thu Apr 4 07:06:56 2024

```

Find Prev Next Match case Whole word Use RegExp Highlight

Errors found: 1 Warnings: 9 Info: 564

- ▲ [WARN] Cmd-line override: LAYOUT_PATH;
- ▲ [WARN] Cmd-line override: LAYOUT_PRIMARY "sch_proj3_flashadc";
- ▲ [WARN]: RESULTS_DB_ascii at line 22 in file /classes/ee620/tech/cds/gpdk045/GPDK045_v5/TECH/GPDK045/gpdk045_v_5_0/pvs/.pviDRC.rul is skipped. It is set in control file.
- ▲ [WARN]: TEXT_DEPTH at line 27 in file /classes/ee620/tech/cds/gpdk045/GPDK045_v5/TECH/GPDK045/gpdk045_v_5_0/pvs/.pviDRCrul is skipped. It is set in control file.

Find Prev Next Match case Whole word Use RegExp

Help Issues Warnings Info ReRun ReSubmit Close Report Kill

/home/cjb1402/ee726/PVS

Figure 5.0.1: DRC results.



Figure 5.0.2: The Holy Grail.