RIT | Kate Gleason College of Engineering

EEEE 726: Project 3
4-Bit StrongARM Flash ADC

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Abstract

The purpose of this project is to design a flash ADC incorporating the previously designed comparator. The RTR StrongARM-based comparator is refined to enhance the performance in this application. A 4-bit design is chosen based on the requirement for <25 dB SQNR and each binary output is designed to drive a 1 pF capacitive load. This ADC has been tested to work in a rail-to-rail configuration with a reference voltage of 2 V, equal to the nominal supply voltage. In schematic-level simulations, a DNL of 20.848 mLSB, INL of 1.2009 mLSB, and propagation delay of 2.7531 ns are achieved at $V_{LSB_{eff}} = 133$ mV.

1 Design

1.1 SQNR

It is known that SQNR in an ADC system is a function of the bit depth of the ADC, since quantization noise is determined by the effective V_{LSB}, shown in Eq. (1.1.2).

$$\text{SQNR} = 20\log\left(\frac{V_{in,rms}}{V_{Q,rms}}\right) \quad , \quad V_{Q,rms} \triangleq \frac{V_{LSB}}{\sqrt{12}} \tag{1.1.1}$$

$$\text{SQNR} \approx 6.02\,N + 1.76\,\text{dB} \tag{1.1.2}$$

Thus, selecting $N = 4$ yields an SQNR = 25.84 dB, satisfying the design requirement of 25 dB. While this figure has little margin, SQNR is only a function of fundamental design aspects of the ADC as shown and will not vary with environmental conditions like noise or even reference voltage ranges.

1.2 Top-Level

A standard resistor ladder was adopted for this ADC design to divide the reference voltage into individual references for each comparator's negative input. The resistors are arranged in an R : 2R ⋯ 2R : R configuration from top to bottom to divide the range into 2^N ranges with 2^N-1 voltages. The values of these resistors are selected to be 13 kΩ, which provides a balance of minimizing current draw from this stage and maintaining a reduced time constant when in parallel with input capacitances of the comparators. This is necessary for kickback noise that appears from the latched comparators to settle before their next sample. If the kickback voltage is significant compared to the voltage for each code, this can result in glitches in the output. Fig. 1.2.1 shows the full top-level schematic of the flash ADC, which consists mainly of the resistor network, comparators, and a thermometer-to-binary encoder for digitizing the comparator outputs. The resistor network shows 2 parallel resistors for matching purposes and dummy resistors provided on the sides for yield in manufacturing.

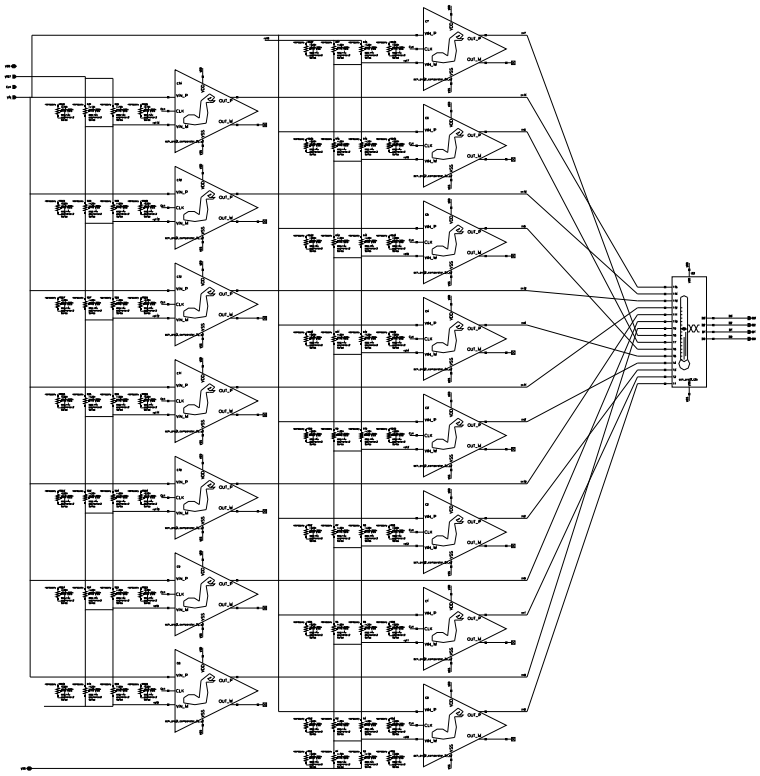

Figure 1.2.1: Top-level schematic of the flash ADC.

The StrongARM comparator employed in this ADC is designed to process rail-to-rail common mode signals, allowing the same exact comparator design to be used for every position. This avoids any mismatch in input capacitance and should contribute toward gain linearity across the common mode range.

1.3 Encoder

Some form of encoder subsystem is necessary in the flash ADC to translate the "thermometer"-coded output of the 15 comparators into 4-bit binary. Various methods have been explored in industry and literature, including Wallace tree, Fat-tree, ROM, and MUX based designs. A MUX-based encoder design based on [1] is used for its low-power operation and high speed at the cost of high device

count, shown in Fig. 1.3.1. Additional power savings and reduction in the number of required devices is provided through the use of transmission gate-based MUXs shown in Fig. 1.3.2, which use half the number of devices as active CMOS multiplexers. Due to the load that the transmission gates put onto the comparators and to provide some delay time correction, the binary signals are sent through a network of inverters and buffers to provide MUX control logic and the eventual outputs, which are sized as shown in Fig. 1.3.3.

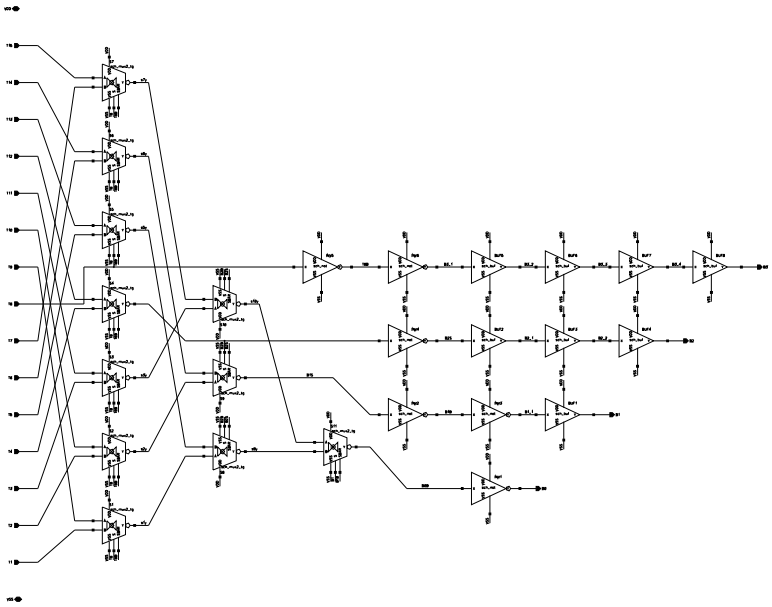

Figure 1.3.1: Schematic view of encoder design.

2 Schematic Level Simulations

Preliminary schematic level simulations have been run at typical corner of 27 °C and 2 V V_{DD}. The schematic was captured and simulated using Cādence Virtuoso.

Currently, using SPECTRE APS with ++aps and +mt=8 at conservative error preset, setting *GND*, V_{DD}, and V_{ref} nodes to their values, and setting IC=0 on appropriate internal nets, running 1 test takes 4̃:15 min at 10 clocks per code. Increasing to a more appropriate 100 clocks per code for 0.01 LSB resolution of INL and DNL increases simulation time to around 20 min. Various measures to decrease the simulation time are being investigated to capture appropriate PVT corner and monte carlo data in a reasonable time.

2.1 INL and DNL Testbench

A simple testbench schematic was set up for the flash ADC as shown in Fig. 2.1.1. The local ground for this design is decoupled from the global ground using a 0 V source, and currently a VCVS is used to increase the given reference voltage of 1 V up to 2 V for testing rail-to-rail operation. In a full system, a reference voltage at the power supply would likely need to be supplied by an LDO and possibly assisted by a charge pump. The supplied 12 MHz clock is realized by a pulse source with 5% rise and fall times, and the input triangle ramp is supplied by a piecewise-linear source. This is defined based on the clock period and is paramatrized along with the simulation time, so that the number of samples per code can be chosen.

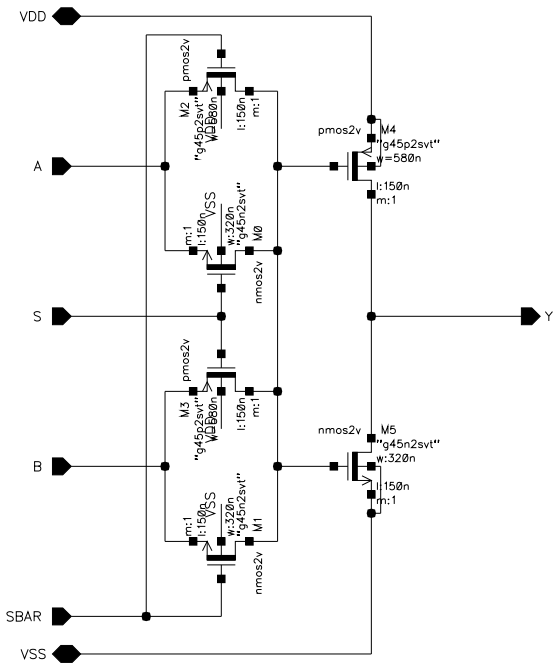

Figure 1.3.2: Schematic of transmission-gate based MUX that provides the functionality of the proposed encoder design. The outputs are inverted for logic purposes and increased drive strength.

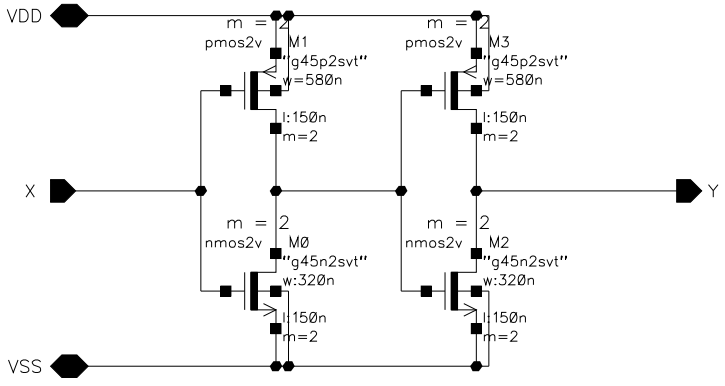

Figure 1.3.3: Schematic of buffer highlighting device sizes, which are also used in the inverter design.

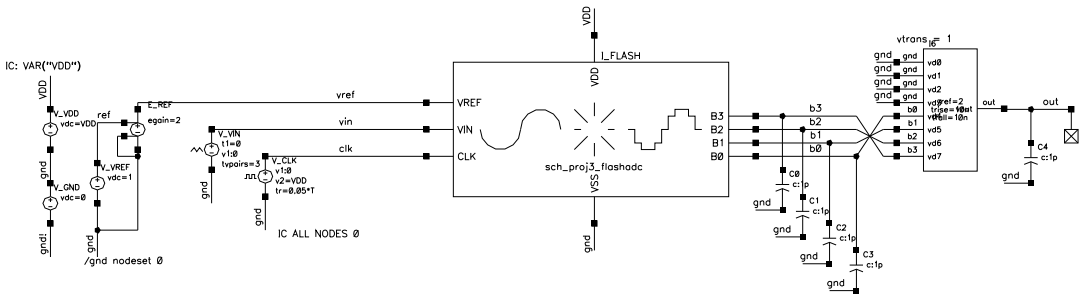

Figure 2.1.1: Testbench setup used for INL and DNL analysis.

Each output bit from the encoder drives a 1 pF load as specified, and are also sent into an ideal 8-bit DAC provided by the *ahdlLib*. This DAC is intended to translate the binary ADC output into a stepped ramp output for comparison with the ideal stepped ramp output with idealized trip voltages. Once normalized for any gain and offset error using the first and last transitions to find a $V_{LSB_{eff}}$, the difference in code widths for the output of the ADC compared to the ideal version allows for quantification of differential nonlinearity (DNL). The summation of these differences across the range provides the integral nonlinearity (INL).

The achieved results for INL and DNL at typical corner are shown in **??**. $V_{LSB_{eff}}$ was calculated to be 133 mV.

Test	Output	Spec	Weight	Pass/Fail	Min	Max	TYP
TB_FLASH	/vin						
TB_FLASH	/b0						
TB_FLASH	/b1						
TB_FLASH	/b2						
TB_FLASH	/b3						
TB_FLASH	/out						
TB_FLASH	/vref						
TB_FLASH	bin1				-2.02 mLSB	-2.02 mLSB	-2.02 mLSB
TB_FLASH	bin2				7.4 mLSB	7.4 mLSB	7.4 mLSB
TB_FLASH	bin3				7.4 mLSB	7.4 mLSB	7.4 mLSB
TB_FLASH	bin4				-20.8 mLSB	-20.8 mLSB	-20.8 mLSB
TB_FLASH	bin5				-11.4 mLSB	-11.4 mLSB	-11.4 mLSB
TB_FLASH	bin6				-2.02 mLSB	-2.02 mLSB	-2.02 mLSB
TB_FLASH	bin7				-2.02 mLSB	-2.02 mLSB	-2.02 mLSB
TB_FLASH	bin8				7.4 mLSB	7.4 mLSB	7.4 mLSB
TB_FLASH	bin9				-11.4 mLSB	-11.4 mLSB	-11.4 mLSB
TB_FLASH	bin10				-2.02 mLSB	-2.02 mLSB	-2.02 mLSB
TB_FLASH	bin11				-2.02 mLSB	-2.02 mLSB	-2.02 mLSB
TB_FLASH	bin12				7.4 mLSB	7.4 mLSB	7.4 mLSB
TB_FLASH	bin13				7.4 mLSB	7.4 mLSB	7.4 mLSB
TB_FLASH	bin14				16.8 mLSB	16.8 mLSB	16.8 mLSB
TB_FLASH	bin15				16.8 mLSB	16.8 mLSB	16.8 mLSB
TB_FLASH	DNL	< 0.5		pass	20.848 mLSB	20.848 mLSB	20.848 mLSB
TB_FLASH	INL	< 1		pass	1.2009 mLSB	1.2009 mLSB	1.2009 mLSB

Figure 2.1.2: INL and DNL results at typical.

2.2 Propagation Delay Testbench

To analyze propagation delay, the same testbench setup was used but with a modified PWL input to step nearly instantaneously right before each clock rise. This was intended to have all of the comparators slam high at once, and the last output bit to fall into place was measured for propagation delay. The results are shown in **??**

Test	Output	Spec	Weight	Pass/Fail	Min	Max	TYP
TB_PROP	/vin						
TB_PROP	/clk						
TB_PROP	/b0						
TB_PROP	/b1						
TB_PROP	/b2						
TB_PROP	/b3						
TB_PROP	/out						
TB_PROP	t1_rise				22.916 ns	22.916 ns	22.916 ns
TB_PROP	t2_rise				25.669 ns	25.669 ns	25.669 ns
TB_PROP	tp_rise	< 30n		pass	2.7531 ns	2.7531 ns	2.7531 ns

Figure 2.2.1: Propagation delay results at typical.

2.3 Results

3 Layout

Revised layout of the comparator is completed, along with layout for each of the individual blocks within each of the schematics shown above. Since redoing the comparator layout, it has been tested to run in extracted simulations at 1.1 GHz with <20 mV hysteresis.

4 Extracted Results

5 Conclusion

References

[1] J. I. Lee and J.-I. Song, “Flash adc architecture using multiplexers to reduce a preamplifier and comparator count.” IEEE, 10 2013. doi: 10.1109/TENCON.2013.6718487. ISBN 978-1-4799-2827-9. ISSN 21593442 pp. 1–4.