

EEEE 726: Project 4

8-Bit StrongARM Charge-Redistribution SAR ADC

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Abstract

This report presents an 8-bit SAR ADC design using the charge redistribution topology and a dynamic StrongArm comparator for low-power operation at a target operating frequency of 1 Msps while driving a load capacitance of 1 pF. Control signals are provided by a Verilog control block and the design is verified with AMS simulation in Cadence Virtuoso using the Cadence gpdk045_v5.0. The ADC achieves <250 mLSB DNL and <500 mLSB INL across 45 PVT corners, limited by the number of samples for histogram analysis due to simulation time which gives a precision of 250 mLSB.

1 Design

This SAR ADC is constructed to meet the requirements specified in Table 1. Since the comparator is dynamic, the reference current is not used. A typical temperature corner of 40 °C is assumed — simulations at 27 °C are not run for this design to save simulation time, since the temperature experienced within an IC would most often be warmer.

1.1 Theory of Operation

Successive Approximation Register (SAR) ADCs represent a clever iteration over topologies like the integrating and flash ADCs by adapting the binary search algorithm to strike a balance between conversion speed and power/layout efficiency, and as such have become the “workhorse” ADC for much of the data converter industry. Their topology is also ideal for pipelining, which greatly extends the

Specification	Value	Units	Comment
V_{Supply}	$2 \pm 10\%$	V	
V_{Ref}	1	V	& 2 V RTR
I_{Bias}	10	μA	Not Used
Operating Temp.	0 to 85	$^{\circ}C$	Nominal @ 40 $^{\circ}C$
Sample Rate	1	MspS	Clock: 12 MHz
N	8	bits	
C_{Load}	1	pF	Digital Outputs
DNL	± 0.5	LSB	
INL	± 1	LSB	
I_{Total}	—	A	Report
Floorplan Area	—	μm^2	Report

Table 1: Design specifications for SAR ADC.

conversion throughput of the architecture. With every clock cycle, the binary search algorithm compares a reference voltage generated by a DAC in the middle of the conversion range with the input voltage, determines if it is higher or lower than the input, and subsequently adjusts the reference to the middle of the new range where the input must be. This process is repeated until the bit depth of the ADC is exhausted. While traditionally consisting of sample and hold, comparator, SAR logic, control logic, and DAC blocks, the charge-redistribution SAR ADC subsumes the SAR logic and DAC functionality into a single capacitor array, often following some form of binary encoding based on the chosen switching procedure. Aside from decreasing the total number of circuit elements necessary to construct the ADC, relying on the principle of charge redistribution provides considerable power savings over combinational logic by relying only on switching.

For the charge-redistribution design using a single supply, during the sample phase, the top plates of the capacitors are connected to the input voltage on the V_{bus} node, accumulating a charge $Q_{total} = 2^N C \cdot V_{in}$, while the node at the negative capacitor plates and attached to the comparator's negative input V_x is connected to V_{ref} . During the hold phase, V_x disconnects from V_{ref} , the V_{bus} node is reattached to V_{ref} and the binary capacitor array and “dummy” unit capacitor top plates are switched to VSS. This essentially flips the voltage on the capacitors with respect to the charge accumulated from the input. From here, the bits are cycled by attaching the top plates of the capacitors one by one to the V_{bus} line that is attached to V_{ref} in order from MSB to LSB. Since V_x is only connected to the comparator input, the general case for the voltage at the comparator input with no offset is shown in Equation (1.1.1).

$$V_x = \frac{\alpha}{2^N} V_{ref} - V_{in} \quad , \quad \alpha = \left\lfloor 2^N \cdot \frac{V_{in}}{V_{ref}} \right\rfloor \quad (1.1.1)$$

The switching continues while recording the comparator output for each bit's value. The functionality of this system can be thought of as a closed-loop feedback system where V_x approaches V_{in} in quantized steps.

1.2 Capacitors

Since the design of this ADC requires precise control of capacitor values, mismatch must be factored into the design considerations. While one can be overly pessimistic and assume a worst-case mismatch of $+\Delta C$ on the MSB capacitor and $-\Delta C$ elsewhere, this does result in considerable overdesign and may lead to slower performance than is necessary to meet yield. Since capacitors can vary similarly to MOSFETs (dependent on the type), a simple application of Pelgrom's theorem of device sizing shows that the overall variance contribution decreases in a square root fashion as size increases. While there is no closed form solution for the full random variable analysis, a simple approximation shown in Equation (1.2.1) can be used for this design with 2^N capacitors.

$$\frac{\Delta C}{C} < \frac{1}{2} \frac{\sqrt{2^{N-1}}}{2^N - 1} \quad (1.2.1)$$

Larger capacitors also reduce the impact of any kickback noise generated by the comparator, where current couples through the parasitic capacitances at the comparator inputs and accumulates charge onto the capacitor array. Additionally, kT/C noise is minimized with larger sizing and the capacitors are made significant compared to any parasitics that may appear from layout [1, 2].

However, the capacitors cannot be made infinitely big for speed and layout area considerations. Since the switches used in an IC design have finite resistance when closed, this couples with the capacitor array to create an RC time constant for charging the array. The capacitors and MOSFET switches must be sized in conjunction to ensure that the array will be charged to well-under 1 LSB of the actual input voltage in the case of the largest expected voltage difference when the switching occurs, all before the next bit cycle. The addition of a dynamic comparator tightens this requirement, such that this charging must happen before the comparator is set to evaluate its inputs.

This design uses only the MIM capacitors provided by the Cadence gpdk045, as initial simulations using a combination of MIM and MOS capacitors yielded terrible results due to the parasitic resistance associated with the MOS caps. The clock frequency of 12 MHz due to the switching procedure adopted by the controller (12 clocks/conversion) gives freedom to use relatively large capacitors for resilience against kickback and other noise sources. The final design uses a unit capacitor of 120.9 fF, consisting of 4.5 μm by 5 μm mimcaps for additional resistance to random mismatch.

1.3 Charge Injection & Bootstrapping

In addition to the comparator kickback as a source of charge injection that can cause voltage error, the switches must also be considered for their ability to dump charge accumulated in the inverted channel back into the capacitor array. To alleviate this issue to some extent at the capacitor array, transmission gates are used as shown in Figure 1.3.1 so that both electrons and holes are injected from the NMOS and PMOS devices, respectively, and cancel each other out to some degree before accumulating in the capacitor. With relatively large capacitors used for the required operation speed, the switches are made larger at a total $W = 3.2 \mu\text{m}$ for the NMOS and $W = 7.2 \mu\text{m}$ for the PMOS devices, to make up for the lack of hole mobility. Each device has a multiplier of 10.

In the critical operations of switching to the input and reference voltages, bootstrapped switches are employed in the presented design to further reduce the injected charge and linearize the on resistance of the switch, which typically increases towards the middle of the common mode range in a traditional T-gate[3, 4]. The bootstrapped switches use a complementary design akin to a T-gate described in [5], shown in Figure 1.3.2. This design is chosen for its simplicity and the overall reduced

resistance from using complementary devices. The switching devices in the bootstrapped version are slightly smaller at $2.56\text{ }\mu\text{m}$ for NMOS and $4.64\text{ }\mu\text{m}$ for PMOS. Specific simulations to determine the switching resistance curve of these switches were not run, but their performance was amicable as initially designed. Though bootstrapped switches are not without their disadvantages [6], the addition of these in the 3 reference switching paths reduced voltage accumulation on the internal nodes of the ADC.

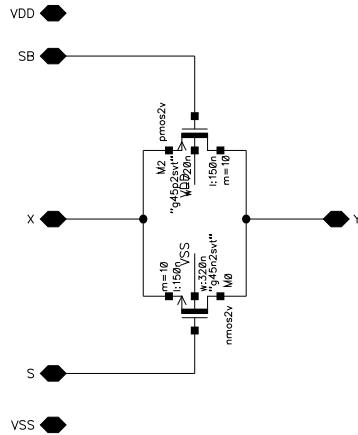


Figure 1.3.1: Transmission gate schematic, used to create normally open and normally closed switches alongside an inverter for appropriate clocking.

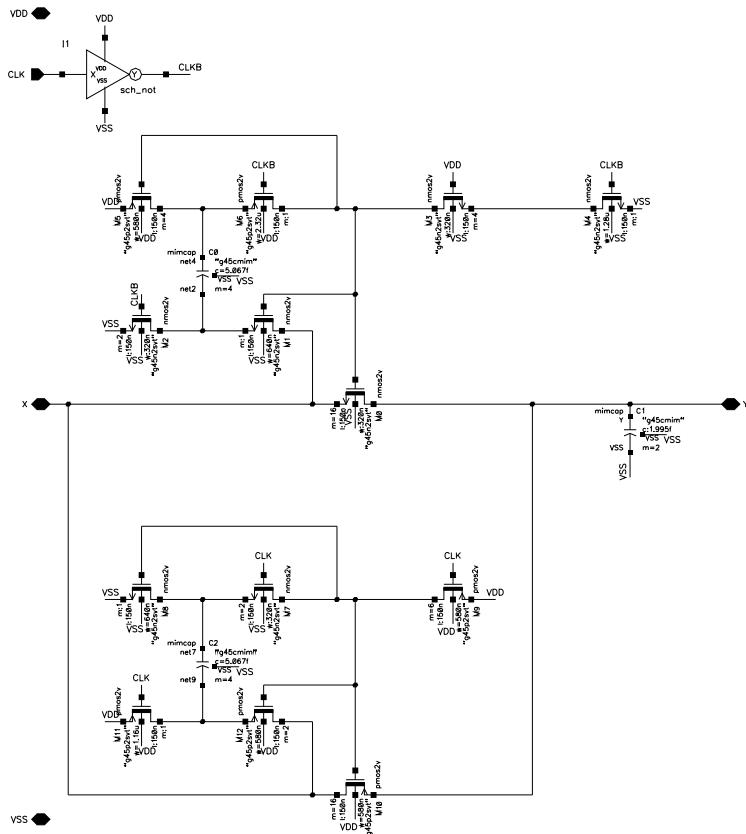


Figure 1.3.2: Bootstrapped switch schematic.

The switched capacitor schematic created for this design is done such that each unit capacitor receives its own SPDT switch for connecting to either V_{SS} or V_{bus} , to provide consistency in the RC constant across the capacitor array and provide equal drive strength to each capacitor, and for ease of layout through having unit cells for placement.

1.4 Comparator

The comparator used in this design is the same rail-to-rail StrongARM comparator used in the previous flash ADC design. The schematic has been updated for simulation purposes to change any device finger definitions to strictly multiplier values for a hopefully better approximation of its behavior across monte carlo simulation, as shown in Figure 1.4.1. Its performance as extracted from layout and simulated at 1.1 GHz is shown in Table 2 for reference.

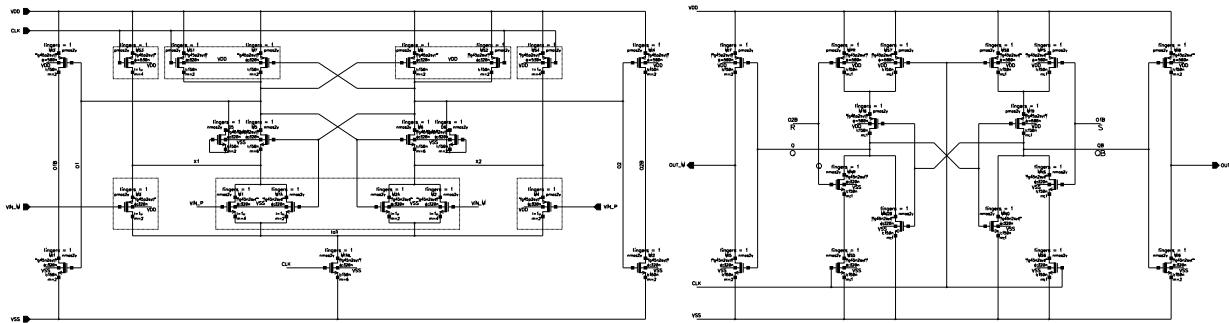


Figure 1.4.1: RTR StrongARM comparator schematic with associated SR latch output to avoid invalid outputs.

Parameter	Units	Nominal
Hysteresis	mV	14.64
Prop. Delay (1 pF)	ns	1.5778
Prop. Delay (1 fF)	ps	414.07
DC Current	nA	1.2868
W/decision	pW	1.067
Layout Area	μm^2	119.79

Table 2: Comparator performance with extracted parasitics from layout.

It is seen in the design of the flash ADC that this comparator design, while having merit for its ability to process a wide range of input signals, the extra devices on the input allow for a lot of kickback noise to be generated. The same kickback reduction scheme is employed in this design, where a transmission gate is placed after the local clock buffer to couple with the parasitic capacitance on the clock line and slow down the charging and discharging of the internal nodes V_A and V_P , which reduces the current sent back through the inputs through the relationship in Equation (1.4.1). The resistance is increased to make up for coupling with the parasitic capacitance of only one comparator by increasing the length of the devices to $1.2 \mu\text{m}$ total, as can be seen in the top right of Figure 1.5.1.

$$I_{kickback} = -\left(\frac{2}{3}WL C_{ox} + C_{GS_{tot}} \frac{dV_A(t)}{dt} - C_{GS_{tot}} \frac{dV_P(t)}{dt}\right) \quad (1.4.1)$$

Initially, no matter how small the RC time constant was made for charging the capacitor array, the

comparator would still evaluate too early and contribute to massive DNL and INL due to its synchronous nature to the switching of the capacitor circuit. Methods of delaying the clock line to the comparator were investigated to hold off its evaluation until the nodes settled, but achieving the amount of delay needed at a clock frequency of only 12 MHz proved difficult without a polyphasic clock or other methods such as a PLL. A simple, but rather brute-force, solution was to invert the clock being sent to the comparator, so that it would evaluate half a cycle later and give the capacitors more than enough time to settle. If more time were to be given to this design, it may be desirable to implement a comparator driver within the Verilog controller, with some combinational logic to generate a clock cycle only when the ADC bits are being cycled. This would both increase power savings and reduce the amount of kickback noise generated during the critical sample and hold phase.

1.5 Top-Level

The top-level design for the SAR ADC is shown in Figure 1.5.1. The switched capacitor array is in the center, with the iterated instance naming schema shown. The multiplier value of 1 is visible for each instance; a schematic using multiplier values instead of iterated instances was also created for running PVT corners, since the simulation global PVT variations would not be greatly impacted by simplifying the simulation by multiplying the currents experienced by the instance according to its multiplier. The schematic using iterated instances was run for monte carlo simulation since this would yield better and more realistic results instead of having every device within the instance have 100% correlation. The dynamic comparator is shown on the right with its “asynchrobatic drive” kickback-reduction circuitry, and the bootstrapped switches are on the left. A single bootstrapped switch instance was created for normally-open operation, and an inverter is placed before the input side reference switch to create normally-closed operation and better ensure the proper timing. The Verilog functional controller block is shown on the bottom.

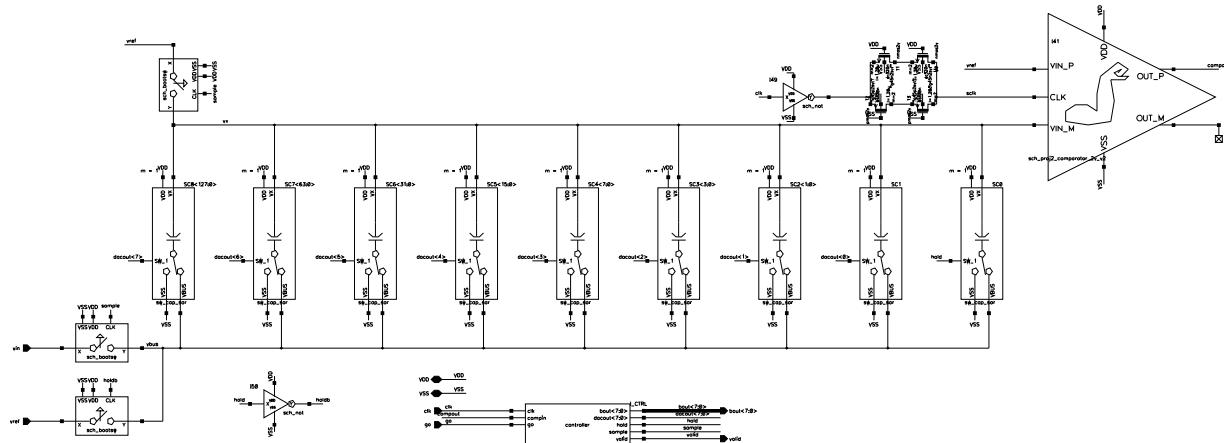


Figure 1.5.1: Top level schematic of SAR ADC. Iterated instances of switched capacitor array are shown.

2 Schematic Level Simulations

PVT corner simulations are performed using tt, ss, sf, fs, and ff process corners, VDD of 1.8, 2.0, and 2.2 V, and temperatures of 0, 40, and 85 °C. 1024 samples are chosen to give a minimum DNL and INL evaluation precision of 0.25 LSB; while this does not give an accurate quantification of the true ADC performance, it is enough resolution to qualify the performance of the ADC against spec-

ifications while maintaining reasonable simulation time with the great number of internal nodes subject to switching and charge redistribution that must be evaluated. Monte carlo analysis is performed over a finite 100 points instead of a greater number for the same time constraint with this complex design. The standard monte carlo method is used with low-discrepancy sequence sampling for improved efficiency. A “nullmfactorcorrelation=yes” netlist option is included with the hope of Spectre properly interpreting this option and setting the correlation for any devices using a multiplier to 0% instead of 100%. A brief comparison showed that this was not the case, indicating that the gpdk045_v5.0 models may not interpret this properly even though it was accepted in the netlisting logs.

The configuration management functionality provided by ADE Assembler is used during this design to perform behavioral simulations of the schematic prior to implementing instances using the gpdk045 components. Additional schematics for all components are constructed using idealized components provided by the *analogLib*, *ahdlLib*, and *basic* libraries within Cadence Virtuoso, which are included in Section A. This design methodology greatly simplifies the debugging process by allowing for single circuit elements such as non-ideal switches to be implemented and debugged with all other components functioning as expected, narrowing down the breadth of where issues may lie. Once all individual components are known to work for the design at the system level, the integration process can begin with reduced circuit debugging overhead.

2.1 Testbench

The testbench used for all simulations is shown in Figure 2.1.1. On the left, the *vdd_inherit* and *vss_inherit* instances from the *basic* library are used to ensure supply continuity between Spectre and AMS. The digital outputs are each loaded with the specified 1 pF load capacitance through an iterated capacitor, and are attached to an ideal 8-bit DAC, which regenerates an analog signal from the ADC’s output to perform histogram analysis on. A piecewise linear source is used as the input stimulus to provide a triangle wave with rise and fall times set to half the input period, for analysis of any nonlinearity introduced by comparator hysteresis or other charging effects from the rising versus falling input wave. Analysis of this design is performed with a reference voltage of 1 V even though the comparator is designed for and has been proven to handle rail-to-rail inputs, to provide a worst-case condition for any circuit element’s contribution to nonlinearity through the halved V_{LSB} at 3.922 mV resulting from the reduced reference.

Coherent sampling theory is applied to the evaluation of this ADC design due to the use of histogram functions to determine DNL and INL. The input waveform period and simulation time are parameterized based on the desired number of samples to be taken N_{samp} , the sampling period T_{samp} , and the desired number of input wave periods M which shall be odd, prime, and not a factor of N_{samp} for T_{samp} . This is accomplished using the design variables setup as shown in Table 3, which provides ease of analysis in the ADE Assembler as well. The transient analysis stop time is defined as $\text{VAR}(\text{"Nsamp"}) * \text{VAR}(\text{"Tsamp"})$. The histogram analysis is setup as shown in Figure 2.1.2.

2.2 Simulator Setup

Spectre X simulator is enabled for this design with the AX accuracy preset and AX parasitic optimization preset checked, though no extracted simulations are performed for this project. The AX preset has its own overrides for the simulation algorithm integration method and accuracy presets. MS options were originally enabled to select the controller instance as a digital block, but later disabled due to issues. The only modifications made to the simulation algorithm are enabling *pivotdc* and

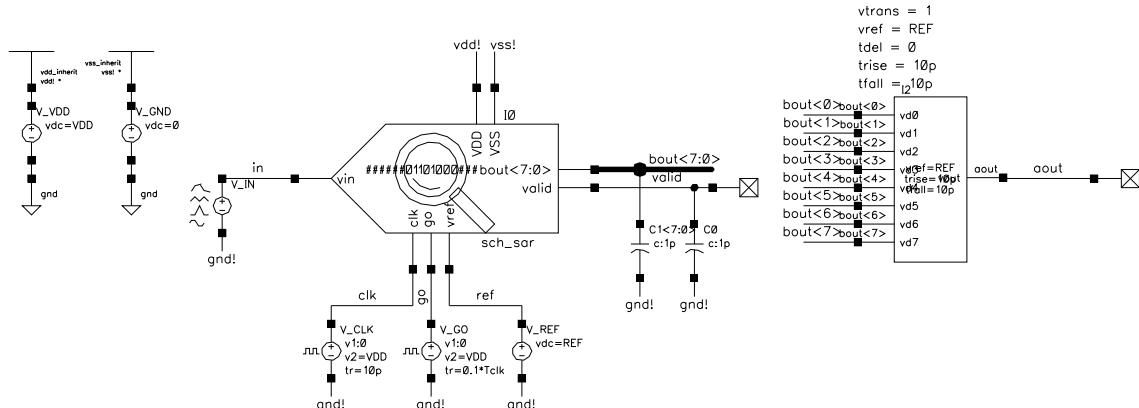


Figure 2.1.1: Testbench schematic used for all SAR simulations.

Name	Value
REF	1
VDD	2
Tclk	Tsamp/12
Tsamp	1u
fs	1/Tsamp
Nsamp	1024 (varies)
Tin	(Nsamp*Tamp)/M
M	3

Table 3: Design variables as set up within ADE test.

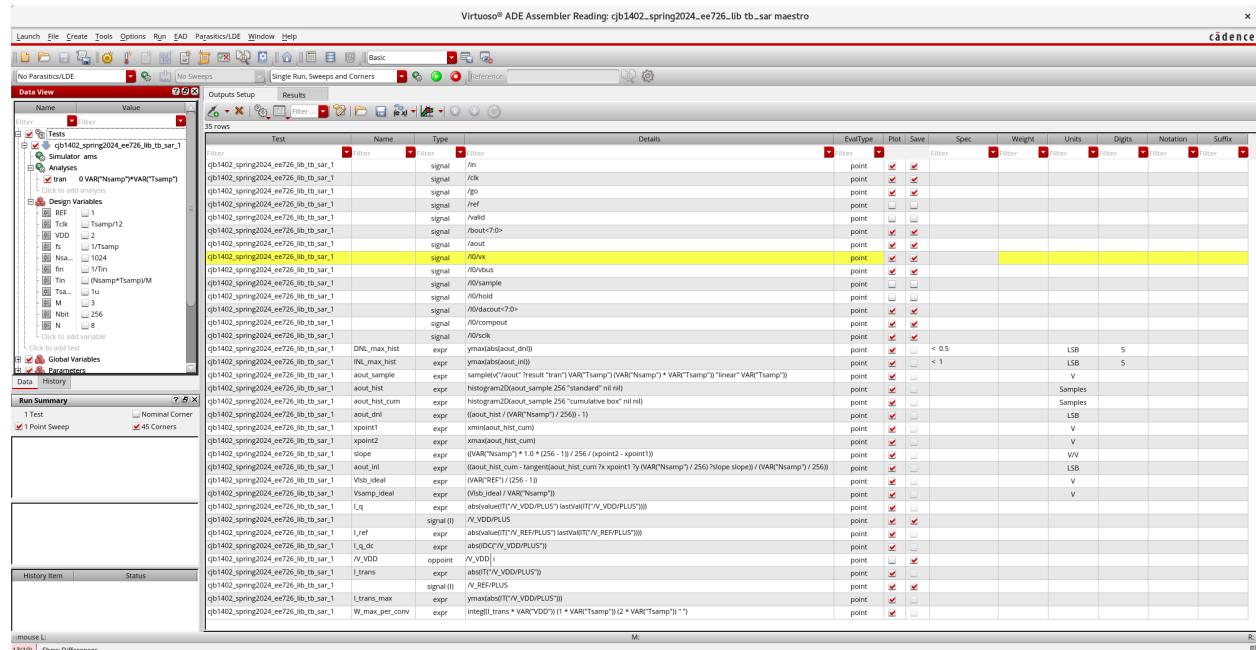


Figure 2.1.2: Histogram analysis setup.

dc_pivot_check to assist the DC solution, and enabling *rebuild_matrix* to provide more consistency from one run to another. Due to the functional Verilog controller, the AMS simulator is selected and a Connect Rule/Connect Module Based Setup is used using the built-in ConnRules_inhconn_mid ruleset.

Required simulation time is greatly extended by the fast-discharging nodes of the dynamic comparator requiring increased precision from the simulator, with 54:33 min required for each PVT corner's transient simulation to evaluate with similar results from monte carlo simulation. 2 threads are allocated by recommendation from the job log files, which enabled queuing of 24 active parallel simulation and netlisting jobs possible on the 48-core computers with negligible increase to the simulation time for each individual analysis, alleviating some of the time overhead.

2.3 Results & Discussion

This ADC design passes specification across all 45 PVT corners, with maximum DNL of 250 mLSB and INL of 500 mLSB. Many corners state an achieved DNL of 0 LSB and INL of 28.422 fLSB, which truly means <125 mLSB in both cases due to the 1024 samples used in simulation yielding 4 points per binary code. Still, the ADC performs admirably and is robust against environmental and process variation. These results are summarized in Table 4. An example waveform showing the charging behavior of the internal nodes at the typical corner is shown in Figure 2.3.1. The current measurements are taken from the V_VDD source for I_Q and $I_{tranmax}$ and the V_REF source for I_{REF} , at an arbitrary settled point during the transient simulation. These values may not represent the same as would be found via DC simulation, but represent the average performance of the ADC while it is running.

Parameter	Units	Max	Min	Mean	Median	Std Dev
DNL _{max}	mLSB	250	0	61.111	0	107.44
INL	mLSB	500	28.422×10^{-12}	77.778	28.422×10^{-12}	147.41
I_Q	nA	122.2	1.827	36.17	23.28	35.69
I_{REF}	nA	54.3	0.06146	0.01102	1.687	18.42
$I_{tranmax}$	mA	80.94	40.92	58.17	57.09	10.54
W/conversion	pW	134.4	54.19	83.57	78.94	23.94

Table 4: Flash ADC performance results across PVT corners, with a precision of 10 mLSB for DNL and INL measurements.

Monte carlo simulation proved not as successful for this design, with a 3σ yield of 41% for DNL and 89% for INL. These results are summarized in Table 5 with histograms in Figures 2.3.2 and 2.3.3. Some preliminary investigation suggests that this is contributed by comparator offset, since minimizing the variation attributed to the input devices of the comparator does improve the yield results. Additionally, the poor performance of the ADC occurs when the input is at its lowest voltages as seen in Figure 2.3.4, where offset would contribute the most severely. Since offset was not characterized over monte carlo simulations during the evaluation of the comparator, it is conceivable that this may be a contributing factor to the experienced nonlinearity. Minimizing the effects here through comparator device size increases would not be advisable due to the increased kickback and slowed operation, so a switched feedback offset compensation scheme may be advisable due to the high gain of the comparator. Closed loop stability would need to be evaluated in this case. Other options may include a fully differential input design, which can alleviate many of the effects of offset and kickback, but a different switching scheme may be necessary to prevent doubling of the switched

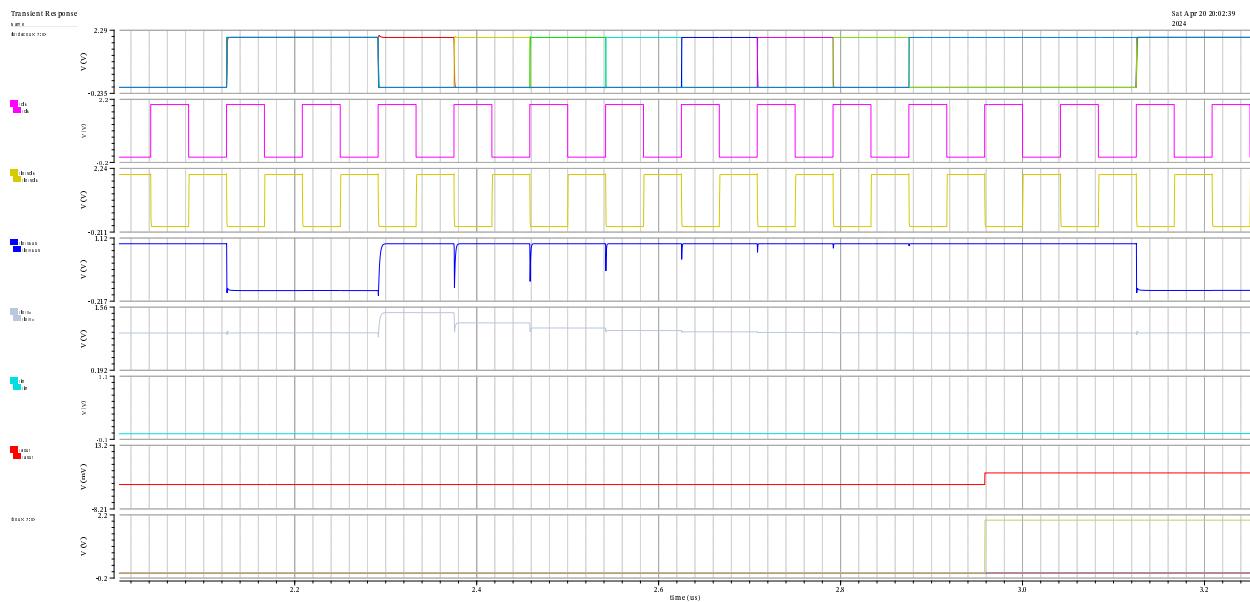


Figure 2.3.1: Waveforms of selected internal and external nodes for SAR ADC during the first valid evaluation at the typical corner.

capacitor device counts.

As previously mentioned, these results were achieved with a reference voltage of 1 V. Reviewing the statistical analysis from the monte carlo simulations, the yield may also have been improved by reducing the magnitude of the mismatch effects with respect to the overall V_{LSB} , since the median and standard deviation are relatively low compared to the mean value. Also of note, the k-sigma method for monte carlo simulation was also investigated, which uses statistical parameters to determine a pass or fail of yield spec within a confidence interval. With confidence set to 80%, it attempted to populate about 600 simulation points but a majority faced simulation errors; the ones that ran produced a slightly better yield than from the raw 100 points.

Parameter	Units	Max	Min	Mean	Std Dev
DNL	mLSB	1000	0	402.5	212.89
INL	mLSB	1000	28.422×10^{-12}	485	240.53

Table 5: Results from 100 points of monte carlo mismatch simulation, with a precision of 250 mLSB.

3 Layout Floorplan

Full layout of the ADC design is not required for this project, but a preliminary floorplan using the device instances in Layout GXL is created and shown in Figure 3.0.1. The switched capacitor instances are common-centroided outwards from the center, with the comparator and bootstrapped switches placed near the center. The full layout size is $226.57 \mu\text{m}$ wide by $190.96 \mu\text{m}$ tall, for a total layout area of $43.265 \mu\text{m}^2$. The unit switched-cap layout is shown in and the bootstrapped switch layout is shown in Figures 3.0.2 and 3.0.3.

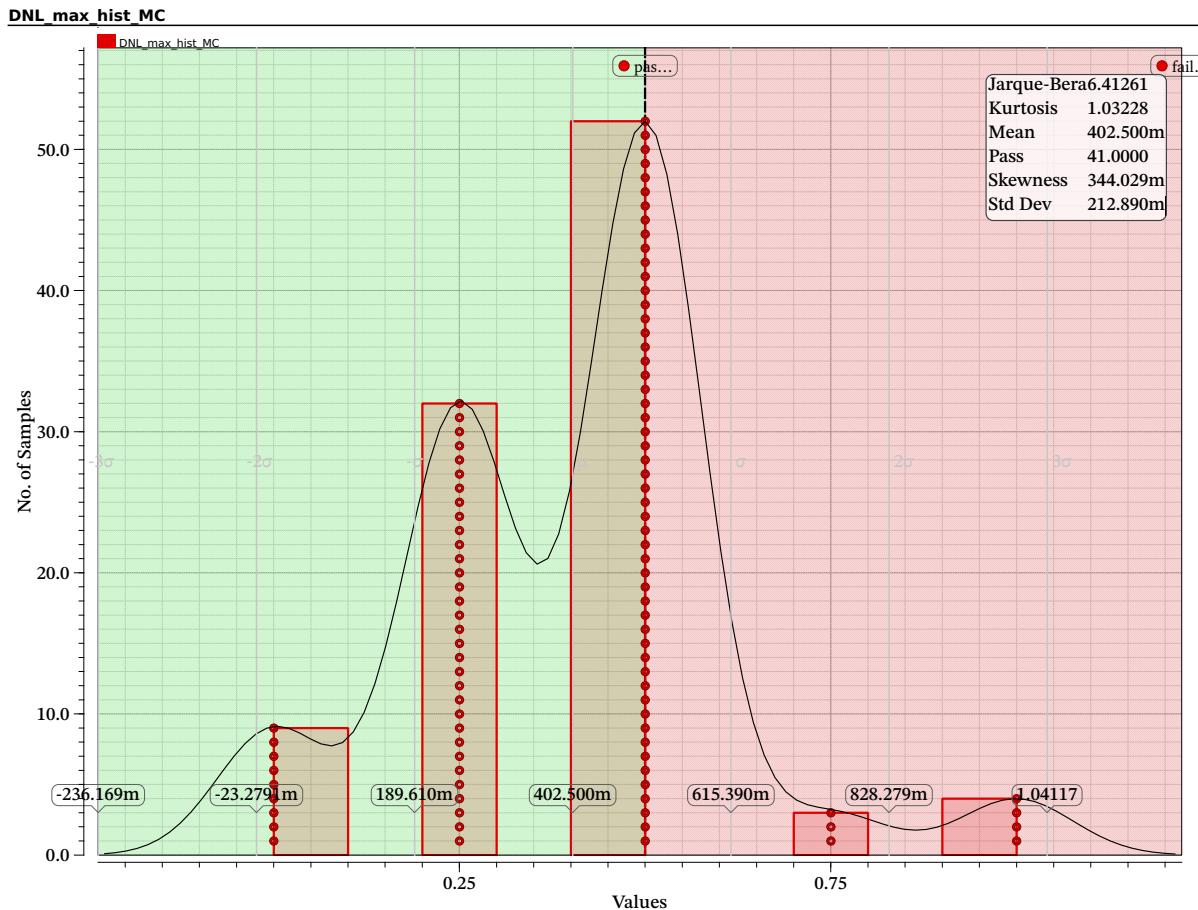
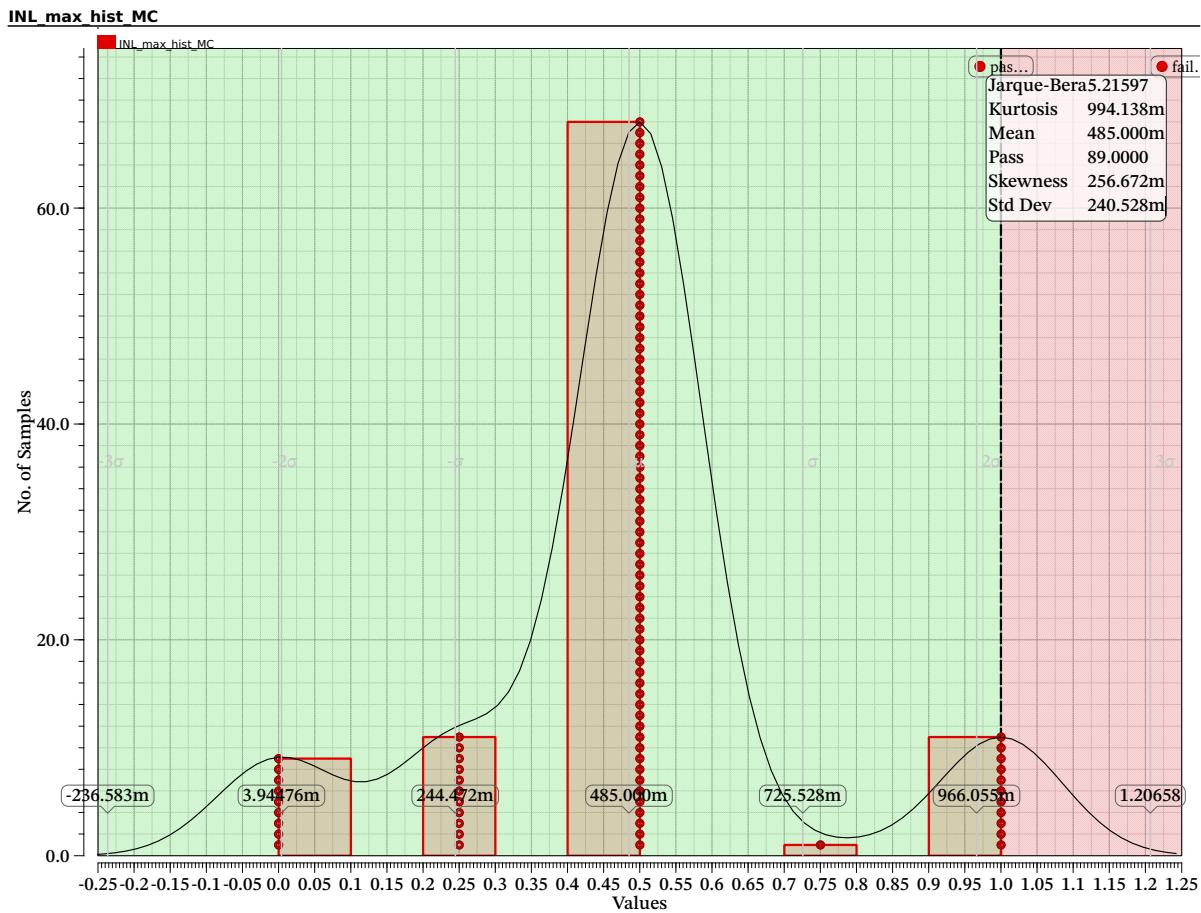
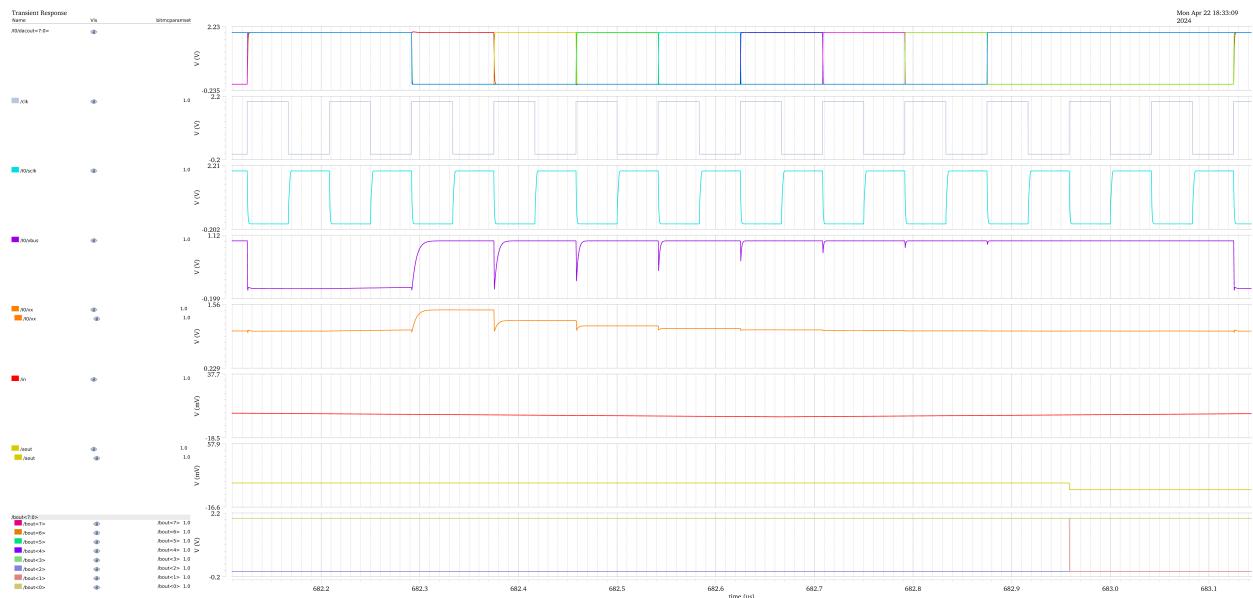


Figure 2.3.2: DNL monte carlo histogram.

**Figure 2.3.3:** INL monte carlo histogram.**Figure 2.3.4:** Example of improper evaluation when input is at its lowest during monte carlo simulation.

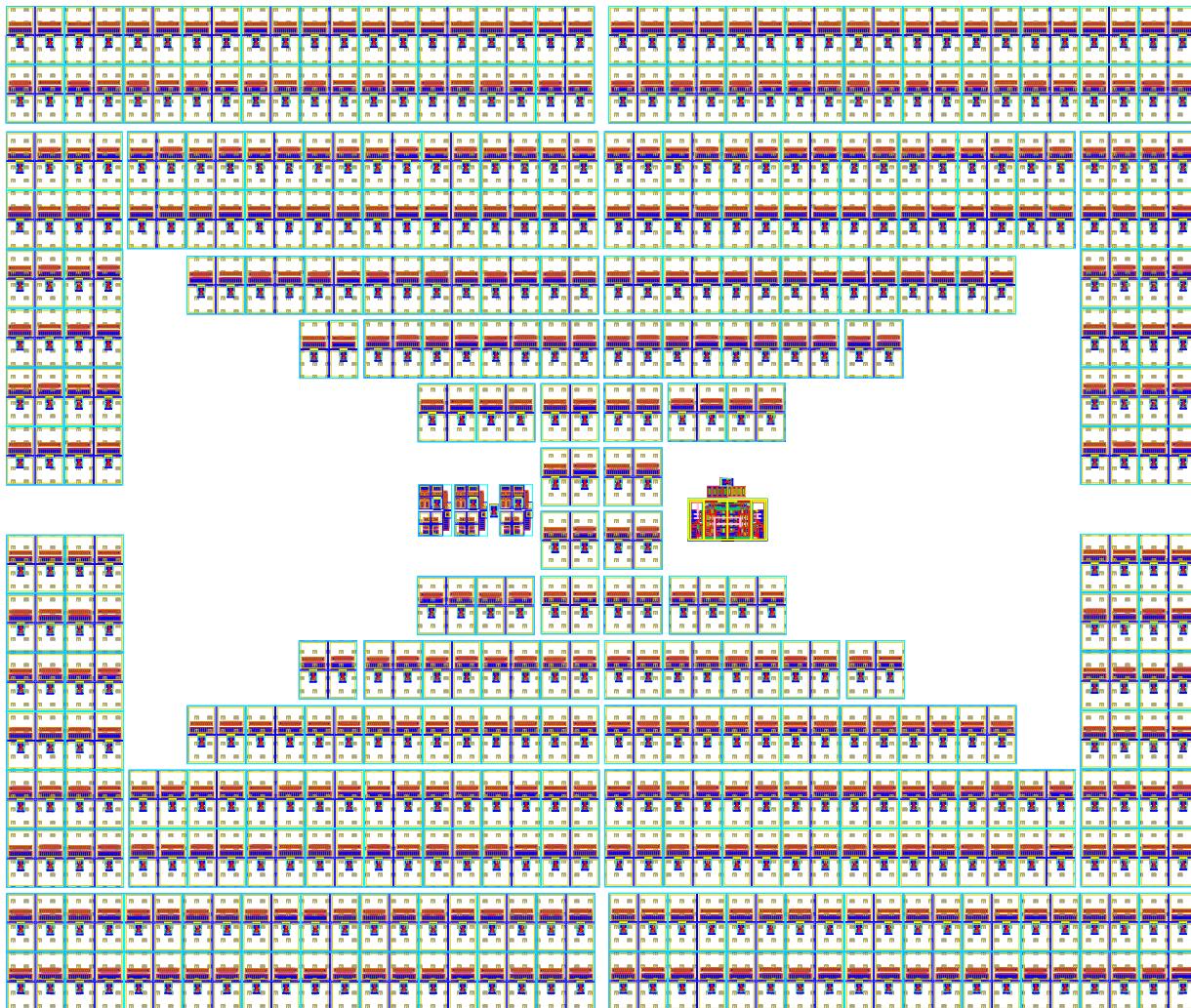


Figure 3.0.1: Full SAR layout floorplan.

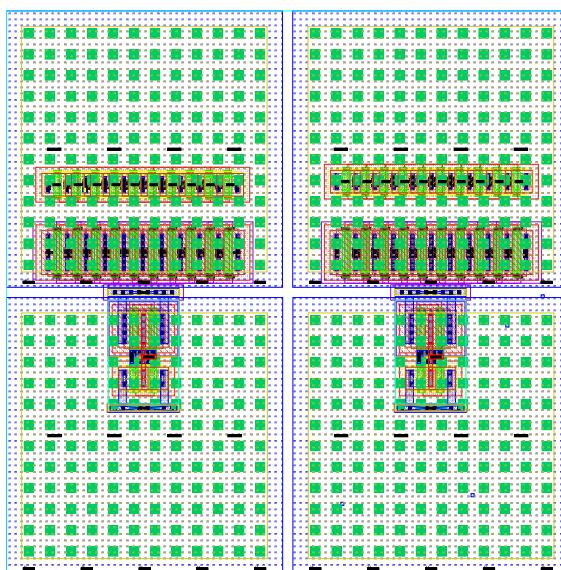


Figure 3.0.2: Unit switched capacitor layout floorplan, with switches on the top and inverters on the bottom.

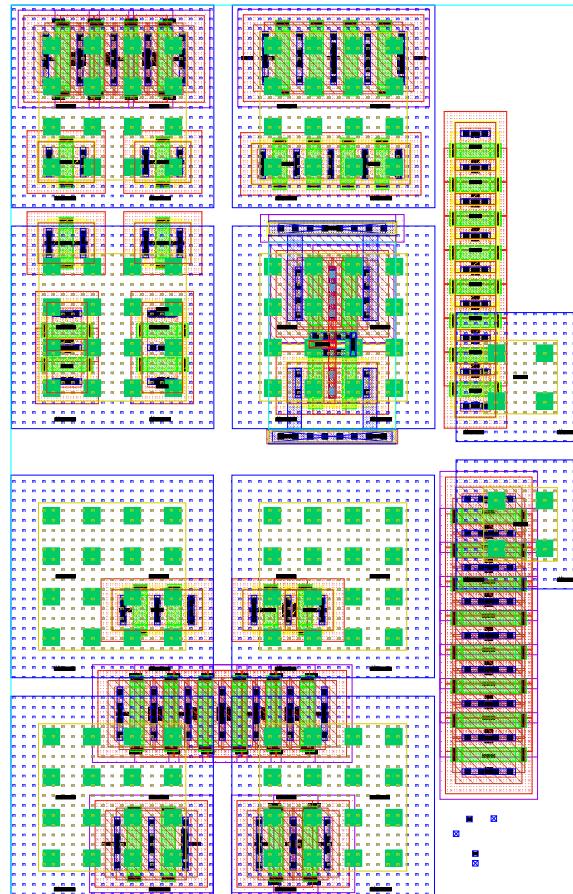


Figure 3.0.3: Bootstrapped switch layout floorplan. Switching devices are on the right underneath a small load capacitor for charge injection reduction.

4 Conclusion

This charge-redistribution based SAR ADC succeeds at meeting the design specifications across corners, and there is a clear path for increasing the 3σ yield in monte carlo simulations, as the results achieved are workable but not ideal for fabrication as-is. The inclusion of this specific dynamic comparator design lends additional functionality, adaptability, and power savings through little DC current draw to this ADC design, while needing special consideration to not negatively impact the internal charge redistribution among the capacitors. An improved driving system has the potential for further improve the resolution of the ADC and allow for the reduction of necessary capacitor size.

References

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A Ideal Schematics

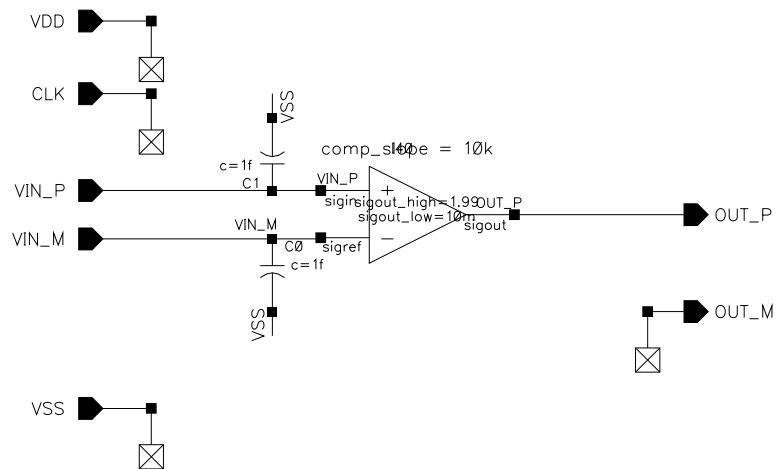


Figure A.0.1: Behavioral comparator schematic.

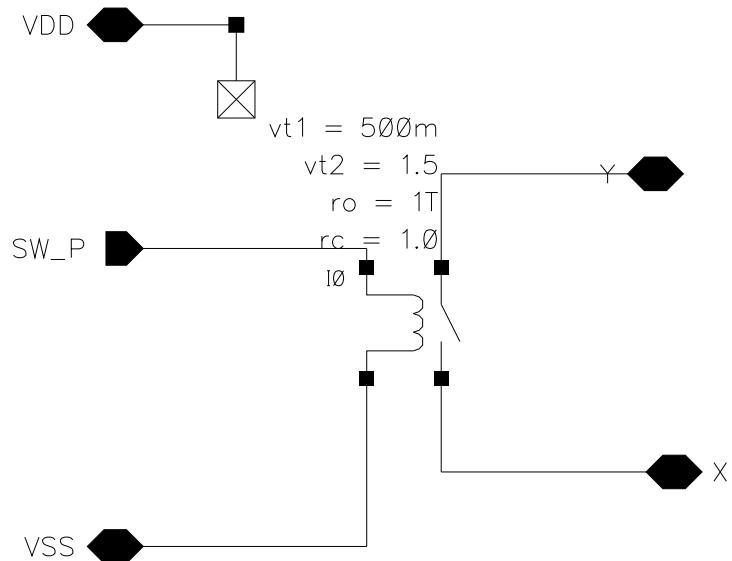


Figure A.0.2: Behavioral normally-open switch schematic.

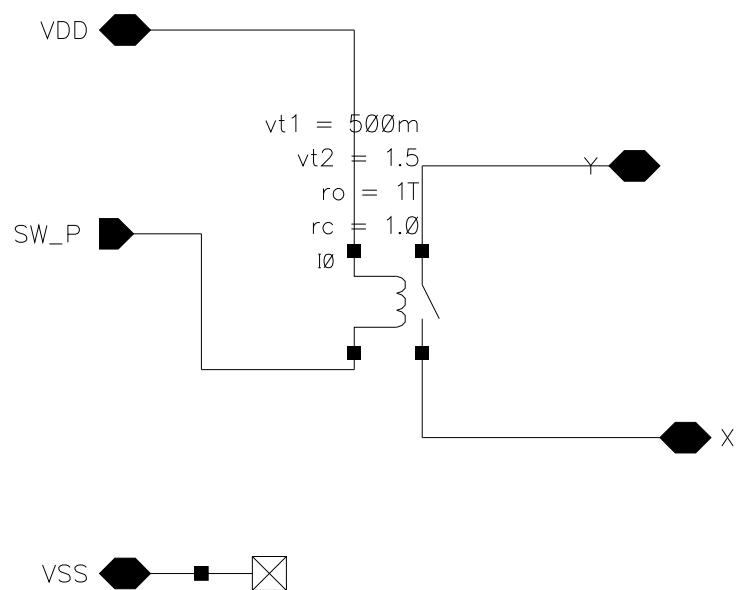


Figure A.0.3: Behavioral normally-closed switch schematic.