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Department of Electrical and Microelectronic Engineering

# EEEE 726: Project 5
# 3.3 V Bandgap-Regulated Charge Pump Power Supply for Portable Applications

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## Abstract

This report presents the design of a regulated charge pump for battery powered portable applications using 3.3 V digital logic, typically supplied by 2 series alkaline batteries yielding a little over 3 V when fully charged. The regulation of the charge pump is designed to keep the output voltage within 10 % as the battery discharges down toward 2 V. While this exercise is more of a thought experiment like the PN junction [1], it worked on the first simulation using Cadence gpdk045_v5.0 components and ideal current sources, without verifying the circuit behaviorally and despite performing limited "napkin math" for device sizing. Swapping out the ideal sources for all wide-swing regulated cascodes shows little impact on the circuit performance. Analysis performed over a range of load resistances displays the ability to drive 48.38 mA into a 61.58 Ω load at 9.65 % voltage dropout when fully charged.

## 1 Design

Charge pumps are often found in IC designs requiring a boost in voltage for additional supply, reference, or other uses. While a bandgap reference may be used on-chip to provide a very stable reference for the charge pump to subsequently boost, the output of the charge pump must be regulated in some way to smooth out the noisy charge pump output and give it added driving capability. The additional regulation circuitry can be substantial in layout area, but a topology proposed by Robert Gregoire [2, 3] for AMI Semiconductor in Bozeman, MT attempts to fold the regulation circuit within the charge pump architecture for compactness. This design adopts a single frequency switching scheme for its well-defined frequency spectrum of noise injection into the output, which can be

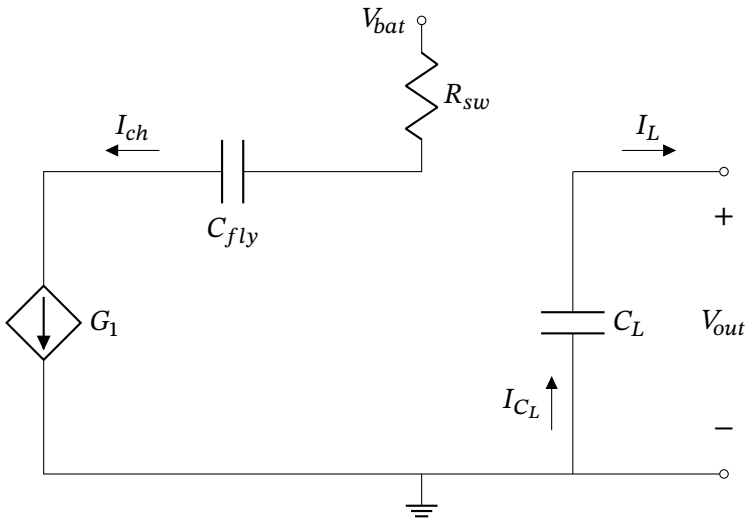


**Figure 1:** Simplified schematic of charge pump during charge phase.

easily filtered out. Additional device savings is provided by using a modified switched-capacitor bandgap reference, so that the typical $N$ additional BJTs are replaced with a scaled current source and a few switches.

## 1.1 Theory of Operation

During charging ($\Phi_1$), shown in Figure 1, the flyback capacitor $C_{fly}$ is charged by switching it into parallel with the supply and regulating the current via an OTA. The amount of charge placed onto $C_{fly}$ is regulated through the OTA by comparing the output to a reference voltage. When the output dips, additional current is supplied to provide the necessary charge under the same time constraints. During this phase, the filter capacitor $C_L$ discharges to provide the necessary current to the load. During $\Phi_2$, shown in Figure 2, $C_{fly}$ is discharged to supply the load and resupply the filter cap with the necessary charge. In both phases, the charging behavior is limited by the RC constant formed by the switches needed to redirect the current paths, so keeping the on resistance to a minimum is paramount.

In Figure 1, $I_{ch}$ is provided by $G_1$, which is defined as $\mathrm{G_M}(V_{ref} - V_{out})$. The exact value of $\mathrm{G_M}$ is difficult to find due to the dynamics of the switching operation, but it is roughly on the order of:

$$\mathrm{G_M} \sim \frac{C_3}{C_1 + C_2 + C_3 + C_{par_{OTA}}} \cdot \frac{g_{m_{OTA}}/C_4}{\left(\left(\frac{W}{L}\right)_2 + \left(\frac{W}{L}\right)_1\right) \cdot F_{osc}} \tag{1}$$

Through this, the load regulation capability can be found along with the output resistance, $R_{out} = {}^{\Delta V_{out}}/_{\Delta I_L} = {}^{2}/_{\mathrm{G_M}}$. When current is drawn beyond the regulation capability, the output voltage is determined by the maximum amount of charge $Q$ that can be transferred to $C_{fly}$ within the given timeframe:

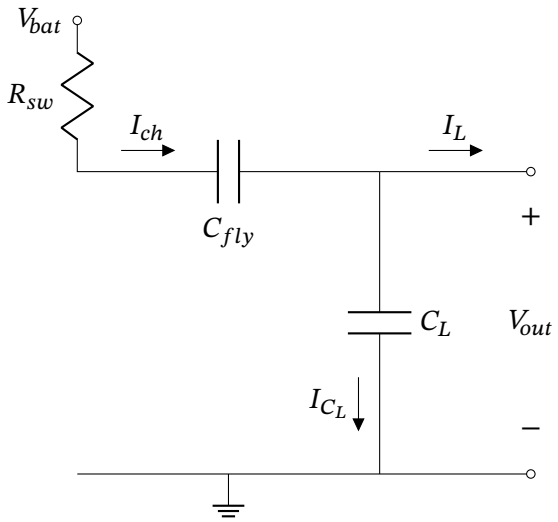


**Figure 2:** Simplified schematic of charge pump during discharge phase.

$$\begin{cases} \Delta Q = C_{fly} \cdot (V_2 - V_1) = {}^{I_L}/_{F_{osc}} \quad , & (2) \\ V_1 \triangleq V_2 + (V_{out} - V_{bat} - V_2) \cdot (1 - e^{-\beta}) & (3) \\ V_2 \triangleq V_1 + (V_{bat} - V_1) \cdot (1 - e^{-\beta}) & (4) \\ \beta \triangleq {}^{1}/_{(2 \cdot F_{osc} \cdot R_{sw} \cdot C_{fly})} & (5) \end{cases}$$

Combining these yields:

$$V_{out} = 2V_{bat} - \frac{I_L}{F_{osc} \cdot C_{fly}} \frac{(1 + e^{-\beta})}{(1 - e^{-\beta})} \tag{6}$$

and

$$I_{L_{max}} = (2V_{bat} - V_{ref}) \cdot \frac{(1 + e^{-\beta})}{(1 - e^{-\beta})} \cdot C_{fly} \tag{7}$$

In the case that $R_{sw} \ll {}^{1}/_{(2 \cdot F_{osc} \cdot C_{fly})}$, $I_{L_{max}}$ reduces to:

$$I_{L_{max}} = (2 \cdot V_{bat} - V_{ref}) \cdot F_{osc} \cdot C_{fly} \tag{8}$$

As $R_{sw}$ increases to be $\gg {}^{1}/_{(2 \cdot F_{osc} \cdot C_{fly})}$, it becomes the limiting factor of output current:

$$I_{L_{max}} = {}^{(2 \cdot V_{bat} - V_{ref})}/_{(4 \cdot R_{sw})} \tag{9}$$

The stability of the system can be assessed using discrete-time analysis in the Z domain. More detail is shown in [3], but in general for a 50 % duty cycle, the system is stable if:

$$\frac{G_M/(2 \cdot F_{osc})}{C_{fly} + C_L} < 2 \tag{10}$$

This limits the achievable load regulation as:

$$R_{out} > 1/(2 \cdot F_{osc} \cdot (C_{fly} + C_L)) \tag{11}$$

### 1.2 Switched Capacitor Reference

A traditional bandgap reference circuit leverages a combination of currents through PN junctions formed by diode connected BJTs operating at different current densities, more closely mimicking an ideal diode. This generates a PTAT current relationship to perform a first-order correction for the CTAT $V_{BE}$ relationship. To eliminate bipolar mismatch and inherently cancel offset at the OTA inputs so that a simpler amplifier can be used, the present design uses a switched topology to bias a single PN junction at two different current densities. Switching this output to charge capacitors yields the following reference voltage:

$$V_{ref} = \frac{C_2}{C_3} \cdot \left( V_{BE} + \frac{C_1}{C_2} \cdot U_T \cdot \ln N \right) \tag{12}$$

where $U_T = k_B T/q$ and $N$ is the ratio of the two currents switched across the PN junction. To achieve effective compensation of the temperature coefficient, $C_1/C_2 \sim 10$. Other ratios may be selected due to an application requiring a temperature coefficient, possibly to cancel another temperature coefficient of what the circuit is driving.

### 1.3 OTA

A simple output-impedance boosted common source OTA, shown in Figure 3. is used in this application for its simplicity. A low offset amplifier is not necessary due to the switched input. The 60 µA bias current is also supplied by a wide-swing regulated cascode as described in [4]; the diode-connected NMOS devices simply serve as resistors to reduce the bias current through the regulating stages, since this is not needed to be high. Originally, the design for a wide swing regulated cascode with increased $g_m$ for better error amplification proposed in [5] was explored, but this design would not work no matter what. This is likely down to the device size limits imposed on the gpdk045_v5.0, which unfortunately limits device lengths to 10 µm. The current bias for the OTA is sufficient to drive the current switch transistor during the charging phase, and since it would ideally be bootstrapped to the output voltage, this could cause some additional current draw from the regulator due to the inefficiency of the charge pump.

### 1.4 Non-Overlapping Clock

Since the charge pump circuit relies on keeping the accumulation of charge on the capacitor places as efficient as possible, a non-overlapping generator circuit is used to split a single clock into the two necessary phases and their non-overlapping complements, shown in Figure 4. The clock used in this design has a 30 % duty cycle to provide some additional efficiency by mostly keeping $C_{fly}$ in the discharging state. The clock generator uses the a standard configuration with large inverter drivers within the loop to reduce the chance of overlap.

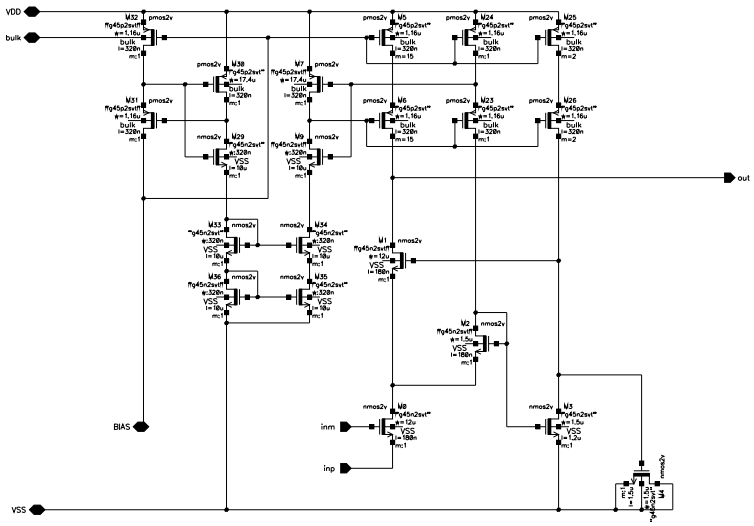


**Figure 3:** OTA with wide-swing bias for the charge pump regulator.

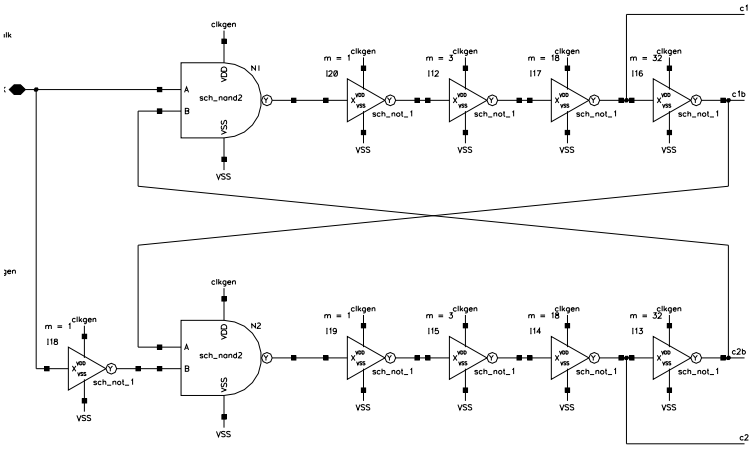


**Figure 4:** Non-overlapping clock generator, with multipliers to provide appropriate drive strength for the gigantic switches.

## 1.5 Comparator for Bulk Bias

Finally, the author has constructed a continuous-time comparator as shown in Figure 5. This is used to observe the input and output voltages, and ensure that the PMOS devices of the charge pump and their gate drivers are biased to the highest level to prevent latchup when the input voltage drops and the regulator takes over to keep the output voltage up. The output of the comparator controls t-gates, which appropriately select the bulk bias voltage. To additionally prevent the large devices from being blown up during a shorting event that the comparator does not have time to respond to, resistors are included before the bulk ties. The comparator startup signal is provided by a NOR gate to ensure it is not powered down before $V_{out}$ discharges below $V_{bat}$.

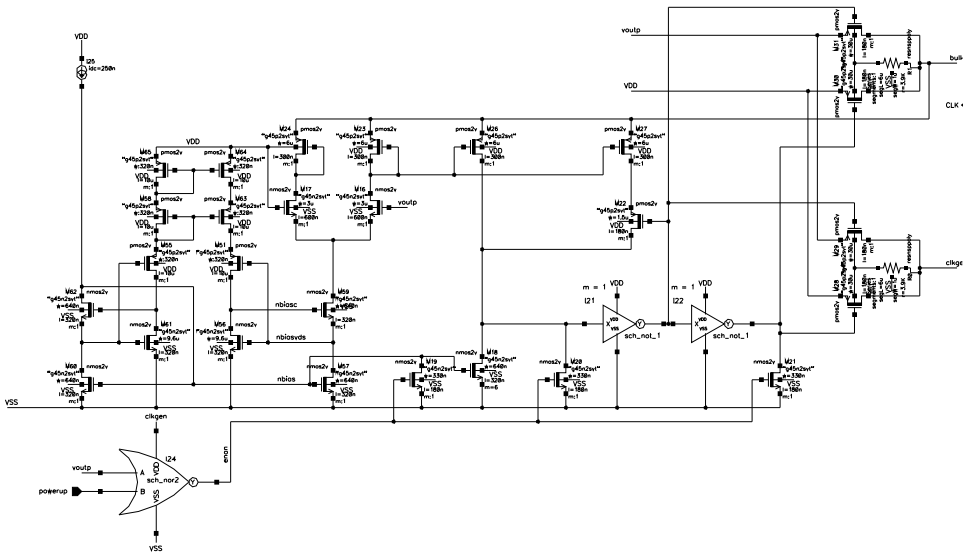


**Figure 5:** Continuous time comparator for selecting the best PMOS bulk bias voltage.

## 2 Top-Level Design

The schematic-level design for this circuit is accomplished with a generously termed "flattened-hierarchy" design shown in Figure 6, which involves dumping everything into a single schematic file. While in no way ideal from an organizational standpoint, this circuit is quite complex and this makes it somewhat easier to navigate all of the connections. The full design is realized using the same normally-open switches from the previous SAR ADC design, with no modification to the t-gate sizes shown in Figure 6. A single 250 nA reference current is supplied to the current mirror of the comparator, which uses the same mirroring structure as the OTA. This is also mirrored to PMOS devices while being stepped up to 1 µA across the BJT during $\Phi_1$, 11 µA for $\Phi_2$, and 10 µA for the charge pump gate drivers. The resistors provided for bulk current limiting are visible on the right side of Figure 6.

### 2.1 Device Sizing

Equation (12) is used as a starting point to calculate for a 3.3 V nominal output voltage. The ratio of $C_1$ to $C_2$ is selected to be 8:1 to target reasonable temperature coefficient correction while enabling 2D common-centroid layout for these important devices. Substitution reveals a subsequent $C_2/C_3$ ratio of about 2.8, so 28 unit capacitors are chosen for $C_3$. The unit MIM capacitors for this design are set to 4 µm by 4 µm, giving a total capacitance of 20.28 fF for quick charging. Using Equation (1) and setting an arbitrary $F_{osc}$ of 100 MHz, the size of $C_4$ can be estimated. Assuming that $C_{par_{OTA}} \sim C_2$, the first term of Equation (1) can reduce in terms of $C_3$ to $1/51.4$. Using $W/L$ ratios of $480/0.18$ and assuming $G_M \geq 16.5$ is needed for 10 % regulation, it is found through relating $g_m$ of the OTA to $C_4$ that $C_4$ does not need to be large, so 4 times the unit capacitance is selected to start with. The device sizes within the charge pump and comparator are scaled from [3] down to a minimum length of 180 nm for integer matching.

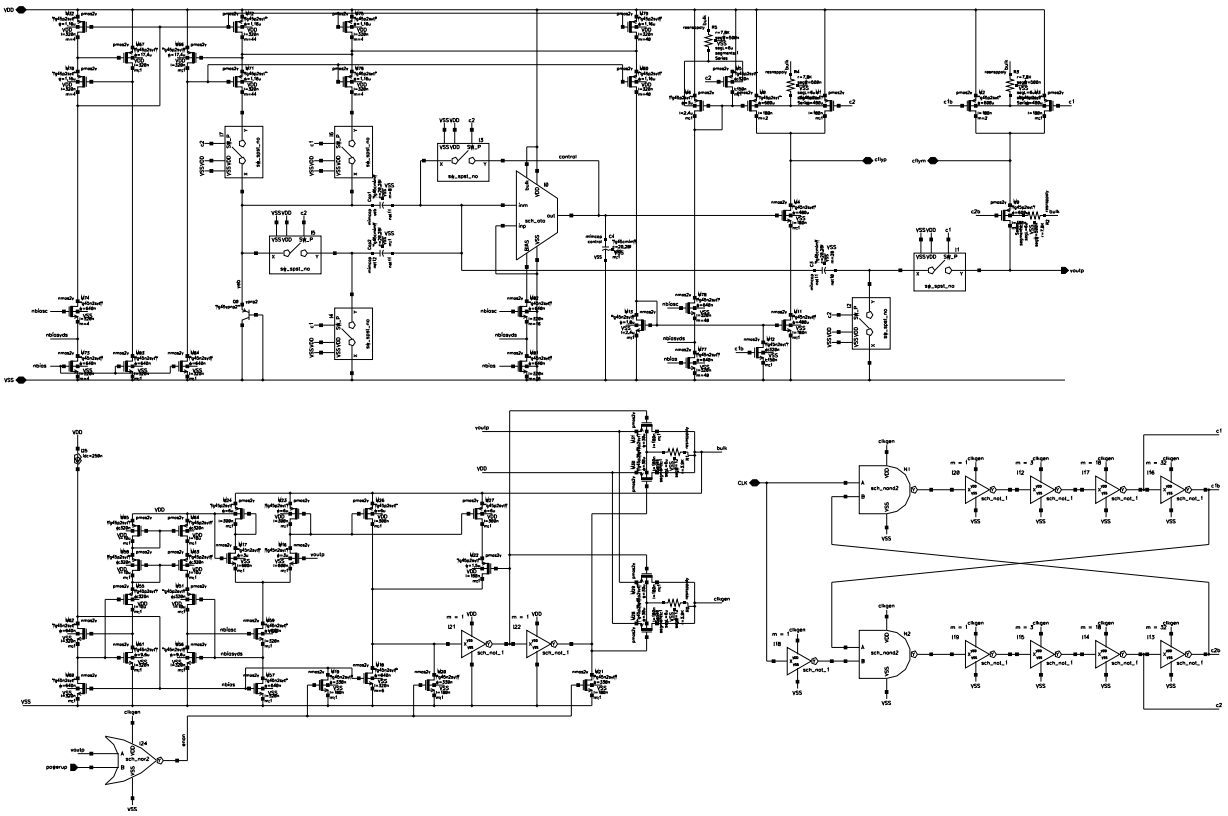

**Figure 6:** Full regulated charge pump schematic, with accoutrements

# 3 Schematic Level Simulations

This circuit was evaluated at a 40 ° C nominal corner for schematic simulations. Spectre X simulator is enabled for this design with the AX accuracy preset. The only modifications made to the simulation algorithm are enabling *pivotdc* and *dc_pivot_check* to assist the DC solution, and enabling *rebuild_matrix* to provide more consistency from one run to another. No initial conditions are set on any of the nodes, leaving this to be found by the DC analysis. Transient simulations are performed over a period of `1000*VAR("Tclk")` while the input is ramped down in voltage to simulate battery discharge while the device is being used. Concrete performance analysis of load and line regulation is somewhat difficult with the parameterized simulation used, so analysis of performance is mostly performed through graphical means.

## 3.1 Testbench

The testbench constructed for the circuit is quite basic, needing only a clock source set up as a pulse with 0.01 % rise and fall times, an enable signal provided by a DC source unless startup behavior is being evaluated, and input power as shown in Figure 8. A 1 Ω resistor is in series with the ideal voltage source to simulate the typical source impedance of an alkaline battery. The flyback and load filter capacitors are provided by off-chip 100 nF and 1 µF devices, respectively.

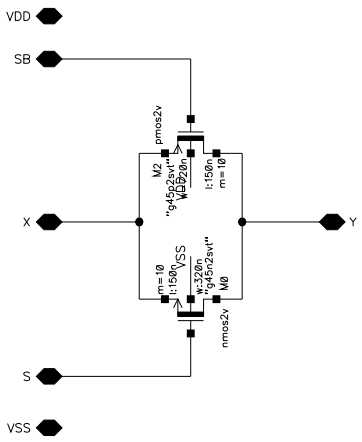


**Figure 7:** Transmission gate sizes used for switching in the regulator.

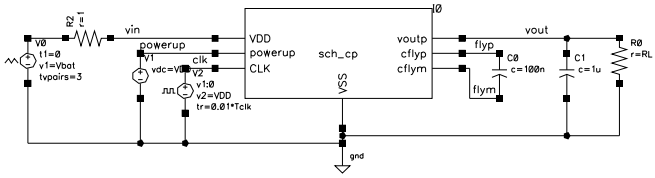


**Figure 8:** Testbench setup for dropout regulation.

## 3.2 Results & Discussion

Upon the first simulation with ideal current sources, the regulator did appear to perform the regulating, as shown in Figure 9. As the battery voltage begins to decline, the charge pump does its best to keep the voltage on the output side up close to 3.3 V, until it begins to be loaded down as well. The markers indicate the location of a 10 % drop in output voltage. This simulation was performed with only 100 clock cycles, so the load capacitor does not have time to display it full discharge, but this was great encouragement that the design does work. Figure 9 also shows no kickback onto the input voltage, since this was done before the 1 Ω load was added.

Subsequently, the ideal sources were substituted out for their wide-swing cascoded counterparts. At DC, this configuration performs admirably and ensures very minimal $V_{DS}$ mismatch in the mirroring devices, so there is minimal change in the bias points for the circuit. Transient simulations also show much the same story, with little to no difference observed in the current/voltage characteristics at the output. From here, 60 simulations are run with 20 different load resistance values from 10 Ω to 10 kΩ at 0, 40, and 85 ° C, as shown in Figure 10. Figure 11 shows the input and output current plots.

Overall, performance is better than expected, achieving 10 % dropout at quiescent when driving 48.38 mA into a 61.58 Ω load. This is most likely down to some overly cautious estimations made when eyeballing device sizes for the target spec. The output resistance is estimated to be around 10 Ω from the plot at which the quiescent output voltage is cut in half. Stability in the frequency domain is ensured with the low output resistance by the high switching frequency and maintaining relatively large capacitors, through the relationship in Equation (10).Temperature stability of the circuit is shown to be extremely good, with 0.0112 % variation from 0 to 85 ° C when driving ∼329 µA into 10 kΩ, up to 11.65 % variation when driving ∼177.3 mA into 10 Ω. Since the circuit is

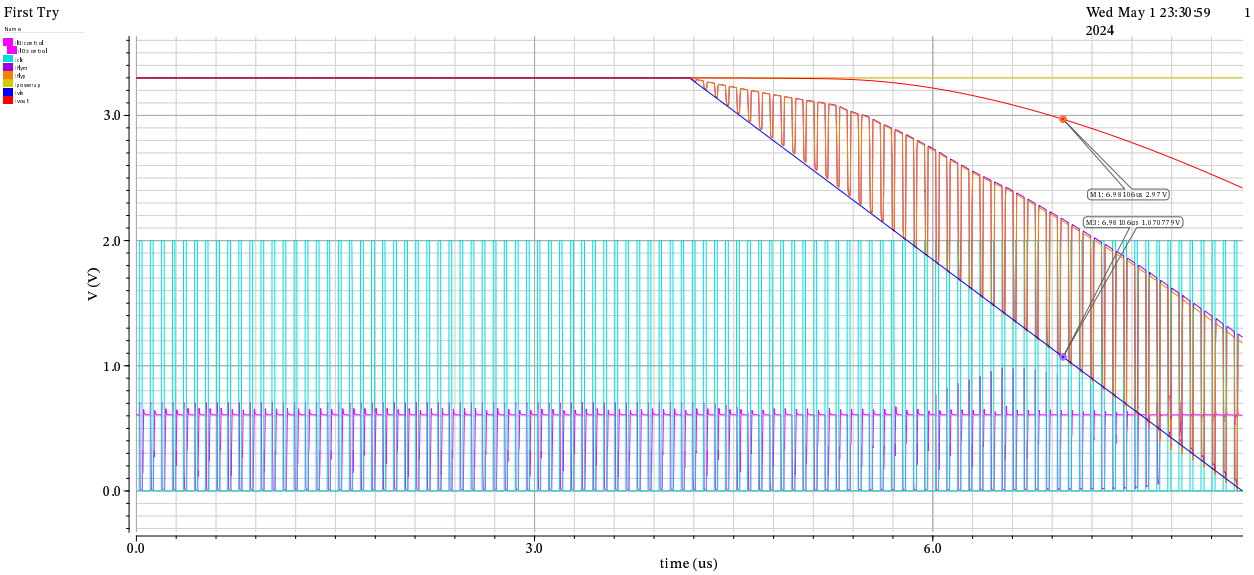


**Figure 9:** It works (ideally).

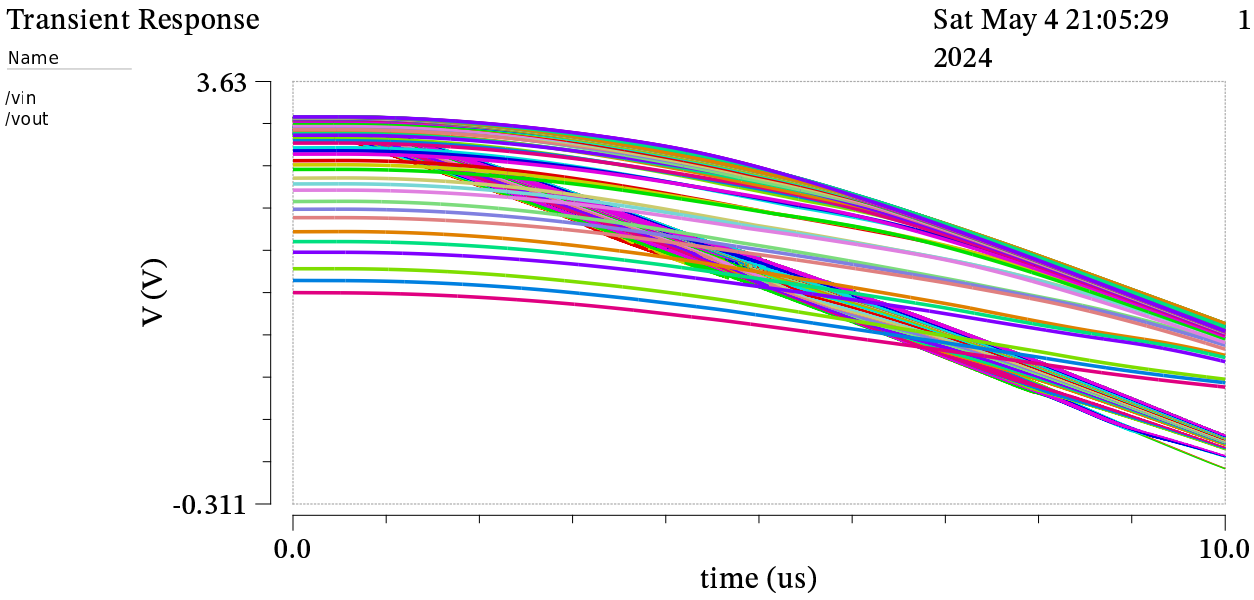


**Figure 10:** Input and output voltage plots for different load resistances.

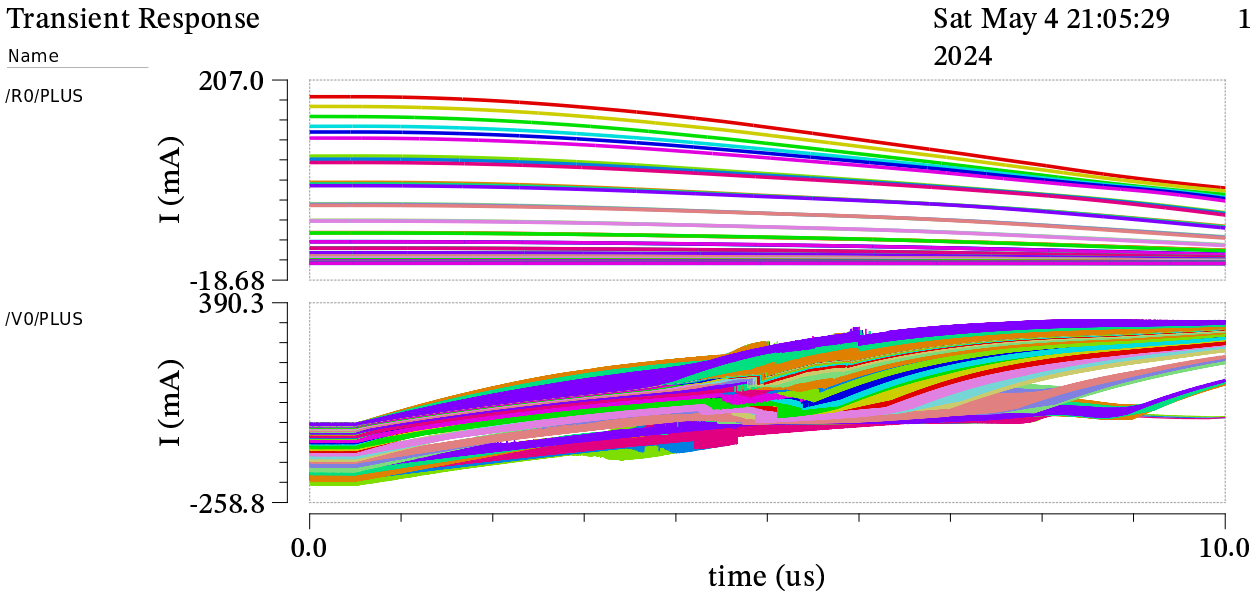


**Figure 11:** Input and output current plots for different load resistances.

not designed to operate at this point, the experienced current stability when operating below 50 mA appears quite sufficient.

Power efficiency calculations proved impossible to get an answer that makes sense from the Cadence calculator, but by observing the plots, about a 2x draw can be seen on the output side as compared to the power supply, which tracks for the behavior of the regulated charge pump. The switching behavior of the bulk bias can also be seen as the input drops below where the output lies, which increases the current draw since the clock power supply is then switched to the more inefficient output side.

While not shown due to data loss associated from what is presumed to be RIT ITS "technicians" spilling their coffee into the Cadence server for at least the fourth time this year, or perhaps the computer case overflowing with dust from being improperly cared for, the startup behavior of the circuit was analyzed at the nominal corner. The behavior of the cirucit is as expected; once power is supplied and the startup line pulled high, the filter capacitor on the output begins to charge and takes an appropriate amount of time to reach the full 3.3 V. Reaching full output takes a little bit longer due to the switching behavior, but no unexpected effects are observed.

## 4 Layout Floorplan

To see potential effects of the $3 \times 1.2$ mm transistors on layout area of the circuit, the devices were generated from source within Layout GXL, and the result is shown in Figure 12. Surprisingly, even at this scale, the $2 \times 2$ BJT device (the smallest one in the PDK) still dominates in single device size. As auto-generated, the floorplan is 157.64 $\mu$m square, yielding an area of 24 850.37 $\mu m^2$. As evidenced in Figure 12, there is quite a lot of room for this design to be compacted in layout, or ample space for decap should the designer prefer.

# 5 Conclusion

For more or less trusting the math laid out by Gregoire on the operation of this circuit, the results obtained by scaling it for the 150 nm PDK and upping the operation speed accordingly appear to be relatively admirable. Benefits of scaling a switched-capacitor design to a small-$\lambda$ process are non-negligible and are evidenced in the low output resistance. The extremely solid DC output indicates that the flyback and filter capacitors can be further reduced in size if desired to improve startup time, and possibly be made small enough to integrate on-chip due to running at 100 MHz instead of the 3 kHz in [3], which required the bigger capacitors. Approaching this design problem definitely exposed the author to plenty of new areas and ideas in IC design, and there is definitely more work to be done for optimization. Future work on this project would be to incorporate a local clock generator (Johnny or Weston's VCO?) and see how temperature changes cause frequency and output variations, optimize the duty cycle, and fully bootstrap the design so that the 250 $\mu$A reference current is provided within this circuit as well, since this would likely be one of the first blocks to receive power within a portable device.

## References

[1] C. Huang, "I thought the pn junction was just a thought experiment," 2024, correspondence in RIT VLSI Laboratory.

[2] B. R. Gregoire, "A switched capacitor regulated charge pump power supply," vol. 2005. IEEE, 2005. doi: 10.1109/CICC.2005.1568778. ISBN 0-7803-9023-7. ISSN 08865930 pp. 750–753.

[3] B. R. Gregoire, "A compact switched-capacitor regulated charge pump power supply," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 1944–1953, 8 2006. doi: 10.1109/JSSC.2006.875303

[4] E. Sackinger and W. Guggenbuhl, "A high-swing, high-impedance mos cascode circuit," *IEEE Journal of Solid-State Circuits*, vol. 25, pp. 289–298, 1990. doi: 10.1109/4.50316

[5] P. Vajpayee, A. Srivastava, S. Rajput, and G. Sharma, "Low voltage regulated cascode current mirrors suitable for sub-1v operation." IEEE, 12 2010. doi: 10.1109/APCCAS.2010.5774891. ISBN 978-1-4244-7454-7 pp. 584–587.

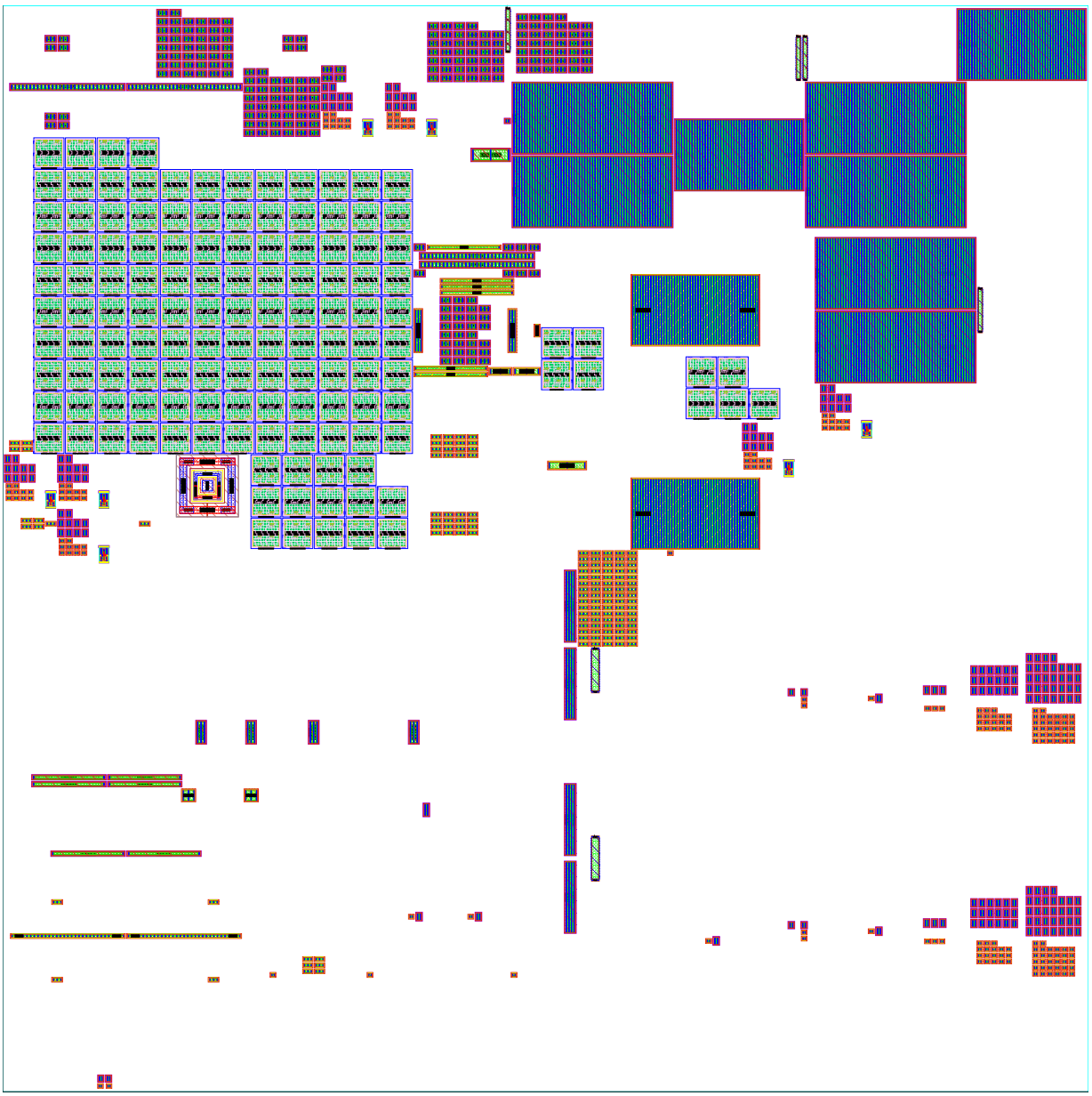

**Figure 12:** Device layouts as auto-generated in Layout GXL.