## 3-Bus Harvard Memory-Mapped RISC Processor ASM Chart Chris Biancone, October 2021 MC0 (IF) MC1 (ID) $IR \leftarrow \mathbf{PM}[PC]$ ${ m CU~decodes~IW}$ PC++ADD2 ADDY $R_{SD} \leftarrow R_{SD} + R_{S}$ 0000 $SR \leftarrow CNVZ$ N SUB2SUB $R_{SD} \leftarrow R_{SD} - R_S$ 0001 $SR \leftarrow CNVZ$ N INC Y $R_{SD} \leftarrow R_{SD} + IW[1:0]$ 0010 $SR \leftarrow CNVZ$ N DEC2 $\mathbf{DEC}$ $R_{SD} \leftarrow R_{SD} - IW[1:0]$ $SR \leftarrow CNVZ$ 0011 N XOR2 XOR $R_{SD} \leftarrow R_{SD} \oplus R_S$ 0100 $SR \leftarrow CNVZ$ ANDY $R_{SD} \leftarrow R_{SD} \&\& R_S$ 0101 $SR \leftarrow CNVZ$ N OR2 $\mathbf{OR}$ $R_{SD} \leftarrow R_{SD} \parallel R_S$ 0110 $SR \leftarrow CNVZ$ N CPY2 $\mathbf{CPY}$ $R_{SD} \leftarrow R_{S}$ 0111 $SR \leftarrow CNVZ$ N SHRA2 $\mathbf{SHRA}$ $R_{SD} \leftarrow R_{SD} >> IW[1:0]$ 1000 $SR \leftarrow CNVZ$ N SHRL2 $\mathbf{SHRL}$ $R_{SD} \leftarrow R_{SD} >>> IW[1:0]$ 1001 $SR \leftarrow CNVZ$ N RRC2RRC $R_{SD} \leftarrow R_{SD} \text{ rrc } R_S$ 1010 $SR \leftarrow CNVZ$ N LD3 $MAB \leftarrow \{PM[PC], 2'b00\}$ IF (MAR > 0x3FD)LD $MAR \leftarrow MAB + MAX$ 1011 PC + + $R_{SD} \leftarrow IPDR$ $IPDR \leftarrow IP$ $ELSE\ R_{SD} \leftarrow DM[MAR]$ $MAX \leftarrow \{R_S[0], R_S[0], R_S\}$ N ST2ST4 $MAB \leftarrow \{PM[PC], 2'b00\}$ IF (MAR > 0x3FD) $\mathbf{ST}$ PC + + $OPDR \leftarrow R_{SD}$ 1100 $MAR \leftarrow MAB + MAX$ $ELSE\ DM[MAR] \leftarrow R_{SD}$ $MAX \leftarrow \{R_S[0], R_S[0], R_S\}$ N JMP4TakenJMP2Y $PC \leftarrow MAR$ $MAB \leftarrow \{PM_{out}[7],$ JMP3 $\mathbf{JMP}$ $PM_{out}[7], PM[PC]$ MSB == 1? $MAR \leftarrow MAB + MAX$ 1101 $MAX \leftarrow PC$ !JMP4TakenPC + +Ν $PC \leftarrow PC$ N POP POP2 $R_{SD} \leftarrow TOS$ 1110 N PUSH PUSH2 $TOS \leftarrow R_{SD}$ 1111 N