Chris Biancone

BS/MS Electrical Engineering **J** (973) 896-0255

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About

Fourth-year EE student at RIT; DoD SMART Scholar. I have background in the semiconductor, embedded systems, and defense industries, and extensive experience working on multidisciplinary teams.

I am black belt and have a passion for playing music, hiking, and designing for a sustainable future.

Education

Rochester Institute of Technology

GPA: 3.64 2019 - Present BS/MS Electrical Engineering with focus in MEMS

Pope John XXIII HS

GPA: 4.26 2015 - 2019 MIT Zero Robotics Captain FTC Robotics

Skills

Altium; Quartus; SPICE; Mentor Graphics; Solidworks; AutoCAD; Excel

C(++); Python; MATLAB; Assembly; Java; Lagrange ETFX; Bash

➤ Agile Development; Semiconductor Design; Additive Manufacturing; Scanning Electron Microscopy

Experience

DEVCOM AC

Armored Vehicle Fire Control Systems

May 2021 -- Present Picatinny Arsenal, NJ Assist development of next-generation medium caliber gun control systems. Apply knowledge of real-time processing, control systems, and military design requirements. Support obsolescence mitigation for Abrams tanks.

RIT / NSF

MEMS Device Research

January 2021 -- Present Rochester, NY Developed novel process flow for manufacturing sensor array of previously unattained sensitivity. Testing to improve current microfluidic models for pumpless cooling of electronics.

RoNetco

Information and Electronics Technologies

June 2019 -- September 2020 Ledgewood, NJ Designed and documented network room fire suppression system. Drafted AutoCAD drawings for construction. Improved efficiency by automating the transition from Windows 7 to 10.

Projects

RISC CPU

Verilog Harvard architecture CPU implemented in hardware on Altera FPGA. Wrote Python assembler for full development stack control.

MSP430 Oscilloscope

Created a functional portable oscilloscope using Assembly algorithms. Uses capacitive touchpad for input and LEDs and UART for display.

Mandelbrot Set Render

Efficiently rendered Mandelbrot Fractal in C++ with colorization and vector-mapping. Integrating with custom thread pool.