Chris Biancone

BS/MS Electrical Engineering

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About

Fifth-year EE student at RIT proficient in analog and mixed signal electronics design and instruction. Experienced CAD tools such as Cādence, Altium, and MATLAB for microelectronics, control system, and SDR system design. Currently conducting research into biophysical effects of DC magnetic fields and semiconducting properties of neurons for publication in a graduate paper.

I am an Isshin-Ryu black belt and enjoy hiking and mountain biking. I have recently combined a love of music with my knowledge in analog electronics design to design a high-tolerance differential RIAA preamplifier.

Education

Rochester Institute of Technology

GPA: 3.7 2019 – Present

BS/MS Electrical Engineering with MS focus in MEMS

Skills

- Cādence Virtuoso, Altium, COMSOL, SPICE, Simulink
- C++, Python, MATLAB, LaTeX
- Analog / Mixed Signal Design, MEMS Fabrication, GTAW & GMAW Welding
- Agile Development Methodology, Technical Instruction

Experience

Control Systems Internship
Summers 2021 – Pres.

Armored Vehicle Fire Control — Picatinny Arsenal, NJ

Managed the re-engineering of an unmanned ground vehicle electrical system to include failure modes. Investigated the adaptation of existing hardware to an open Ethernet standard. Supported the development of next-generation fire control for medium caliber systems.

Graduate Teaching Assistant
January 2023 – Pres.

Analog Electronics — RIT

Instructed and assisted students in RIT's EE480 Analog Electronics lab. Exercises include SPICE and hardware characterization and simulation of diode circuits and multistage BJT/MOSFET amplifiers.

Undergraduate Research
January 2021 – Pres.

Microfluidics MEMS — RIT & NSF

Developed novel process flow for manufacturing piezoresistive diaphragm array with 200 nm thickness. Packaging and testing for use to improve current microfluidic models for pumpless cooling of electronics.

Projects

RTR Fully-Differential Op-Amp

Developed and simulated post-layout a novel auto-biasing architecture for a 3-stage folded cascode differential op-amp, achieving a 13 dB improvement in linearity over other rail-to-rail designs. Pursuing IP protection or publication.

RTR StrongARM Comparator

Modified the StrongARM dynamic comparator architecture to process signals above and below the voltage supply for application in flash and SAR ADCs. Achieved 890 μV resolution at 1 GHz operation with 260 pA quiescent current draw and 16 μm by 10 μm layout area.

8-bit RISC CPU

Designed a Harvard-architecture CPU with Memory-Mapped I/O and 16 instructions, described in Verilog. Wrote custom assembler in python to verify syntax and translate Assembly into program files.