The Cabling Scheme and DSM Algorithms for the EMC Trigger

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Change Log:

Date	Description
January 11th, 2009	First complete version
January 12th, 2009	For each algorithm there is now a list of which DSMS use that algorithm
March 25th, 2009	All layer 0 algorithms (BE001, BE003, BW001, BW003, EE001, EE002) have the "overflow protection" removed, so input values of 63 are no longer ignored. This is the "b" version of all those algorithms
August 5th, 2009	Updated the description of the layer 2 algorithm to include the list of which bits were sent to the scalar system.
April 5, 2010	Added page numbers to this document and re-formatted the table containing the output of EM201 to help with downstream trigger configuration file management.
December 20, 2010	Modified the EM201 algorithm for 2011. The JP0 bit for the full calorimeter (BEMC+EEMC+overlap) was added into the output list.
January 18, 2011	Fixed name of Bit 9 in the EM201 output. BJP1 is really BJP2. Logic was always correct, just the documentation was wrong.
January 12, 2012	Changes for 2012 running. Added a register to BC101 algorithm to select one of four HT thresholds, and pass all the bits on to the new EM202 DSM. Added four registers to the EM201 algorithm; one to select which JP threshold is used in the AJP logic and the others for controlling the DAQ10k logic. Finally created the EM202 algorithm, to make a TPC bitmask based on the selected BEMC HT bits.
February 17, 2015	Changes for 2015 pp running. At layer-0 the 4th BEMC HT bit has been re-purposed to make an HT.TP bit. At layer-2 (EM201) these bits are combined to make a back-to-back topology bit for triggering on J/Ψ. The layer-1 algorithm, which just passes through the relevant bits, is unchanged from January 12, 2012.

Eta-Phi Coverage

The EMC trigger operates on fixed jet patches that overlap in eta but not in phi. The detector is connected to the DSM tree in such a way that each BEMC layer 0 DSM board receives a 6-bit ADC value from each of 10 trigger patches. Each trigger patch covers a region of eta-phi space measuring (0.2x0.2). The assignment of trigger patches to layer 0 DSM boards is done so that each layer 0 DSM board covers a region measuring (1x0.4). Calculating the energy in any (1x1) jet patch requires summing up the ADC values from all 25 trigger patches within that patch. This therefore involves combining data from several layer 0 DSM boards.

The experience of the first few years showed that it is not necessary to pass full-range, full-resolution sums from layer 0 to layer 1. We can select just the lower 6 bits from each sum with overflow logic to indicate when any higher order bits are set. This makes it possible for each layer 0 DSM board to pass the sums from at least two groups of trigger patches to layer 1. As a result, it is possible to calculate the energy for overlapping (1x1) jet patches. This is illustrated in Figure 1, which shows a (2x2) region of eta-phi space. The thin solid lines indicate which areas are connected to each layer 0 DSM board. There are 10 layer 0 DSM boards in this diagram; 5 at negative eta and 5 at positive eta. The thick lines indicate which areas are then connected to each layer 1 DSM board. The dashed lines (both thick and thin) show how each layer 0 DSM board splits its trigger patches into sub-groups.

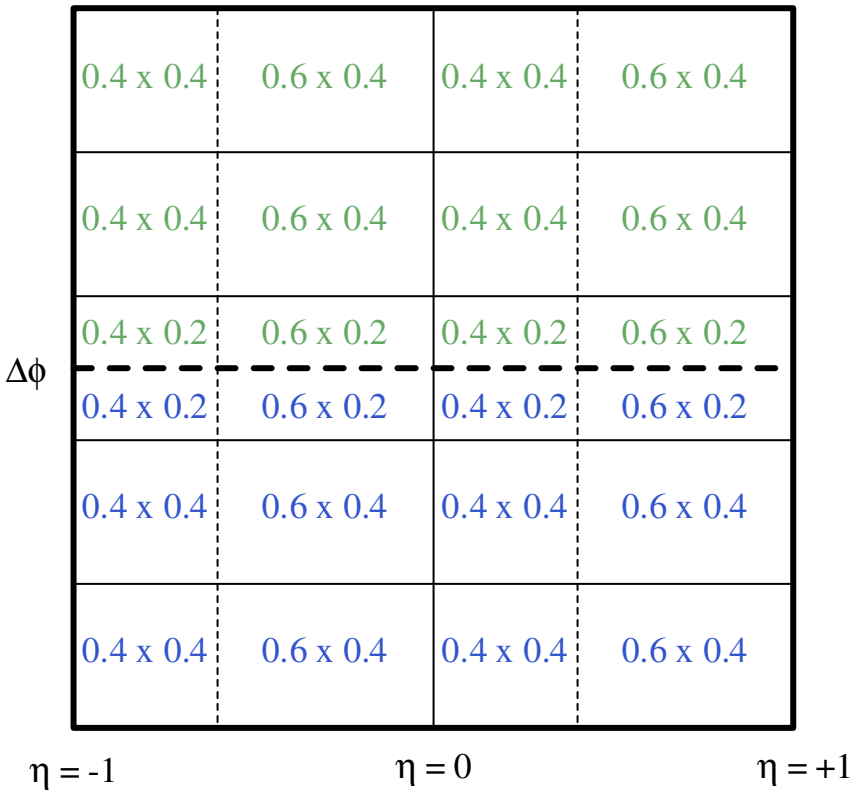

Figure 1: The BEMC DSM Eta-Phi Scheme

It can be seen that the two DSM boards covering the central phi region actually split their patches into four small groups, covering either a (0.6x0.2) region or one measuring (0.4x0.2). The other eight DSM boards split their patches into just two groups, making a (0.6x0.4) region and a (0.4x0.4) region. Each DSM board can put the 6-bit sums from two groups onto one output cable. This means the two DSM boards covering the central phi region must use both output cables to pass on the sums from all four of their groups.

The layer-0 to layer-1 connections are then arranged so that positive and negative eta regions at a given phi-value all go to the same layer 1 DSM board. It can be seen that the two output cables from the DSM boards covering the central phi region go to different layer 1 DSM boards. Every layer 1 DSM board receives 12 input sums covering an area measuring (2x1) in total. It combines these sums to make three overlapping (1x1) jet patches. It also makes a partial jet patch that is completed at layer 2 using data from the EEMC DSM tree. This eliminates acceptance gaps in eta, but leaves acceptance gaps in phi.

BEMC Cabling Detail

Figure 2 shows the detail of the cabling scheme. As in Figure 1, the middle section of the diagram shows the (2x2) region of eta-phi space. The solid lines indicate which areas are connected to each layer 0 DSM board and the dashed lines outline the individual trigger patches. The long-dashed lines show how each layer 0 DSM will split its channels into two eta groups. In the central phi region, the numbers show how the trigger patches are connected to the ten input channels of the layer 0 DSM boards. The sidebars show how the layer 1 DSM boards are connected to the layer 0 boards so that each one receives data from both East and West sides of the detector. The East-side layer 0 DSM boards connect to the even-numbered channels of the layer 1 boards, and the West-side layer 0 boards connect to the odd-numbered channels. It can be seen that there is a difference in the cabling of the upper (in this diagram) and lower layer 1 DSM boards. The upper layer 1 DSM board receives data from the single–output layer 0 DSM boards on channels 0:3, and the data from the double-output boards on channels 4 and 5. The lower layer 1 DSM board receives the data from the double-output boards on channels 0 and 1, and the single-output boards on the other channels. Since the format of the data is always the same the cabling difference does not matter, and all of the layer 1 DSMS are able to use the same algorithm.

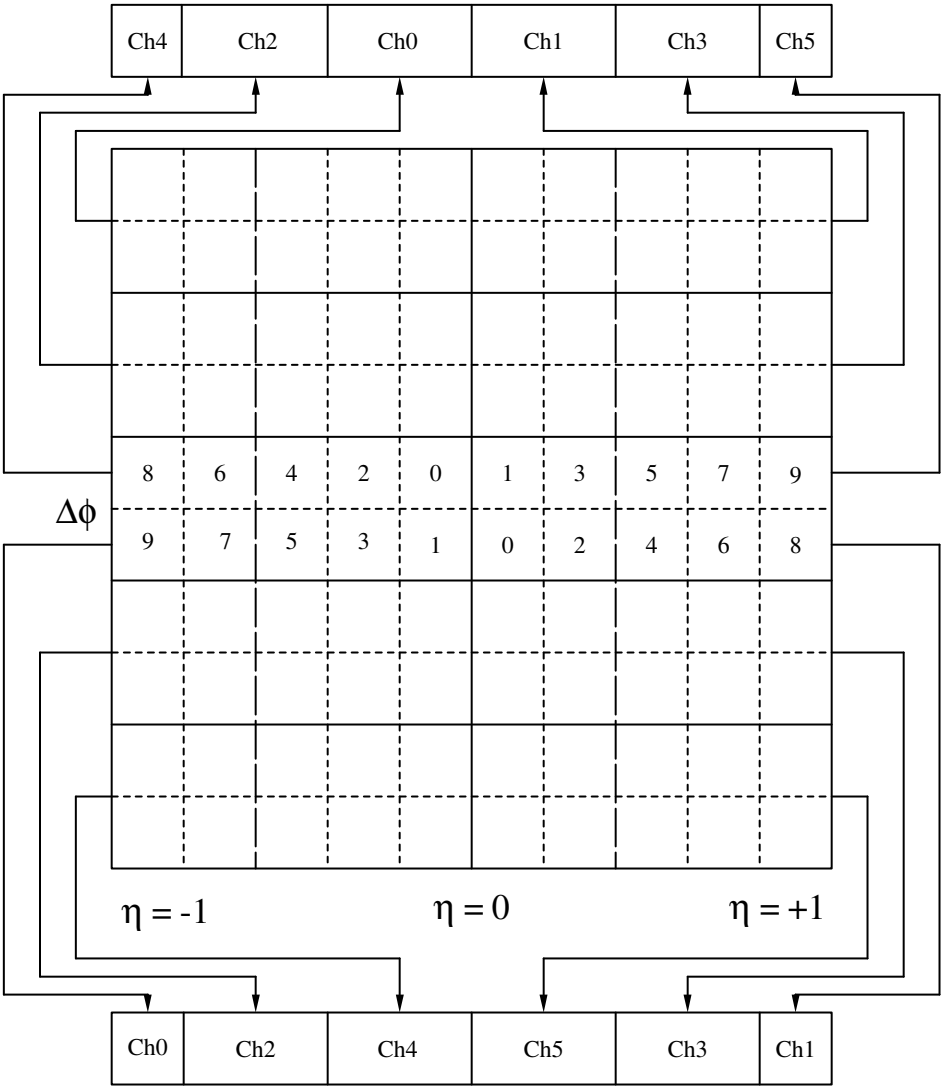

Figure 2: BEMC Cabling Scheme

BEMC Layer 0 Algorithm Description

From Figure 2 it can be seen that it will be necessary to have four different algorithms for the layer 0 DSM boards: single-output East (negative eta), single-output West (positive eta), double-output East and double-output West. It should be noted that, as well as summing different groups of channels, the double-output layer 0 algorithms also switch their output mapping between the East and West sides.

Single-output East

- RBT File: bemc_be001_2015_a.rbt
- Users: BE001:BE002, BE004:BE007, BE009:BE012, BE014:BE105
- Input: 10 BEMC channels: bits 0:5 = high tower, bits 6:11 = trigger patch

- LUT: Pedestal subtraction and energy calibration is done in the BEMC read-out electronics. Therefore the LUT's are mostly 1-to-1. Missing, dead and non-instrumented channels are zeroed out here.
- Registers: Five registers, each containing one 6-bit threshold value for either the high tower comparison or the trigger patch comparison. These are NOT size ordered.
    - R0: BEMC-HT-th0 (6 bits)
    - R1: BEMC-HT-th1 (6)
    - R2: BEMC-HT-th2 (6)
    - R3: BEMC-HT-th3 (6)
    - R4: BEMC-TP-th0 (6)
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Step 2: Sum TP channels 0:5 (low eta) and 6:9 (high eta).
  Compare each HT value to 4 thresholds and each TP value to 1 threshold.
- Step 3: Subtract the pedestal from each TP sum. The pedestal is defined as (N-1) where "N" is the number of channels that were added together to make the TP sum. If the initial TP sum is less than N, then the result of the pedestal subtraction process shall be zero. Next, select the lower 6 bits of each pedestal-subtracted TP sum. Set all 6 bits high (63) if any higher-order bits are set in the pedestal-subtracted sum.
  Combine (OR) the HT bits for each of thresholds 0:2 together.
  Make the HT.TP bit for each channel by combining (AND) the HT-th3 and TP bits, and then OR the results from all 10 channels.
- Step 4: Send the two 6-bit sums (low and high eta), the 3 HT bits and the 1 HT.TP bit to layer 1 on one output cable.

Single-output West

- RBT File: bemc_bw001_2015_a.rbt
- Users: BW001:BW002, BW004:BW007, BW009:BW012, BW014:BW105
- Input: Same as Single-output East algorithm
- LUT: Same as Single-output East algorithm
- Registers: Same as Single-output East algorithm
- Algorithm: Same as Single-output East algorithm, except the low and high eta TP sums at Step 2 involve channels 0:3 and 4:9 respectively, instead of 0:5 and 6:9.

Double-output East

- RBT File: bemc_be003_2015_a.rbt
- Users: BE003, BE008, BE013
- Input: Same as Single-output East algorithm
- LUT: Same as Single-output East algorithm
- Registers: Same as Single-output East algorithm
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Step 2: Sum TP channels in four groups: 0, 2 and 4 (low eta), 6 and 8 (high eta), 1, 3 and 5 (low eta) and 7 and 9 (high eta).
  Compare each HT value to 4 thresholds and each TP value to 1 threshold.

- Step 3: Subtract the pedestal from each TP sum and then select the lower 6 bits, as in the single-output East algorithm.
  Combine (OR) the HT bits from each of thresholds 0:2 from the even-numbered input channels and the odd-numbered input channels separately.
  Make the HT.TP bit for each channel by combining (AND) the HT-th3 and TP bits, and then OR the results from the even- and odd-numbered channels separately.
- Step 4: Send the two 6-bit sums (low and high eta), the 3 HT bits and the 1 HT.TP bit from the even-numbered channels to the upper (in Figure 2) layer 1 DSM board on the first output cable. Send the data from the odd-numbered channels to the lower DSM board on the second output cable.

Double-output West

- RBT File: bemc_bw003_2015_a.rbt
- Users: BW003, BW008, BW013
- Input: Same as Single-output East algorithm
- LUT: Same as Single-output East algorithm
- Registers: Same as Single-output East algorithm
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Step 2: Sum TP channels in four groups: 0 and 2 (low eta), 4, 6 and 8 (high eta), 1 and 3 (low eta) and 5, 7 and 9 (high eta).
  Compare each HT value to 4 thresholds and each TP value to 1 threshold..
- Step 3: Subtract the pedestal from each TP sum and then select the lower 6 bits, as in the single-output East algorithm.
  Combine (OR) the HT bits from each of thresholds 0:2 from the even-numbered input channels and the odd-numbered input channels separately.
  Make the HT.TP bit for each channel by combining (AND) the HT-th3 and TP bits, and then OR the results from the even- and odd-numbered channels separately.
- Step 4: Send the two 6-bit sums (low and high eta) and the 4 HT bits from the even-numbered channels to the ***lower*** layer 1 DSM board on the ***second*** output cable. Send the data from the odd-numbered channels to the ***upper*** DSM board on the ***first*** output cable. (NOTE: Bold italics indicate the difference in output mapping between this algorithm and the East-side algorithm).

In all four algorithms the output data on each cable will therefore have the same format, which is shown in Table 1:

Table 1: Output of Layer 0 BEMC DSM Boards

Data	Bit Range	Bit Count	Bit Total
TP sum for low-eta group	0:5	6	16
TP sum for high-eta group	6:11	6	
HT bits	12:14	3	
HT.TP bit	15	1	

BEMC Layer 1 Algorithm Description

There is just one layer-1 algorithm for the BEMC, which will be used by all 6 DSM boards. For 2012 that algorithm has been updated to drive data to the new EM202 DSM on the second output cable for the DAQ10k project.

- RBT File: bemc_bc101_2012_a.rbt
- Users: BC101:BC106
- Input: 6 channels, each with the format given in Table 1
- LUT: 1-to-1 mapping
- Registers: Four registers. Each of the first three registers contains one 9-bit threshold value for the jet patch comparison. As in the past, these are SIZE-ORDERED, so th0 < th1 < th2. The fourth register selects one of the four HT bits from each channel to be passed to EM202
    - R0: BEMC-JP-th0 (9 bits)
    - R1: BEMC-JP-th1 (9)
    - R2: BEMC-JP-th2 (9)
    - R3: BEMC-DAQ10k-HT-Sel (2)
- Step 1: Receive two 6-bit TP sums (low and high eta), 3 HT bits and 1 HT.TP bit on each of 6 cables. Four of the cables come from single-output layer 0 DSM boards. The other two cables come from two different double-output layer 0 DSM boards. The low and high eta sums will be referred to as ChX_{LO} and ChX_{HI} to indicate which channel, and which eta range, are being selected.
- Step 2: Calculate 3 jet patches sums as follows:
    - JPX ($-1 < \eta < 0$) = $Ch0_{LO} + Ch0_{HI} + Ch2_{LO} + Ch2_{HI} + Ch4_{LO} + Ch4_{HI}$
    - JPY ($-0.6 < \eta < 0.4$) = $Ch0_{LO} + Ch1_{LO} + Ch2_{LO} + Ch3_{LO} + Ch4_{LO} + Ch5_{LO}$
    - JPZ ($0 < \eta < 1$) = $Ch1_{LO} + Ch1_{HI} + Ch3_{LO} + Ch3_{HI} + Ch5_{LO} + Ch5_{HI}$

  In parallel, calculate the partial jet patch sum to be combined with the EEMC data at layer 2:
    - JPpartial ($0.4 < \eta < 1$) = $Ch1_{HI} + Ch3_{HI} + Ch5_{HI}$

  Combine (OR) the HT bits from input channels 0:2 and 3:5 separately.
  Combine (OR) the HT.TP bits from input channels 0:2 and 3:5 separately.
  In parallel, use register 3 to select one of the HT or HT.TP bits from each of the 6 input channels
- Step 3: Compare each of JPX, JPY and JPZ to three thresholds and then pack the results for each jet patch into a 2-bit integer (this is the same logic as has been used for many years now).
  Select the lower 6 bits of JPpartial, and set all bits high (63) if any of the higher order bits of JPpartial are set.
  Combine (OR) the two intermediate groups of HT and HT.TP bits together.
  Also, delay the 6 HT bits selected for the DAQ10k logic to the 4^{th} step.
- Step 4: Send the 2-bit integer for each of the three completed jet patches, along with the HT and HT.TP bits and 6 bits of JPpartial to the first layer-2 DSM board (EM201).
  In parallel send the 6 selected HT bits to the other layer 2 DSM board (EM202) for the DAQ10k project. The output data format is shown in Table 2.

Table 2: Output of Layer 1 BEMC DSM Boards

Data	Cable	Bit Range	Bit Count	Total
JPX threshold bits	0	0:1	2	16
JPY threshold bits		2:3	2	
JPZ threshold bits		4:5	2	
JPpartial sum		6:11	6	
HT bits		12:14	3	
HT.TP nit		15	1	
DAQ10k HT bits	1	0:5	6	6

EEMC Cabling Detail

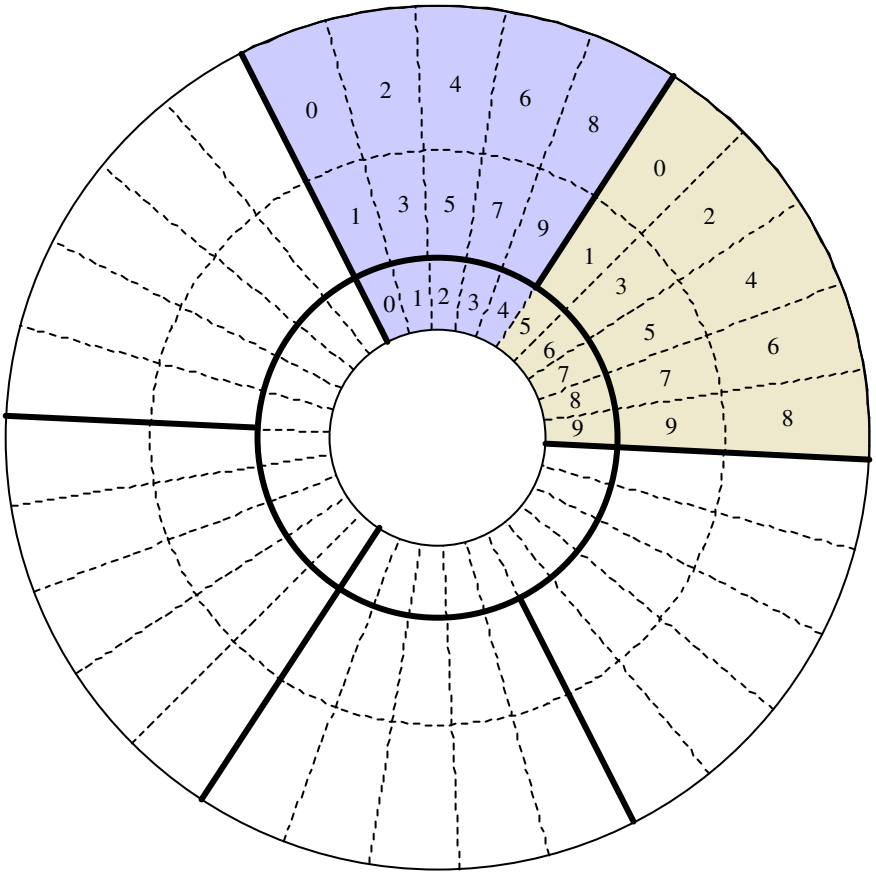

Figure 3: EEMC DSM Eta-Phi Scheme, seen from the West looking towards the center of STAR

Figure 3 shows how the EEMC trigger patches are connected to the layer 0 DSM boards, as seen from the West looking towards the center of STAR. The thick solid lines indicate which areas are connected to each layer 0 DSM board. The thin dashed lines outline the

individual trigger patches. A pair of adjacent jet patches is highlighted. The numbers indicate which layer 0 DSM board channel is connected to each trigger patch.

It can be seen that every EEMC (1x1) jet patch is split between two layer 0 DSM boards. In each case, the 10 outer trigger patches (lowest eta) are connected one layer 0 DSM board, and the 5 inner trigger patches (highest eta) are connected to another layer 0 DSM board. That second board also contains the five inner trigger patches for the adjacent jet patch. In this cabling scheme the boards that cover the outer trigger patches each have one output cable. The boards that cover the inner trigger patches of two jet patches have two output cables. The result is twelve cables which are split between two layer 1 DSM boards in such a way that each of the layer 1 DSM boards covers half of the EEMC.

The aim of the cabling and algorithm scheme is to make (1x1) jet patches that overlap in eta. The EEMC only covers one unit of eta so all that is possible is to make one internal (1x1) jet patch and a partial (0.4x1) jet patch on the EEMC-BEMC boundary that can be combined with the partial jet patch (JPpartial) from the BEMC side of the boundary. The EEMC cabling scheme is therefore set up to construct (1x1) jet patches with the same phi range as in the BEMC. The partial (0.4x1) jet patch is constructed by summing together the even numbered channels of the single-output layer 0 DSMS (which cover the low eta part of the EEMC).

The EEMC layer 0 algorithms differ from the BEMC algorithms primarily in the definition of which groups of channels are added together to make the TP sums. The single-output EEMC layer 0 DSM boards add together the even-numbered (low eta) channels in one group, and the odd-numbered (high-eta) channels in another group. The low eta group forms the partial jet patch that can be combined with the BEMC partial jet patch at layer 2. The double-output EEMC layer 0 DSM boards add together channels 0:4 in one group, and channels 5:9 in the other (as indicated in Figure 3). However, there is an additional difference associated with the pedestal subtraction. The BEMC layer 0 algorithms do the pedestal subtraction such that each TP sum is left with a residual pedestal of 1. Six TP sums are added together to make a jet patch, so the BEMC jet patch pedestal value is 6. Only three TP sums are added together to make the partial jet patch (JPpartial), so it's pedestal value is 3. In order to simplify later analysis it would be useful to ensure that all jet patches, including those that come from the EEMC and the BEMC-EEMC boundary, also have a pedestal value of 6. To this end, the pedestal subtraction in the EEMC layer 0 algorithms is done as shown in Table 3. Note that "N" is still the number of channels that are added together to make the TP sum, just like in the BEMC logic. In the case of the EEMC algorithms, "N" is always 5.

Table 3: TP sum Pedestal Calculations in the EEMC Layer 0 Algorithms

TP Sum	Pedestal Subtraction Equation	Residual Pedestal
Low eta sum from single-output DSM	TPsum = TPsum-(N-3)	3
High eta sum from single-output DSM	TPsum = TPsum-(N-2)	2
Sum from double-output DSM	TPsum = TPsum-(N-1)	1

When the three sums listed in Table 3 are added together to make an internal EEMC jet patch the total pedestal value of the jet patch is 6, which matches the BEMC. When the low eta sum from the single-output DSM is added to JPpartial, from the BEMC, to complete the boundary-spanning jet patch, the total pedestal for that jet patch also comes to 6, again matching the BEMC.

EEMC Layer 0 Algorithm Description

Single-output (Low Eta)

- RBT File: eemc_ee001_2009_b.rbt
- Users: EE001, EE003, EE004, EE006, EE007, EE009
- Input: 10 EEMC channels: bits 0:5 = high tower, bits 6:11 = trigger patch
- LUT: Pedestal subtraction and energy calibration is done in the EEMC read-out electronics. Therefore the LUT's are mostly 1-to-1. Missing, dead and non-instrumented channels are zeroed out here.
- Registers: Two registers, each containing one 6-bit threshold value for the high tower comparison. Unlike in the past, these are NOT size ordered.
    - R0: EEMC-HT-th0 (6 bits)
    - R1: EEMC-HT-th1 (6)
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Step 2: Sum the five even numbered (low eta) TP channels and the five odd numbered (high eta) channels separately. In parallel with the sum logic, compare each HT value to 2 thresholds. Note that in the past this comparison had included logic to ignore HT values of 63 (i.e. all bits high) because this value could be produced by a broken input connection. Those bad channels are now zeroed out in the LUT upstream of this algorithm. So, starting with this "b" version of the algorithm, that extra logic has been removed and what is left is a simple comparison of two numbers: the HT value and the threshold.
- Step 3: Subtract the pedestal from each TP sum. The pedestal subtraction equations are described in Table 3. If the initial TP sum is less than N (5), then the result of the pedestal subtraction process shall be zero. Next, select the lower 6 bits of each pedestal-subtracted TP sum. Set all 6 bits high (63) if any higher-order bits are set in the pedestal-subtracted sum. In parallel with this, combine (OR) the HT bits together.
- Step 4: Send the two 6-bit TP sums (low and high eta) and the 2 HT bits to layer 1 on one output cable.

Double-output (High Eta)

- RBT File: eemc_ee002_2009_b.rbt
- Users: EE002, EE005, EE008
- Input: Same as Single-output (Low Eta)
- LUT: Same as Single-output (Low Eta)
- Registers: Same as Single-output (Low Eta)

- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Step 2: Sum the TP channels in two groups: (0:4) and (5:9). In parallel with the sum logic, compare each HT value to 2 thresholds. Note that in the past this comparison had included logic to ignore HT values of 63 (i.e. all bits high) because this value could be produced by a broken input connection. Those bad channels are now zeroed out in the LUT upstream of this algorithm. So, starting with this "b" version of the algorithm, that extra logic has been removed and what is left is a simple comparison of two numbers: the HT value and the threshold.
- Step 3: Subtract the pedestal from each TP sum using the equation from Table 3, and then select the lower 6 bits, as in the single-output (low eta) algorithm. In parallel with this, combine (OR) the HT bits from channels (0:4) and (5:9) separately.
- Step 4: Send the 6-bit sum and the 2 HT bits from channels (0:4) to layer 1 on the first output cable. On the cable, the sum will be in the bit range used by the low-eta sum in the single-output algorithm. The bits assigned to the high-eta sum will be set to zero. Send the data from channels (5:9) to layer 1 on the second output cable.

In both algorithms the output data on each cable have similar formats, as shown in Table 4:

Table 4: Output of Layer 0 EEMC DSM Boards

Data	Bit Range	Bit Count	Bit Total
TP sum for low-eta group	0:5	6	16
TP sum for high-eta group (N/A, set to zero, for the double-output algorithm)	6:11	6	
HT bits	12:13	2	
Unused	14:15	2	

EEMC Layer 1 Algorithm Descriptions

The two EEMC layer 1 DSM boards have slightly different algorithms due to a feature of the layer-0 to layer-1 connection scheme. These connections are shown in Figure 4. As in Figure 3, the thick solid lines indicate which areas are connected to each layer 0 DSM board. The dashed lines show how the inner regions are split by the layer 0 DSM boards to make pieces of two adjacent jet patches. The arrows show how the outputs of the layer 0 DSM boards (including both outputs from the double-output boards) connect to the input channels of the two layer 1 DSM boards.

It can be seen that the layer 1 DSM board covering the bottom half of the EEMC (EE101) receives data from the outer (low eta) parts of its jet patches on input channels 0, 3 and 4. It is therefore these channels that will provide the partial jet patch information that needs to be passed up to layer 2. However, the layer 1 DSM board covering the upper half of the EEMC (EE102) receives data from the outer parts of its jet patches on input channels

1, 2 and 5, so it is these channels that will provide the partial jet patch information. The two layer 1 DSM board algorithms are therefore slightly different, to account for this difference in the input mapping.

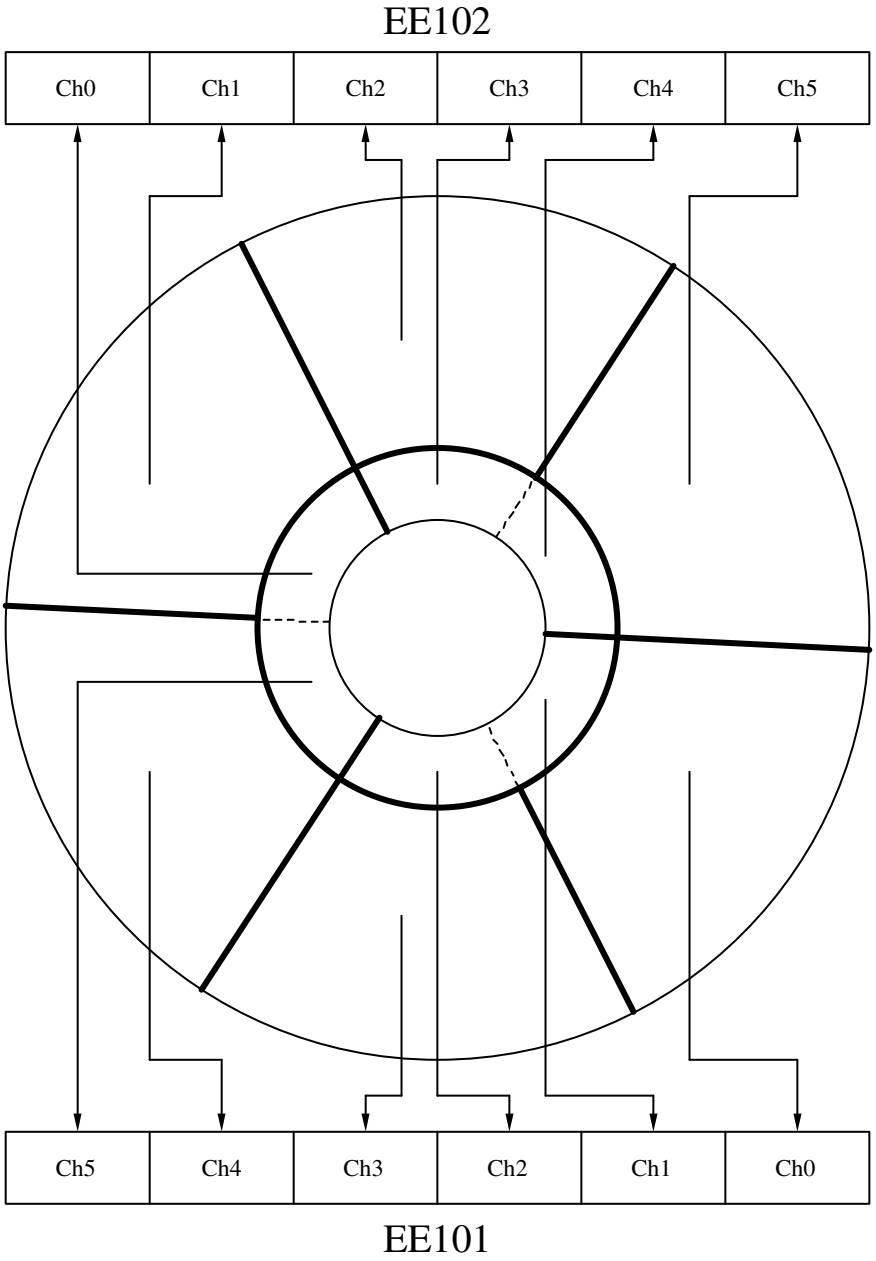

Figure 4: The EEMC Cabling Scheme, with the Endcap seen from the West looking toward the center of STAR.

Lower Half (EE101)

- RBT File: eemc_ee101_2009_a.rbt
- User: EE101

- Input: 6 channels, each with the format given in Table 4 (see Page 11)
- LUT: 1-to-1 mapping
- Registers: Three registers, each containing one 8-bit threshold value for the jet patch comparison. As in the past, these are SIZE-ORDERED, so th0 < th1 < th2
    - R0: EEMC-JP-th0 (8 bits)
    - R1: EEMC-JP-th1 (8)
    - R2: EEMC-JP-th2 (8)
- Step 1: Receive two 6-bit TP sums (low and high eta) and 2 HT bits on each of six cables. Three of these cables (channels 0, 3 and 4) come from single-output layer 0 DSM boards. The other three cables (channels 1, 2 and 5) come from double-output layer 0 DSM boards, and on those cables the second 6-bit TP sum will always be zero. The sums will be referred to as ChX_{LO} and ChX_{HI} to indicate which channel, and which eta range, are being selected.
- Step 2: Calculate 3 jet patches sums as follows:
    - JPA (4 o'clock) = $Ch0_{LO} + Ch0_{HI} + Ch1_{LO}$
    - JPB (6 o'clock) = $Ch3_{LO} + Ch3_{HI} + Ch2_{LO}$
    - JPC (8 o'clock) = $Ch4_{LO} + Ch4_{HI} + Ch5_{LO}$

  In parallel, compare pairs of the low eta sums arriving from the single-output layer 0 DSM boards (i.e. $Ch0_{LO}$, $Ch3_{LO}$ and $Ch4_{LO}$). Also combine (OR) the HT bits from input channels 0:2 and 3:5 separately.
- Step 3: Combine (OR) the two intermediate groups of HT bits together. Compare each of JPA, JPB and JPC to three thresholds and then pack the results for each jet patch into a 2-bit integer (this is the same logic as has been used for many years now). Combine the results of the 2-channel comparisons (calculated at Step 2) to select the largest low eta sum.
    - A (4 o'clock) = ($Ch0_{LO} > Ch3_{LO}$) and not ($Ch4_{LO} > Ch0_{LO}$)
    - B (6 o'clock) = ($Ch3_{LO} > Ch4_{LO}$) and not ($Ch0_{LO} > Ch3_{LO}$)
    - C (8 o'clock) = ($Ch4_{LO} > Ch0_{LO}$) and not ($Ch3_{LO} > Ch4_{LO}$)

  This is the partial jet patch that will be sent on to layer 2. Note that if all three low eta sums are the same (e.g. in an event where nothing happens) then all three comparisons will be false. In this case, sum A, at 4 o'clock, is selected. Use a 2-bit integer to indicate which of the three sums has been selected.
    - 1 = A (4 o'clock)
    - 2 = B (6 o'clock)
    - 3 = C (8 o'clock)
- Step 4: Send, to layer 2, the 2-bit integer for the three completed jet patches, along with the 6 bits of selected partial jet patch sum, its 2-bit ID and the 2 HT bits. The output data format is shown in Table 5.

Table 5: Output of Layer 1 EEMC DSM Boards

Data	Bit Range	Bit Count	Total
JPA threshold bits	0:1	2	16
JPB threshold bits	2:3	2	
JPC threshold bits	4:5	2	
Selected partial jet patch sum	6:11	6	
Partial jet patch ID	12:13	2	
HT bits	14:15	2	

Upper Half (EE102)

- RBT File: eemc_ee102_2009_a.rbt
- User: EE102
- Input: Same as Lower Half (EE101)
- LUT: Same as Lower Half (EE101)
- Registers: Same as Lower Half (EE101)
- Step 1: Receive two 6-bit TP sums (low and high eta) and 2 HT bits on each of six cables. Three of these cables (channels 1, 2 and 5) come from single-output layer 0 DSM boards. The other three cables (channels 0, 3 and 4) come from double-output layer 0 DSM boards, and on those cables the second 6-bit TP sum will always be zero. Note that this mapping is exactly the opposite of the mapping into the first layer 1 DSM board (EE101).
- Step 2: Calculate 3 jet patches sums as follows:
    - JPA (10 o'clock) = $Ch1_{LO} + Ch1_{HI} + Ch0_{LO}$
    - JPB (12 o'clock) = $Ch2_{LO} + Ch2_{HI} + Ch3_{LO}$
    - JPC (2 o'clock) = $Ch5_{LO} + Ch5_{HI} + Ch4_{LO}$

  In parallel, compare pairs of the low eta sums arriving from the single-output layer 0 DSM boards (i.e. $Ch1_{LO}$, $Ch2_{LO}$ and $Ch5_{LO}$). Also combine (OR) the HT bits from input channels 0:2 and 3:5 separately.
- Step 3: Combine (OR) the two intermediate groups of HT bits together. Compare each of JPA, JPB and JPC to three thresholds and then pack the results for each jet patch into a 2-bit integer (this is the same logic as has been used for many years now). Combine the results of the 2-channel comparisons (calculated at Step 2) to select the largest low eta sum.
    - A (10 o'clock) = ($Ch1_{LO} > Ch2_{LO}$) and not ($Ch5_{LO} > Ch1_{LO}$)
    - B (12 o'clock) = ($Ch2_{LO} > Ch5_{LO}$) and not ($Ch1_{LO} > Ch2_{LO}$)
    - C (2 o'clock) = ($Ch5_{LO} > Ch1_{LO}$) and not ($Ch2_{LO} > Ch5_{LO}$)

  This is the partial jet patch that will be sent on to layer 2. Note that if all three low eta sums are the same (e.g. in an event where nothing happens) then all three comparisons will be false. In this case, sum A, at 10 o'clock, is selected. Use a 2-bit integer to indicate which of the three sums has been selected.
    - 1 = A (10 o'clock)
    - 2 = B (12 o'clock)
    - 3 = C (2 o'clock)

- Step 4: Send, to layer 2, the 2-bit integer for the three completed jet patches, along with the 6 bits of selected partial jet patch sum, its 2-bit ID and the 2 HT bits. The output format is the same as shown in Table 5.

EMC Layer 2 Algorithm Description

The final piece of this DSM tree is the DSM board at layer 2, EM201, where the BEMC and EEMC data will be combined. The input map to this DSM board is shown in Table 6:

Table 6: Input Map for the EMC Layer 2 DSM Board

Channel	Source	Phi
0	BEMC BC101	10 o'clock
1	BEMC BC102	12 o'clock
2	BEMC BC103	2 o'clock
3	BEMC BC104	4 o'clock
4	BEMC BC105	6 o'clock
5	BEMC BC106	8 o'clock
6	EEMC EE101	4, 6 and 8 o'clock
7	EEMC EE102	10, 12 and 2 o'clock

The task of this algorithm is to complete the jet patches that overlap the BEMC-EEMC boundary, combine the jet patch threshold and high tower bits for each detector and implement the adjacent jet patch logic.

The data from the BEMC has the format shown in Table 2 for cable 0, and the data from the EEMC has the format shown in Table 5. It can be seen from Table 5 that each EEMC layer 1 DSM deals with 3 jet patches, but there are only enough bits available to pass one partial jet patch sum. The largest partial sum is chosen to be sent. This means the layer 2 DSM board will only be able to complete two of the six jet patches that overlap the BEMC-EEMC boundary. This is not enough to make a useful contribution to the adjacent jet patch logic so they will not be included in that logic.

The layer 2 DSM for the EMC tree will therefore perform the following steps:

- RBT File: l1_em201_2015_a.rbt
- User: EM201
- Input: 6 channels from BEMC, each with the format given in Table 2, and 2 channels from the EEMC, each with the format given in Table 5.
- LUT: 1-to-1 mapping
- Registers: Five registers. The first three registers each contain one 7-bit threshold value for the jet patch comparison of the boundary-spanning patches. As in the past, these are SIZE-ORDERED, so th0 < th1 < th2.
    - R0: BEMC-EEMC-overlap-JP-th0 (7 bits)
    - R1: BEMC-EEMC-overlap-JP-th1 (7)
    - R2: BEMC-EEMC-overlap-JP-th2 (7)

- R3: AJP-th-Sel (2)
- R4: BEMC-HTTP-Sel (2)
  - 0 = back-to-back HTTP bits
  - 1 = non-adjacent HTTP bits

- Step 1: Receive all the information from the six BEMC layer 1 DSMS, and the two EEMC layer 1 DSMS.
- Step 2: Complete all 6 possible boundary-spanning jet patches in parallel by adding the partial jet patch sums received from the EEMC to each of the partial jet patch sums received from the BEMC. Table 7 shows which BEMC JPpartial sums are combined with the JPpartial sum received from each of EE101 and EE102. Note that only two of these six sums are valid at any one time. The selection of the valid sums will be done at Step 3.

Table 7: Boundary-Spanning Jet Patch Completion

DSM	Patch Location	ID	BEMC JPpartial Sum
EE101	4 o'clock	1	Ch3 – BC104
	6 o'clock	2	Ch4 – BC105
	8 o'clock	3	Ch5 – BC106
EE102	10 o'clock	1	Ch0 – BC101
	12 o'clock	2	Ch1 – BC102
	2 o'clock	3	Ch2 – BC103

Delay the partial-jet-patch ID from EE101 and EE102 to Step 3.
Combine (OR) the HT bits from the six BEMC layer 1 DSMS.
Combine (OR) the HT bits from the two EEMC DSMS.
Check for back-to-back and non-adjacent combinations of the HT.TP bits

HTTP-B2B = (4 o'clock and 10 o'clock) or
(6 o'clock and 12 o'clock) or
(8 o'clock and 2 o'clock)
HTTP-NonAdj = (10 o'clock and (2, 4 or 6 o'clock)) or
(12 o'clock and (4, 6 or 8 o'clock)) or
(2 o'clock and (6 or 8 o'clock)) or
(4 o'clock and 8 o'clock)

Unpack the JP bits from the BEMC and EEMC. In each case, JP0 is the lowest threshold bit, JP1 refers to the middle threshold and JP2 is the highest threshold.

- Step 3: Delay the combined HT bits to the 4^{th} step.
Use R4 to select either the HTTP-B2B or the HTTP-NonAdj bits.
Combine (OR) the JP bits for the BEMC and EEMC separately.
Compare all six completed boundary jet patches to three thresholds. Then use the partial-jet-patch ID from each of the two EEMC layer 1 DSMS ("ID" column in Table 7) to identify which two of these six sets of threshold bits are valid this time. Combine (OR) those results with the BEMC-only and EEMC-only bits to make a set of JP threshold bits that are unified across the whole calorimeter.

Search for jet patches that are adjacent in phi. The search will be done independently, and therefore in parallel, in each of the four eta regions covered by the BEMC-only and EEMC-only jet patches, i.e. $-1<\eta<0$, $-0.6<\eta<0.4$, $0<\eta<1$ and $1<\eta<2$. Note that the boundary-spanning patches are ignored by the adjacent jet patch logic. The logic will look for specific combinations of the JP0, JP1 and JP2 threshold bits separately. Within any eta region and for any JP threshold the adjacent jet patch bit (AJP) will be calculated from:

AJP = (2 o'clock and 4 o'clock) or
(4 o'clock and 6 o'clock) or
(6 o'clock and 8 o'clock) or
(8 o'clock and 10 o'clock) or
(10 o'clock and 12 o'clock) or
(12 o'clock and 2 o'clock)

Register 3 will then select the results from just one of the threshold bits. Finally, combine (OR) the selected AJP bit for the 3 eta regions contained within the BEMC, and separately combine all the AJP bits to make one bit unified over BEMC and EEMC.
Finally, search for back-to-back combinations of EEMC-only jet patches using just the JP0 threshold bits.

EB2B = (2 o'clock and 8 o'clock) or
(4 o'clock and 10 o'clock) or
(6 o'clock and 12 o'clock)

- Step 4: Send to the next layer the HT and HT.TP bits, some of the JP bits and the jet patch topology bits. The output data format is shown in Table 8 (next page). In parallel, send a copy of this set of bits to the scalar system.

Table 8: Output of Layer 2 EMC DSM Board

Bit	Name	Description
Bit 0	BemcHiTwr-th0	Barrel HT bit
Bit 1	BemcHiTwr-th1	Barrel HT bit
Bit 2	BemcHiTwr-th2	Barrel HT bit
Bit 3	Bemc-HTTP	Barrel HTTP bit
Bit 4	EemcHiTwr-th0	Endcap HT bit
Bit 5	EemcHiTwr-th1	Endcap HT bit
Bit 6	JP1	JP1, unified over the BEMC+EEMC
Bit 7	JP2	JP2, unified over the BEMC+EEMC
Bit 8	BJP1	BJP1 for the 18 BEMC-only patches
Bit 9	BJP2	BJP2 for the 18 BEMC-only patches
Bit 10	EJP1	EJP1 for the 6 EEMC-only patches
Bit 11	EJP2	EJP2 for the 6 EEMC-only patches
Bit 12	AJP	AJP for BEMC and EEMC but NOT the boundary
Bit 13	BAJP	BAJP for the BEMC-only patches
Bit 14	EB2B	EEMC-only JP0 topology bit
Bit 15	JP0	JP0, unified over the BEMC+EEMC