# DropBox 3: Computer Architecture

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## Contents



## 1 Assignment

1. Ref. problem 8.16

   (a) A DMA cycle could take as long as 750 n$s$ without the need for wait states. This corresponds to a clock period of 750 n$s$/3 = 250 n$s$, which in turn corresponds to a clock rate of about 4 MHz. This approach would reduce power consumption.

2. Ref. problems 8.17a and 8.17b

   (a) Telecommunications links can operate continuously by their nature, so burst mode can't be used. Cycle-stealing is then necessary.

   (b) All the links of DMA channels have the same data rate, so they must be given equal priority, or you won't be maximizing the throughput potential.