包含block的EDID

Byte sequence

00: Extension tag (which kind of extension block this is); 02h for CEA EDID

01: Revision number (Version number); 03h for Version 3

02: Byte number "d" within this block where the 18-byte DTDs begin. If no non-DTD data is present

in this extension block, the value should be set to 04h (the byte after next). If set to 00h,

there are no DTDs present in this block and no non-DTD data.

03: Number of DTDs present, other Version 2+ information

bit 7: 1 if display supports underscan, 0 if not

bit 6: 1 if display supports basic audio, 0 if not

bit 5: 1 if display supports YCbCr 4:4:4, 0 if not

bit 4: 1 if display supports YCbCr 4:2:2, 0 if not

bit 3..0: total number of native formats in the DTDs included in this block

04: Start of Data Block Collection. If byte 02 is set to 04h, this is where the DTD collection

begins. If byte 02 is set to another value, byte 04 is where the Data Block Collection begins,

and the DTD collection follows immediately thereafter.

The Data Block Collection contains one or more data blocks detailing video, audio, and speaker

placement information about the display. The blocks can be placed in any order, and the initial

byte of each block defines both its type and its length:

bit 7..5: Block Type Tag (1 is audio, 2 is video, 3 is vendor specific, 4 is speaker，allocation, all other values Reserved)

bit 4..0: Total number of bytes in this block following this byte

Once one data block has ended, the next byte is assumed to be the beginning of the next data

block. This is the case until the byte (designated in Byte 02, above) where the DTDs are known

to begin.

Any Audio Data Block contains one or more 3-byte Short Audio Descriptors (SADs). Each SAD

details audio format, channel number, and bitrate/resolution capabilities of the display as

follows:

SAD Byte 1 (format and number of channels):

bit 7: Reserved (0)

bit 6..3: Audio format code

1 = Linear Pulse Code Modulation (LPCM)

2 = AC-3

3 = MPEG1 (Layers 1 and 2)

4 = MP3

5 = MPEG2

6 = AAC

7 = DTS

8 = ATRAC

0, 15: Reserved

9 = One-bit audio aka SACD

10 = DD+

11 = DTS-HD

12 = MLP/Dolby TrueHD

13 = DST Audio

14 = Microsoft WMA Pro

bit 2..0: number of channels minus 1 (i.e. 000 = 1 channel; 001 = 2 channels; 111 =

8 channels)

SAD Byte 2 (sampling frequencies supported):

bit 7: Reserved (0)

bit 6: 192kHz

bit 5: 176kHz

bit 4: 96kHz

bit 3: 88kHz

bit 2: 48kHz

bit 1: 44kHz

bit 0: 32kHz

SAD Byte 3 (bitrate):

For LPCM, bits 7:3 are reserved and the remaining bits define bit depth

bit 2: 24 bit

bit 1: 20 bit

bit 0: 16 bit

For all other sound formats, bits 7..0 designate the maximium supported bitrate divided by

8kHz.

Any Video Data Block will contain one or more 1-byte Short Video Descriptors (SVDs). They are decoded as follows:

bit 7: 1 to designate that this should be considered a "native" resolution, 0 for non-native

bit 6..0: index value to a table of standard resolutions/timings from CEA/EIA-861E:

Code

Short Aspect

Name Ratio HxV @ F

1 DMT0659 4:3 640x480p @ 59.94/60Hz

2 480p 4:3 720x480p @ 59.94/60Hz

3 480pH 16:9 720x480p @ 59.94/60Hz

4 720p 16:9 1280x720p @ 59.94/60Hz

5 1080i 16:9 1920x1080i @ 59.94/60Hz

6 480i 4:3 720(1440)x480i @ 59.94/60Hz

7 480iH 16:9 720(1440)x480i @ 59.94/60Hz

8 240p 4:3 720(1440)x240p @ 59.94/60Hz

9 240pH 16:9 720(1440)x240p @ 59.94/60Hz

10 480i4x 4:3 (2880)x480i @ 59.94/60Hz

11 480i4xH 16:9 (2880)x480i @ 59.94/60Hz

12 240p4x 4:3 (2880)x240p @ 59.94/60Hz

13 240p4xH 16:9 (2880)x240p @ 59.94/60Hz

14 480p2x 4:3 1440x480p @ 59.94/60Hz

15 480p2xH 16:9 1440x480p @ 59.94/60Hz

16 1080p 16:9 1920x1080p @ 59.94/60Hz

17 576p 4:3 720x576p @ 50Hz

18 576pH 16:9 720x576p @ 50Hz

19 720p50 16:9 1280x720p @ 50Hz

20 1080i25 16:9 1920x1080i @ 50Hz\*

21 576i 4:3 720(1440)x576i @ 50Hz

22 576iH 16:9 720(1440)x576i @ 50Hz

23 288p 4:3 720(1440)x288p @ 50Hz

24 288pH 16:9 720(1440)x288p @ 50Hz

25 576i4x 4:3 (2880)x576i @ 50Hz

26 576i4xH 16:9 (2880)x576i @ 50Hz

27 288p4x 4:3 (2880)x288p @ 50Hz

28 288p4xH 16:9 (2880)x288p @ 50Hz

29 576p2x 4:3 1440x576p @ 50Hz

30 576p2xH 16:9 1440x576p @ 50Hz

31 1080p50 16:9 1920x1080p @ 50Hz

32 1080p24 16:9 1920x1080p @ 23.98/24Hz

33 1080p25 16:9 1920x1080p @ 25Hz

34 1080p30 16:9 1920x1080p @ 29.97/30Hz

35 480p4x 4:3 (2880)x480p @ 59.94/60Hz

36 480p4xH 16:9 (2880)x480p @ 59.94/60Hz

37 576p4x 4:3 (2880)x576p @ 50Hz

38 576p4xH 16:9 (2880)x576p @ 50Hz

39 108Oi25 16:9 1920x1080i(1250 Total) @ 50Hz\*

40 1080i50 16:9 1920x1080i @ 100Hz

41 720p100 16:9 1280x720p @ 100Hz

42 576p100 4:3 720x576p @ 100Hz

43 576p100H 16:9 720x576p @ 100Hz

44 576i50 4:3 720(1440)x576i @ 100Hz

45 576i50H 16:9 720(1440)x576i @ 100Hz

46 1080i60 16:9 1920x1080i @ 119.88/120Hz

47 720p120 16:9 1280x720p @ 119.88/120Hz

48 480p119 4:3 720x480p @ 119.88/120Hz

49 480p119H 16:9 720x480p @ 119.88/120Hz

50 480i59 4:3 720(1440)x480i @ 119.88/120Hz

51 480i59H 16:9 720(1440)x480i @ 119.88/120Hz

52 576p200 4:3 720x576p @ 200Hz

53 576p200H 16:9 720x576p @ 200Hz

54 576i100 4:3 720(1440)x576i @ 200Hz

55 576i100H 16:9 720(1440)x576i @ 200Hz

56 480p239 4:3 720x480p @ 239.76/240Hz

57 480p239H 16:9 720x480p @ 239.76/240Hz

58 480i119 4:3 720(1440)x480i @ 239.76/240Hz

59 480i119H 16:9 720(1440)x480i @ 239.76/240Hz

60 720p24 16:9 1280x720p @ 23.98/24Hz

61 720p25 16:9 1280x720p @ 25Hz

62 720p30 16:9 1280x720p @ 29.97/30Hz

63 1080p120 16:9 1920x1080p @ 119.88/120Hz

0, 64 - 127 Reserved

\*Short video descriptors 20 & 39 are both 1920x1080i@50 16:9 but differ in the amount of vertical total lines which are 1125 and 1250, respectively.

Notes: Parentheses indicate instances where pixels are repeated to meet the minimum speed

requirements of the interface. For example, in the 720X240p case, the pixels on each line

are double-clocked. In the (2880)X480i case, the number of pixels on each line, and thus

the number of times that they are repeated, is variable, and is sent to the DTV monitor by

the source device.

Increased Hactive expressions include “2x” and “4x” indicate two and four times the reference

resolution, respectively.

The CEA/EIA-861/A standard included only numbers 1-7 and numbers 17-22 above(but not as short

video descriptors which were introduced in CEA/EIA-861B) and are considered primary video format

timings.

The CEA/EIA-861B standard included the first 34 short video descriptors above.

The CEA/EIA-861D standard included the first 59 short video descriptors above.

HDMI 1.0 to HDMI 1.2a uses the CEA-861-B video standard, HDMI 1.3 to HDMI 1.3c uses the

CEA-861-D video standard, and HDMI 1.4 uses the CEA/EIA-861E video standard.

A Vendor Specific Data Block (if any) contains as its first three bytes the vendor's IEEE

24-bit registration number, LSB first. For HDMI, it is always 00-0C-03 for HDMI Licensing, LLC.

It is followed by a two byte source physical address, LSB first. The source physical address

provides the CEC physical address for upstream CEC devices.

The remainder of the Vendor Specific Data Block is the "data payload",which can be anything the

vendor considers worthy of inclusion in this EDID extension block. HDMI 1.3a specifies some

requirements for the data payload. See that spec for detailed info on these bytes:

VSD Byte 1-3 IEEE Registration Identifier (LSB First)

VSD Byte 4-5 Components of Source Physical Address (See section 8.7 of HDMI 1.3a)

VSD Byte 6 (bits are set if sink supports...):

bit 7: Supports\_AI (...a function that needs info from ACP or ISRC packets)

bit 6: DC\_48bit (...16-bit-per-channel deep color)

bit 5: DC\_36bit (...12-bit-per-channel deep color)

bit 4: DC\_30bit (...10-bit-per-channel deep color)

bit 3: DC\_Y444 (...4:4:4 in deep color modes)

bit 2: Reserved (0)

bit 1: Reserved (0)

bit 0: DVI\_Dual (...DVI Dual Link Operation)

VSD Byte 7 If non-zero (Max\_TMDS\_Frequency / 5mhz)

VSD Byte 8 (latency fields indicators):

bit 7: latency\_fields (set if latency fields are present)

bit 6: i\_latency\_fields (set if interlaced latency fields are present; if set

four latency fields will be present, 0 if bit 7 is 0)

bits 5-0: Reserved (0)

VSD Byte 9 Video Latency (if indicated, value=1+ms/2 with a max of 251 meaning 500ms)

VSD Byte 10 Audio Latency (video delay for progressive sources, same units as above)

VSD Byte 11 Interlaced Video Latency (if indicated, same units as above)

VSD Byte 12 Interlaced Audio Latency (video delay for interlaced sources, same units as above)

Additional bytes may be present, but the HDMI spec says they shall be zero.

If a Speaker Allocation Data Block is present, it will consist of three bytes. The second and

third are Reserved (all 0), but the first contains information about which speakers are present in

the display device:

bit 7: Reserved (0)

bit 6: Rear Left Center / Rear Right Center present for 1, absent for 0

bit 5: Front Left Center / Front Right Center present for 1, absent for 0

bit 4: Rear Center present for 1, absent for 0

bit 3: Rear Left / Rear Right present for 1, absent for 0

bit 2: Front Center present for 1, absent for 0

bit 1: LFE present for 1, absent for 0

bit 0: Front Left / Front Right present for 1, absent for 0

Note that for speakers with right and left polarity, it is assumed that both

left and right are present.

"d": byte (designated in byte 02) where DTDs begin. 18-byte DTD strings continue for an unspecified

length (modulo 18) until a "00 00" is as the first bytes of a prospective DTD. At this point,

the DTDs are known to be complete, and the start address of the "00 00" can be considered to be "XX"

(see below)

"XX"-126: Post-DTD padding. Should be populated with 00h

127: Checksum - This byte should be programmed such that the sum of all 128 bytes equals 00h.