How IP Subsystem Will Speed NVM Express (NVMe) Adoption

Non-Volatile Memory Express (NVM Express or NVMe) is an emerging protocol standard for accessing solid state drives (SSDs) over PCI Express (PCIe) links. It would thus make sense, if you're designing an SoC that has an SSD interface, to cobble together a subsystem that includes an NVMe controller, PCIe controller, and PCIe PHY. But what if you could just buy a configurable subsystem that includes all of these components running under a common firmware layer?

You can, with the introduction this week (May 15, 2012) of the Cadence Design IP for NVM Express subsystem. The high level of integration makes it easy to drop the solution into an SoC, and opens some opportunities for optimization that would otherwise be difficult.

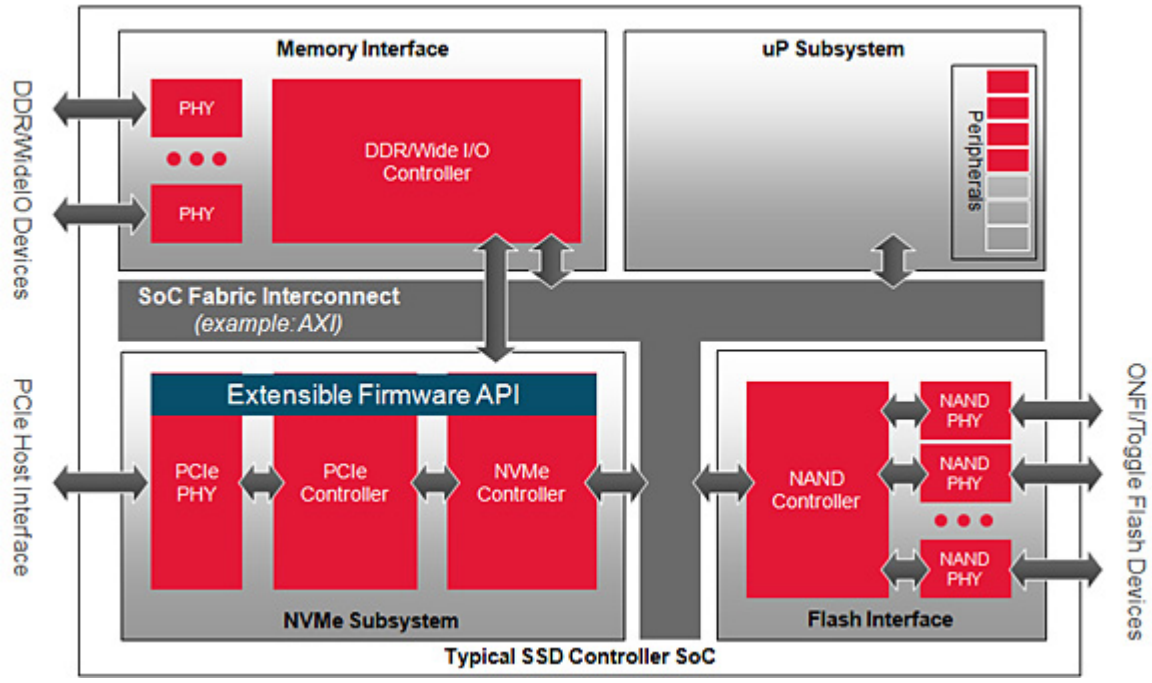
So why NVMe? In many designs, the system bottleneck has moved from computing to data access. Reducing latency and boosting throughput are becoming critical requirements. PCIe-based storage solutions for NAND flash are thus making inroads, but many such solutions have used non-standard protocols. Existing standards such as Fibre Channel and Serial ATA (SATA) were not created with SSDs, virtualization, and high I/O operations/second in mind.

The NVM Express specification was released in March 2011 by the NVMe Work Group, whose web site is a good source of information about the standard. NVM Express 1.0 defines an optimized register interface, command set, and feature set for PCI Express SSDs. In addition to leveraging high-performance PCIe as its transport layer, NVMe is scalable from low-end client devices to high-performance enterprise applications. It supports up to 64K outstanding requests, offers end to end data protection, and robust error reporting.

A Configurable Subsystem

The Cadence announcement provides a complete PCIe and NVMe solution. "What we're delivering is not just an NVMe controller," said John Tam, product marketing director for SoC Realization at Cadence. "It's a complete subsystem that integrates multiple pieces of IP with firmware, and with verification environments, to make it much easier for people to put NVMe into their designs."

The diagram below shows how an NVMe subsystem (at lower left) might fit into an SSD controller SoC. The subsystem includes a PCIe PHY, PCIe controller, NVMe controller, and an extensible firmware API. It also comes with NVMe verification IP, which was announced separately in March 2012. One advantage of the subsystem approach, Tam noted, is that SoC integration is much easier compared to assembling the various components manually and making sure they all work together.



Another perhaps less obvious advantage is the optimization that becomes possible through the subsystem approach. For example, Cadence has been able to optimize the subsystem in the following ways:

- The connection between the NVMe and PCIe controllers improves latency
- A complete firmware/hardware verified solution maximizes the command throughput for interaction between the system software and the storage system
- DMA operations between PCIe and NVMe improve performance and reduce CPU operations
- Command expansion and hardware accelerators work together to provide flexibility and maximum performance

The bottom line? "By looking at this subsystem as a whole, we can reduce the latency, improve the throughput, and reduce the CPU overhead," Tam said.

The Cadence Design IP for NVM Express subsystem is important not only because it will ease the adoption of NVMe. It also represents a direction that IP providers will need to take in order to address the levels of SoC complexity that will very quickly be upon us.

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