Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of the participant: Kartikaya Dwivedi

Title of the circuit: ALU_module

Theory/Description: ALU is a fundamental BLock of CPU.IT is here implemented using VHDL which do arithmetic Addition, Bitwise OR, Bitwise AND, A+B'+1 operation and neglects the carry part of the result.

It takes 2 bit long 2 input A and B and 2-bit Selection input allowing 4 different operations.

It gives

A+B when Sel=00

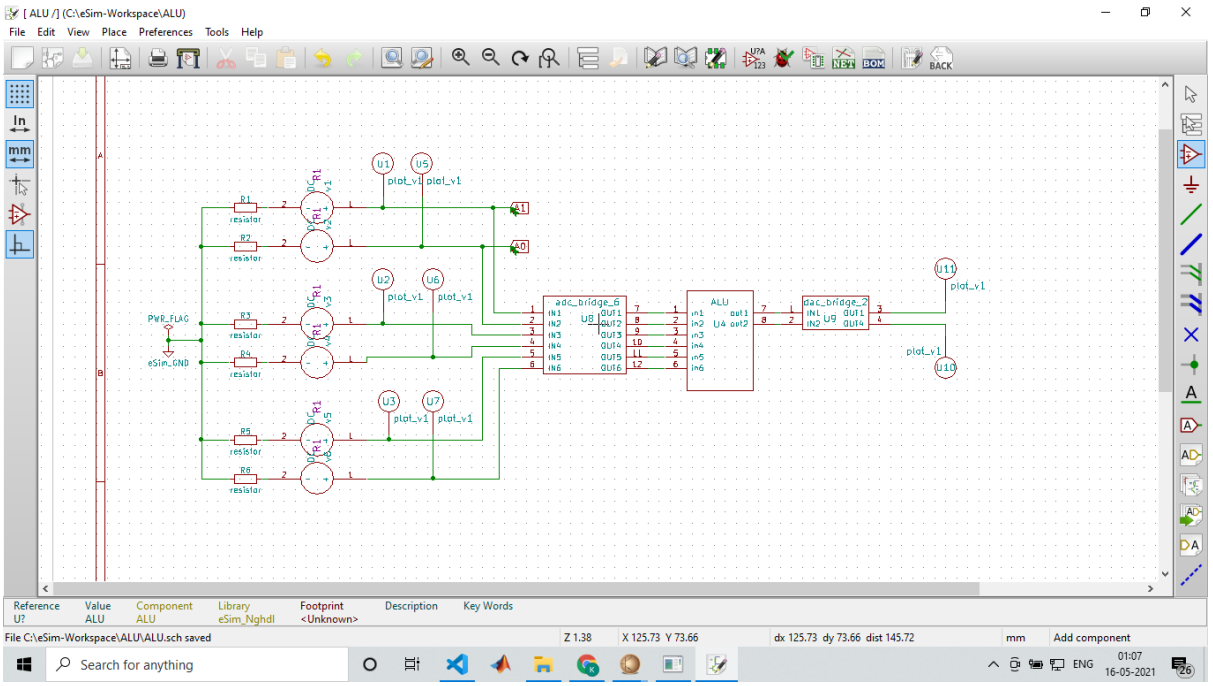
A+B'+1 when Sel=01

A and B when Sel=10

A or B when Sel =11

The primary block is implemented using VHDL.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :

Source/Reference(s) :

1:Spoken Tutorials

2:https://en.wikipedia.org/wiki/Arithmetic_logic_unit