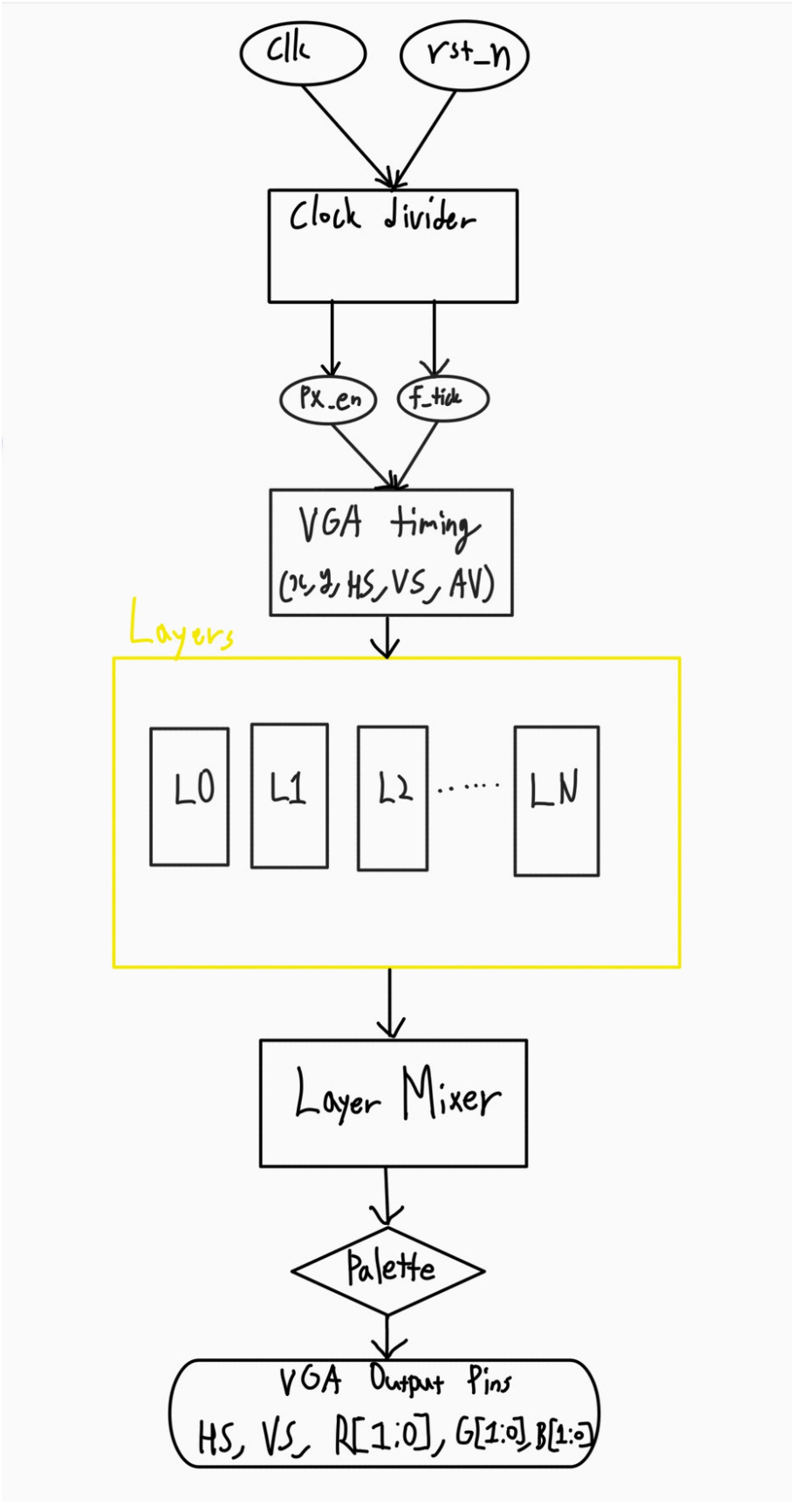
Block Diagram



Input Pins

clk	48 MHz system clock from the Tiny Tapeout board. All logic runs synchronous to this.
rst_n	Global reset (active low). Resets all counters and state machines.

Output Pins

HS	Horizontal Sync (active low). Marks the end of each scan line.
VS	Vertical Sync (active low). Marks the end of each frame.
R[1:0]	Red [1:0]. 2-bit red channel output (0 = black, 3 = full red).
G[1:0]	Green [1:0]. 2-bit green channel output (0 = black, 3 = full green).
B[1:0]	Blue [1:0]. 2-bit blue channel output (0 = black, 3 = full blue).

Project Timeline

- ☐ **Oct 1 (Week 5)** – VGA timing working
  - ☐ Implement HS/VS, x,y counters, video_active
  - ☐ Verify waveforms in Cocotb
- ☐ **Oct 8 (Week 6)** – First effect running
  - ☐ Add simple background (gradient/plasma)
  - ☐ Confirm visible color changes in sim
- ☐ **Oct 13–17 (Week 7)** – Reading Week

- [ ] Catch-up / refine existing code
- [ ] (Optional) start RNG module for future effects

- [ ] **Oct 22 (Week 8)** – Task 2: Sub-block evaluation
  - [ ] Add at least one more effect (starfield/scroller)
  - [ ] Show each block works independently

- [ ] **Oct 29 (Week 9)** – Integration (part 1)
  - [ ] Create layer mixer (combine multiple effects)
  - [ ] Synthesize first full design in OpenLane

- [ ] **Nov 5 (Week 10)** – Integration (part 2)
  - [ ] Add palette (RGB222 mapper)
  - [ ] Connect everything at top level
  - [ ] Run full-frame simulation

- [ ] **Nov 12 (Week 11)** – Task 3: System integration
  - [ ] Verify entire design at gate-level (post-synth)
  - [ ] Ensure HS/VS + RGB outputs look correct

- [ ] **Nov 19 (Week 12)** – Final verification
  - [ ] Check timing/area fits in 1 tile
  - [ ] Confirm I/O mapping matches spec

- [ ] **Nov 26 (Week 13)** – Documentation complete
  - [ ] Block diagram + I/O table polished
  - [ ] Final README + design description in /docs

- [ ] **Dec 3 (Week 14)** – Final submission & evaluation
    - [ ] Submit repo with verified RTL + docs
    - [ ] Be ready to explain/demo design