

3.3V BANK

- PCI
- LIMB
- Configuration

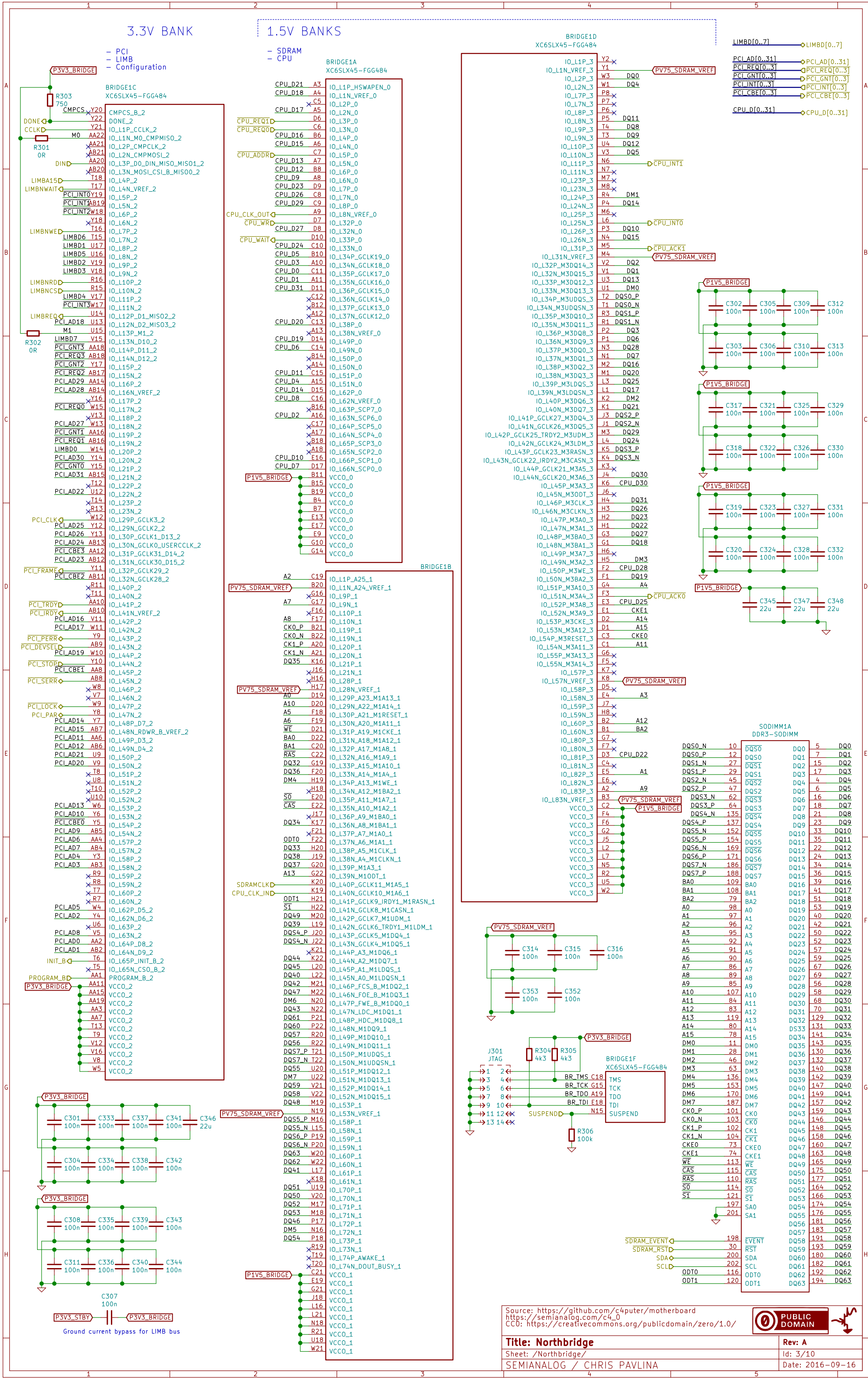
1.5V BANKS

- SDRAM
- CPU

BRIDGE1D  
XC6SLX45-FGG484

LIMBD[0..7] → LIMBD[0..7]

PCI\_AD[0..31] → PCI\_AD[0..31]  
PCI\_REQ[0..3] → PCI\_REQ[0..3]  
PCI\_GNT[0..3] → PCI\_GNT[0..3]  
PCI\_INT[0..3] → PCI\_INT[0..3]  
PCI\_CBE[0..3] → PCI\_CBE[0..3]  
CPU\_D[0..31] → CPU\_D[0..31]



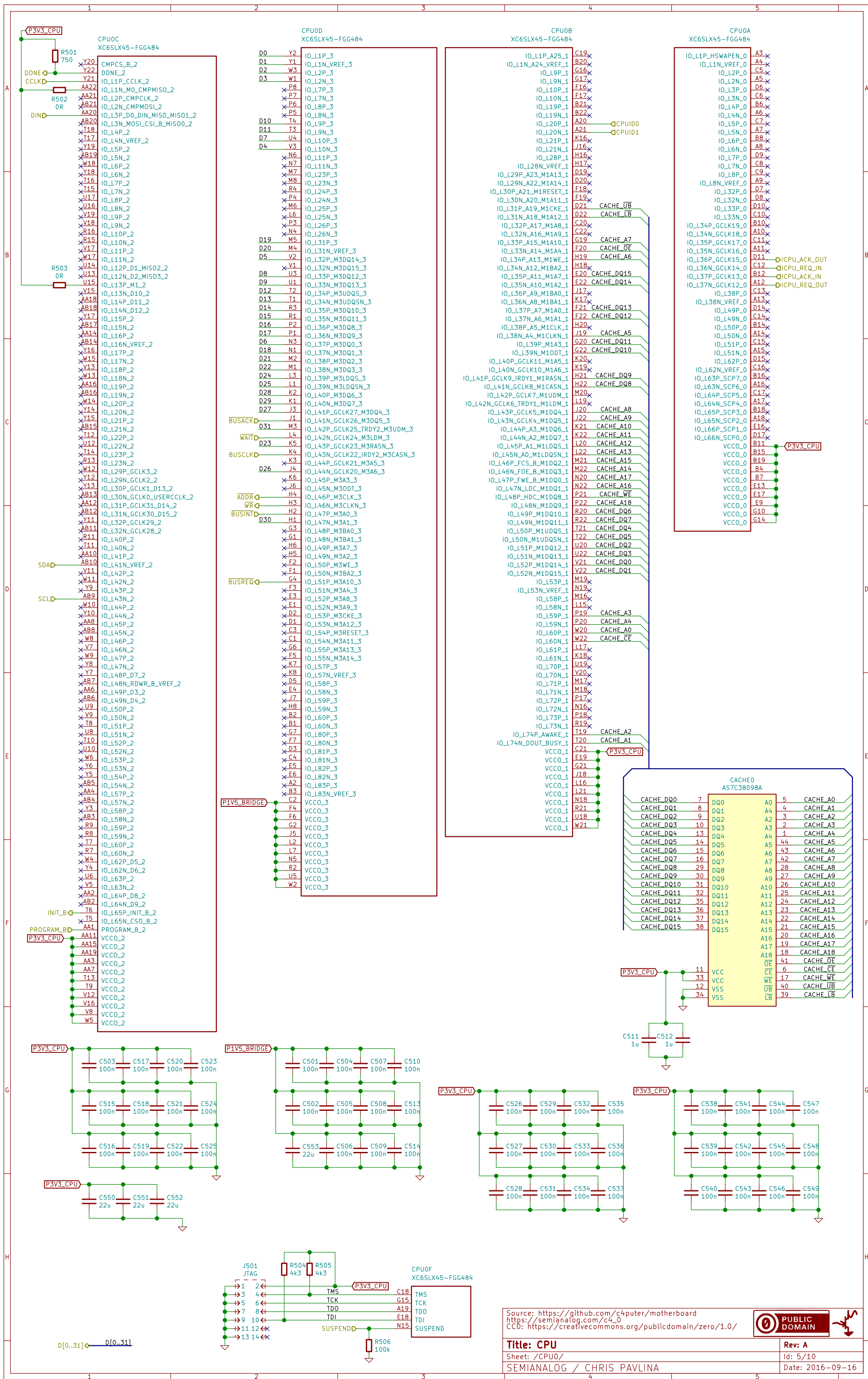
Source: <https://github.com/c4puter/motherboard>  
[https://semianalog.com/c4\\_0](https://semianalog.com/c4_0)  
CC0: <https://creativecommons.org/publicdomain/zero/1.0/>

**PUBLIC DOMAIN**

Title: Northbridge		Rev: A	
Sheet: /Northbridge/		Id: 3/10	
SEMIALOG / CHRIS PAVLINA		Date: 2016-09-16	







Source: <https://github.com/c4puter/motherboard>  
[https://semianalog.com/c4\\_0](https://semianalog.com/c4_0)  
 CC0: <https://creativecommons.org/publicdomain/zero/1.0/>



**Title:** CPU

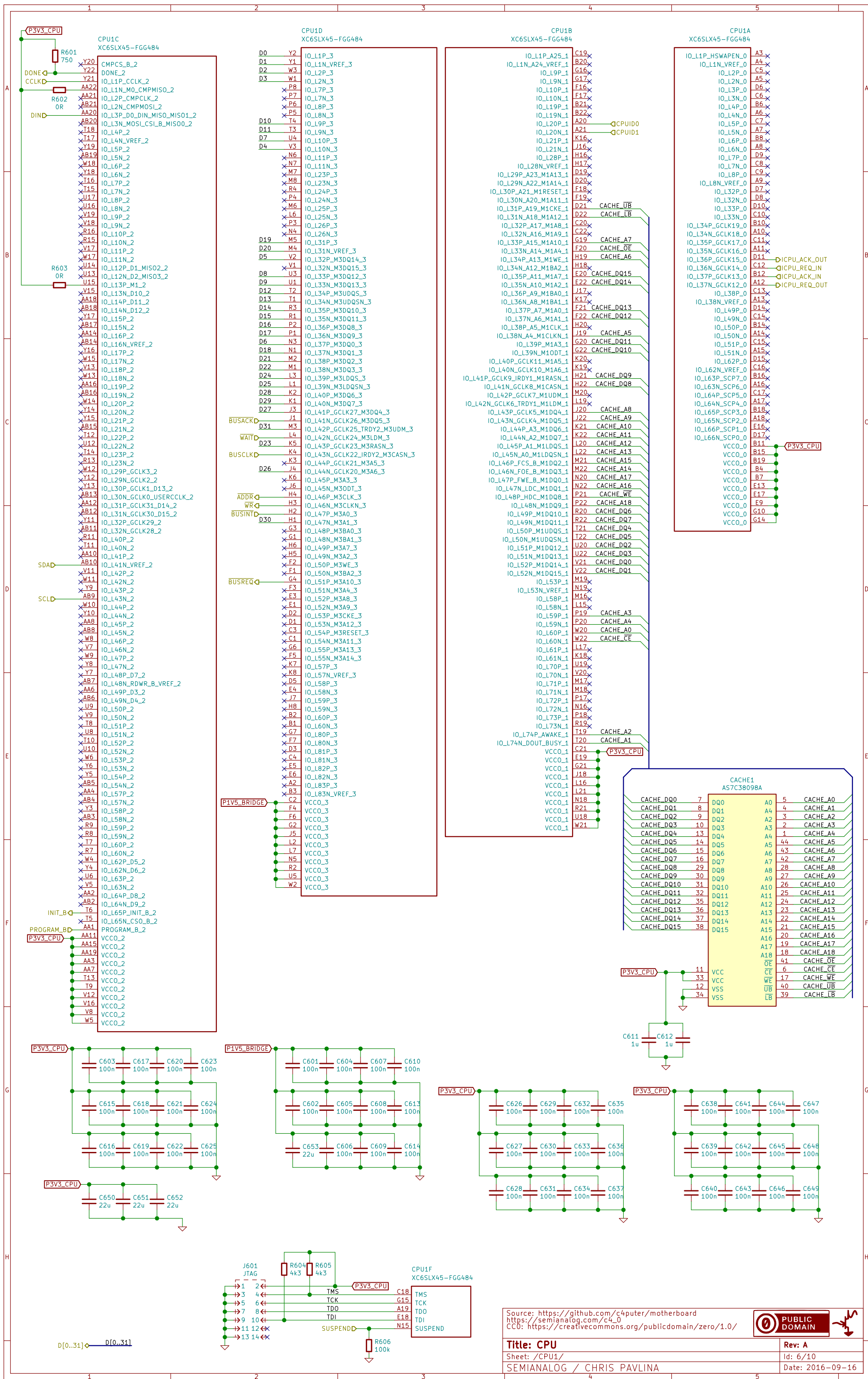
Sheet: /CPU0/

SEMIANALOG / CHRIS PAVLINA

Rev: A

Id: 5/10

Date: 2016-09-16



Source: <https://github.com/c4puter/motherboard>  
[https://semianalog.com/c4\\_0](https://semianalog.com/c4_0)  
 CC0: <https://creativecommons.org/publicdomain/zero/1.0/>



**Title:** CPU

Sheet: /CPU1/

SEMIANALOG / CHRIS PAVLINA

Rev: A

Id: 6/10

Date: 2016-09-16

