AAE DSPA LAB 2 instruction: ADC

November 2021

1 Introduction

1.1 Analog to digital conversion

The process of transforming the signal from the analog domain to the digital domain. It can be divided into sampling and quantization, what means conversion of a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal.

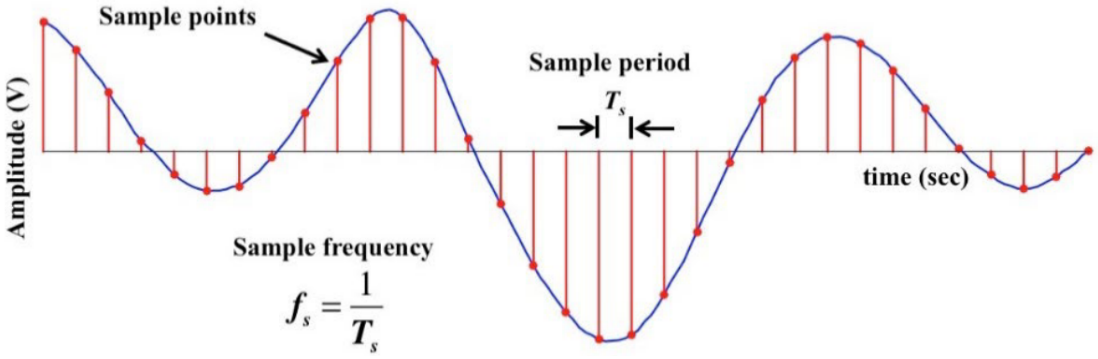

Figure 1: Analog to digital conversion.

1.2 ADC bandwidth

The bandwidth of an ADC is characterized mainly by its sampling rate, analog front-end and optional antialiasing filter. According to Nyquist–Shannon sampling theorem [1], the sampling frequency should be at least 2 times more than maximum signal frequency.

1.3 Resolution

An ideal ADC has an ENOB (Effective Number Of Bits) equal to its resolution. In real cases noise, ADC accuracy and linearity must be considered. It is characterized by SNR (Signal to Noise Ratio) and SINAD (signal-to-noise and distortion ratio) [2]. SNR, or sometimes called SNR-without-harmonics is calculated from the FFT data the same as SINAD, except that the signal harmonics are excluded from the calculation, leaving only the noise terms. In practice, it is only necessary to exclude the first 5 harmonics, since they dominate. SINAD represents overal quality of the signal. ENOB can be calculaded usign below equation:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

1.4 Oversampling

When summing up N ADC samples, uncorrelated noise increases its amplitude by $\sqrt{N}$, while summing up a coherent signal increases its average by N. As a result, the Signal-to-Noise Ratio SNR increases by $\sqrt{N}$. The number of samples required to get n bits of additional data precision is $N = 2^{2n}$ [3].

2 Tasks

2.1 ADC configuration 1

- Set ADC clock to 21 MHz. The main uC clock (SYSCLK, HCLK) should be fixed to 168 MHz. Refer to pages 133-135 of STM32F407xx datasheet [4].
- Set external trigger for ADC. Use TIM3 Trigger Out Event.
- Configure TIM3 to generate event at 50 kHz. Refer to pages 85, 105, 361-366, 392, 406 of reference manual [5].
- Put ADC callback to main.c. Write necessary code to pick ADC samples and put it to the RAM buffer.
- Use generator to drive ADC input. Generate 1 kHz, 10 kHz and 40 kHz, 1 V amplitude, 1.5 V offset sine signal. Save buffer values using STM32CubeIDE debug mode. Make plots of collected samples (you can use Gnuplot, Octave, Matlab, etc.).
- Explain the behavior of the signals in the obtained plots.

2.2 ADC configuration 2

- Set ADC clock to 21 MHz and the main clock to 168 MHz.
- Set DMA request, use circular buffer.
- Set external trigger for ADC. Use TIM3 Trigger Out Event.
- Configure TIM3 to generate event at 800 kHz.
- Put ADC DMA complete transfer callback to main.c. Write necessary code to perform 16x oversampling. The final sampling rate should be 50 kHz after oversampling.
- Use generator to drive ADC input. Generate 1 kHz, 10 kHz and 40 kHz, 1 V amplitude, 1.5 V offset sine signal. Save buffer values using STM32CubeIDE debug mode. Save buffer values using STM32CubeIDE debug mode. Make plots of collected samples.
- Explain the behavior of the signals in the obtained plots.

2.3 Extra task - ENOB

- Calculate FFT from samples obtained in both previous configurations at 1 kHz.
- Calculate SINAD, then ENOB of ADC configuration 1 and ADC configurtion 2.

3 Questions

1. What is the Nyquist frequency and aliasing?
2. What theoretical ADC resolution can be achieved with 16x oversampling?
3. What is the advantages of using DMA?

References

[1] *Nyquist-Shannon sampling theorem*. Science Direct.

[2] W. Kester, "Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so You Don't Get Lost in the Noise Floor," p. 8.

[3] "AVR121: Enhancing ADC resolution by oversampling," p. 14.

[4] STMicroelectronics, *STM32F405xx STM32F407xx Datasheet*. DS8626 Rev 9, 2020.

[5] STMicroelectronics, *RM0090 Reference Manual*. RM0090 Rev 18, 2019.