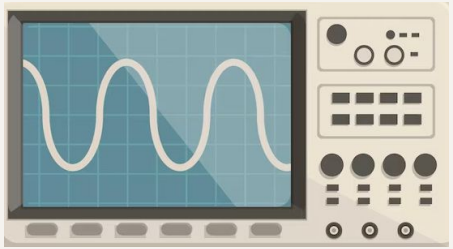
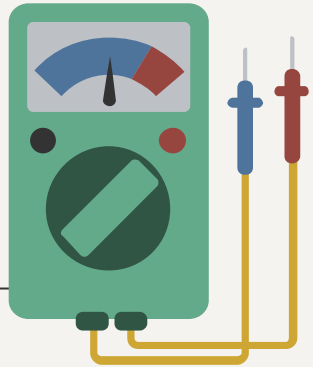


Digital Oscilloscope

Farid Musayev, Chenglong (Eric) Wang ECE241



Overview

01 Introduction

02 Functions and Demo

03 Development Process

04 Future Improvements and Work Distribution

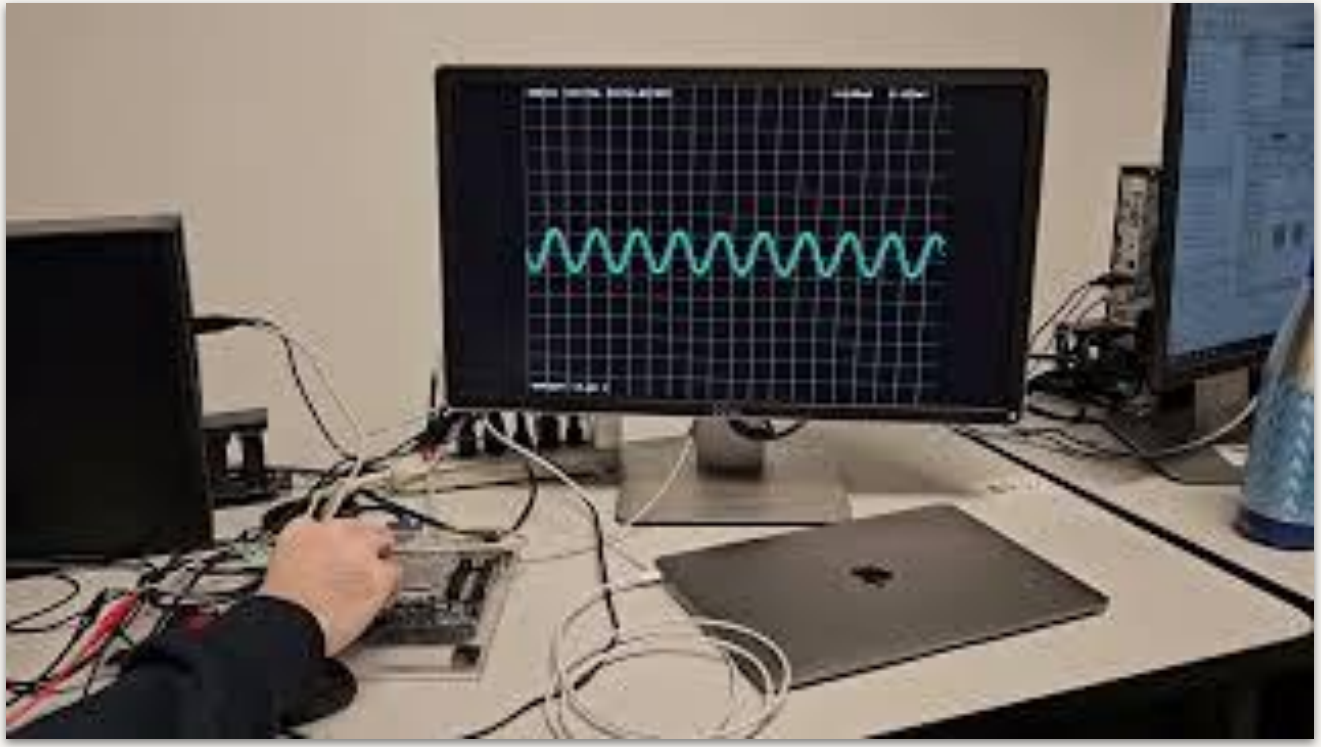
Introduction

This project implements a digital oscilloscope on the DE1-SoC FPGA that samples an analog signal from a waveform generator and displays it on a VGA monitor in real time. The goal is to recreate the core behavior of an oscilloscope entirely in digital logic, with smooth waveform rendering and intuitive user controls for horizontal and vertical scaling.

Core Functions:

- **Signal acquisition:** AD7928 ADC samples the input and streams digital data into an on-chip ring buffer.
- **Processing and control:** FPGA logic applies horizontal time-base scaling, vertical scaling, and a freeze mode to hold a captured waveform.
- **User interface:** DE1-SoC buttons and switches control zoom, scaling, and freeze/run.
- **VGA display:** Lastly the FPGA produces an output that goes through the VGA DAC, that renders the waveform as a continuous trace on the 640x480 VGA display.

Demo Video



User Controls Summary

Component	Control	Function
Reset	SW[0]	HIGH = Run, LOW = Reset
View	SW[1]	Show Grid
	SW[2]	Show Waveform
	SW[9]	Freeze Display
Color	SW[6:4]	R, G, B channels ON/OFF
Source	SW[8]	LOW = ADC, HIGH = Test Pattern
X-Axis	KEY[0]	Timebase Zoom IN (Faster)
	KEY[1]	Timebase Zoom OUT (Slower)
Y-Axis	SW[3]	Mode Select (LOW = Gain, HIGH = Offset)
(SW[3]=0)	KEY[2]	Voltage Gain Increase (Zoom In)
(SW[3]=0)	KEY[3]	Voltage Gain Decrease (Zoom Out)
(SW[3]=1)	KEY[2]	Move Trace DOWN
(SW[3]=1)	KEY[3]	Move Trace UP

Block Diagram (High Level)

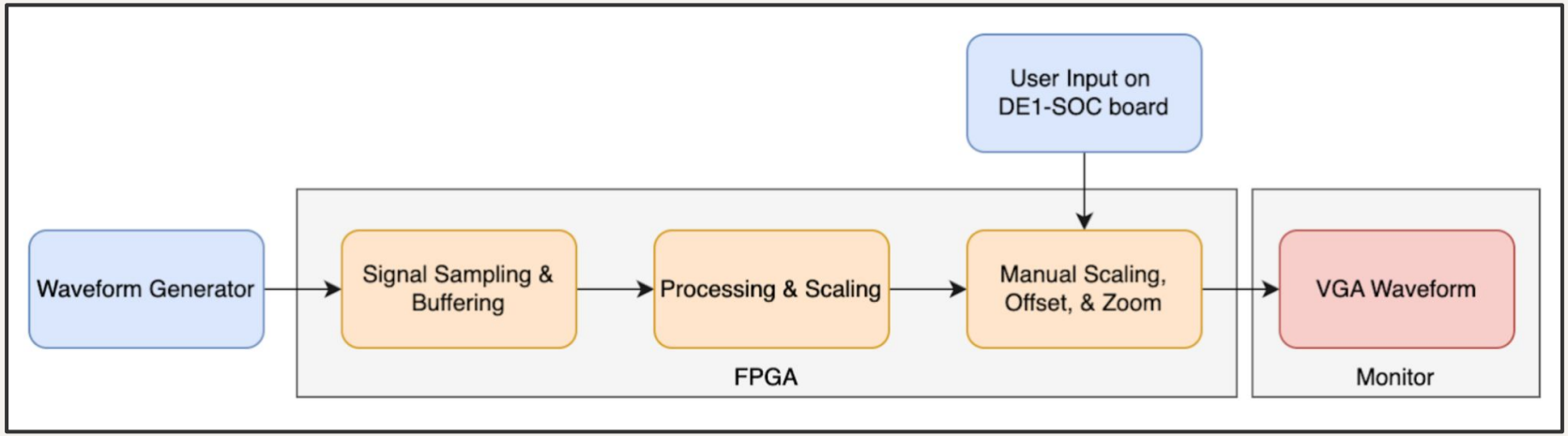


Figure 1: High Level Block Diagram.

Block Diagram (Detailed)

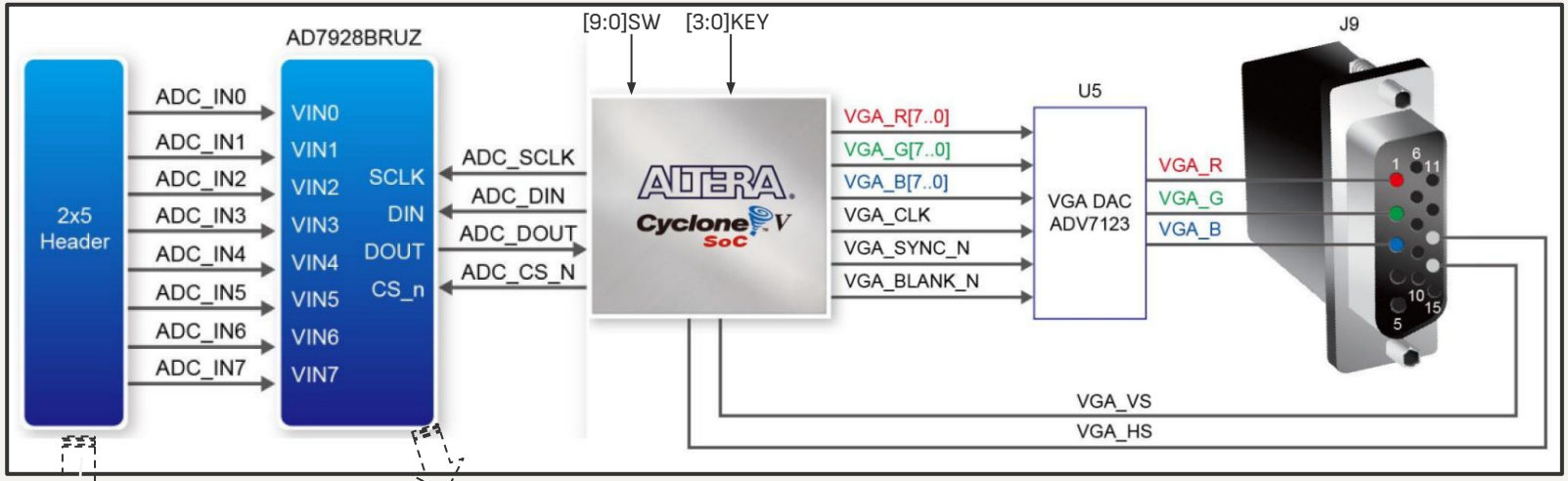


Figure 2: Detailed High Level Block Diagram.

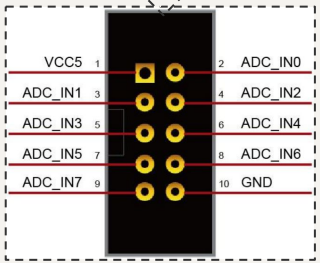


Figure 3: 2x5 header pins schematic

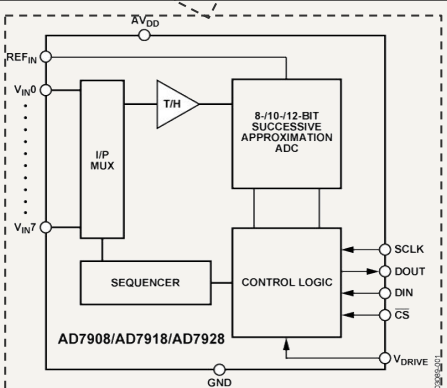
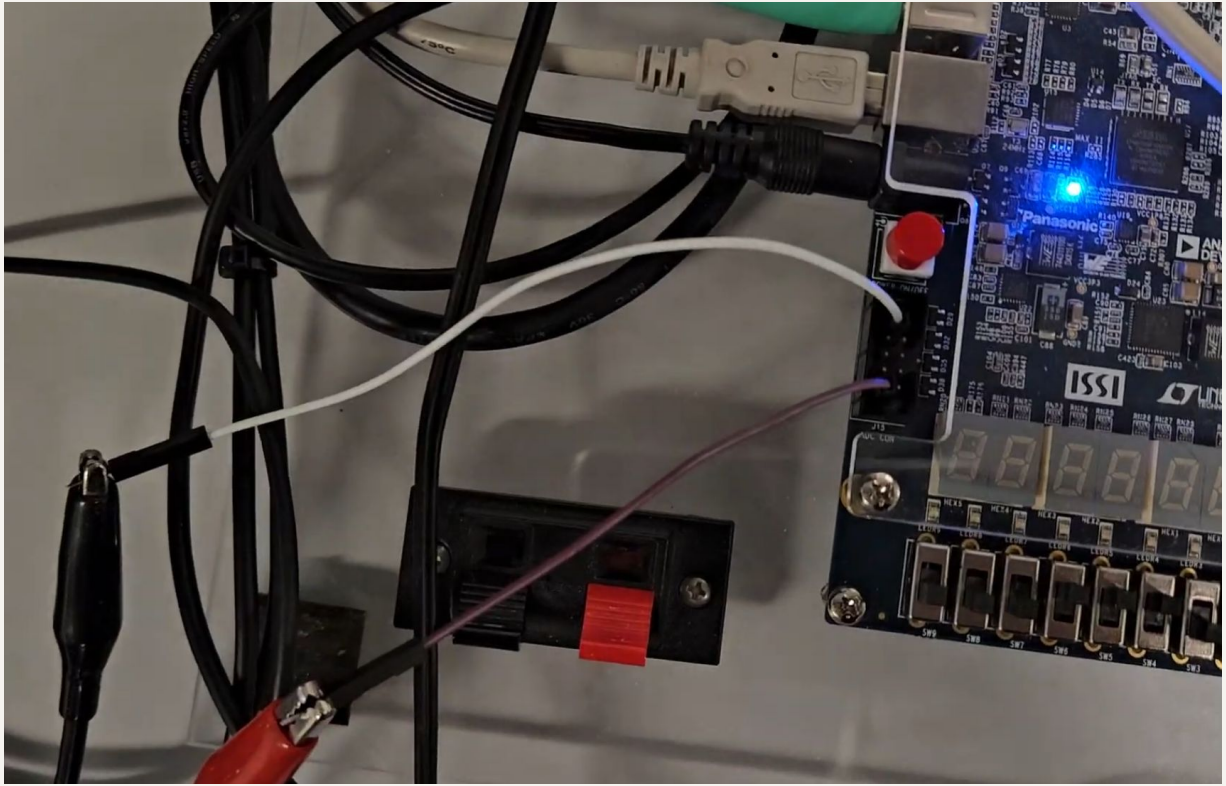


Figure 4:AD7928 Internal Components

Images: Terasic DE1-SoC User Manual. www.terasic.com

Receiving External Analog Signal



Signal Sampling and Buffering

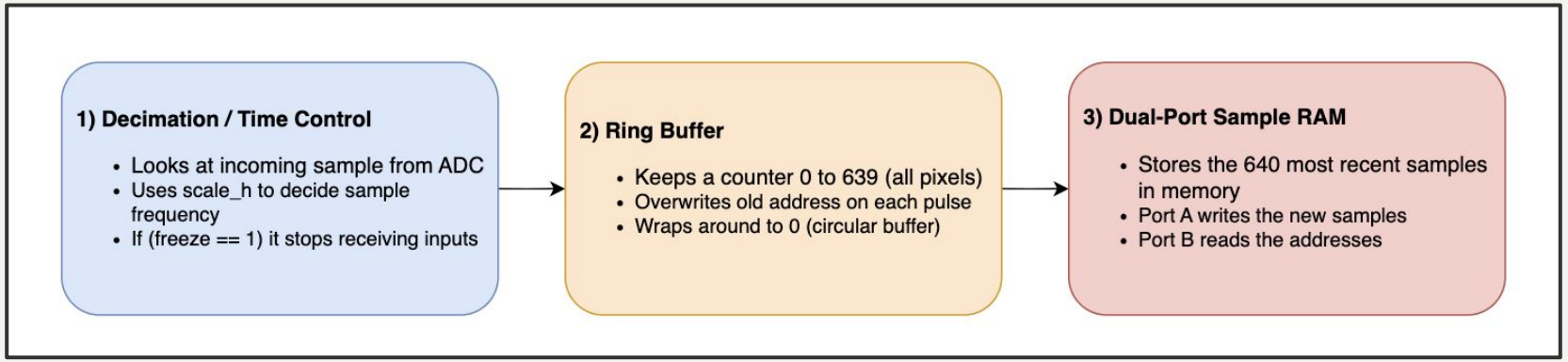
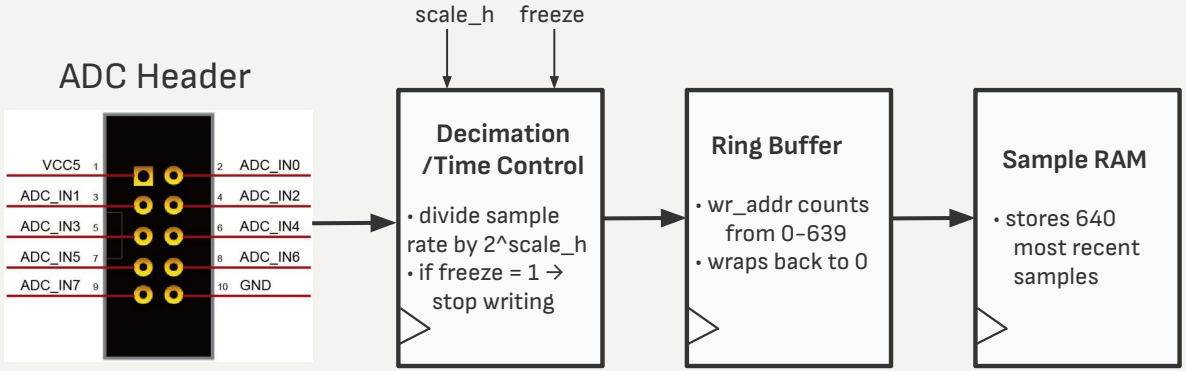


Figure 5: Signal Sampling And buffering sub-component block diagram



User Controls - Scaling, offsets

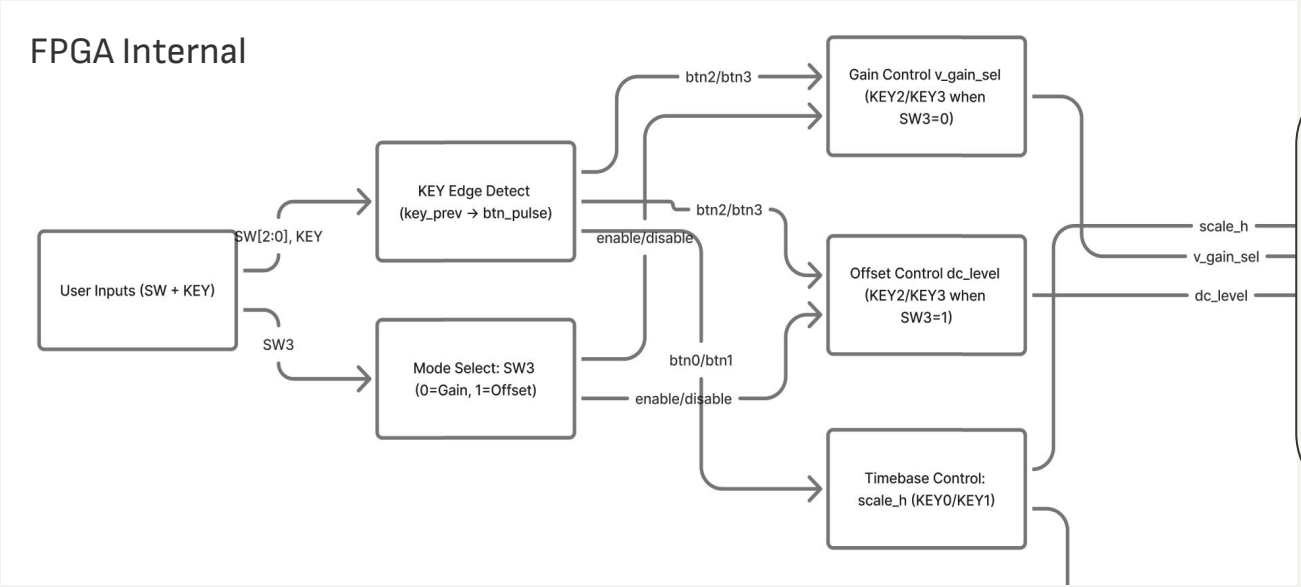


Figure 6: User Control sub-component block diagram (simplified).

Waveform render:
Greater v_gain_sel->greater gain ->greater amplitude.

Greater scale_h->pixels writes less often -> samples are more spaced out.

y_off = sample_y - dc_level
y_pixel_position = 240 - y_off
Greater dc_level->y_off more negative -> greater y position.

Monitor VGA Display

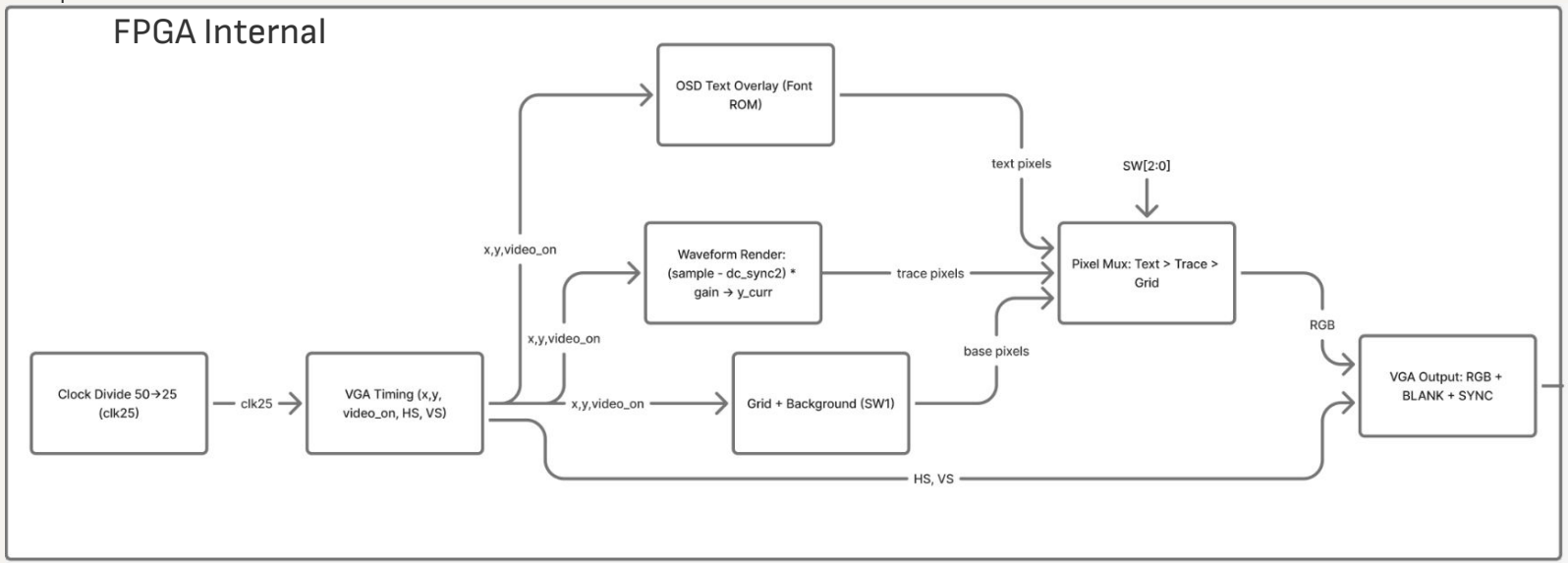


Figure 7: VGA Display sub-component block diagram (simplified).

Bugs & Issues - 1

Issue:
When we flipped the “freeze” switch, the waveform didn’t actually hold a stable frame. Instead it would keep drifting or causing unexpected outputs.

Root Cause:
The freeze signal was not stopping the capture logic. The write pointer was still advancing, which causes the window to keep sliding instead of being frozen.

Fix:
Make the write pointer stop updating when frozen. This creates one frozen frame that doesn’t continuously drift.

Bugs & Issues - 2

Issue:
The push buttons on DE1-Soc is sensitive to presses resulting in multiple unwanted increments/decrements

Root Cause:
The buttons “flickers” on/off for a few milliseconds when being pressed, the code reads it as another press.

Fix:
Implemented a edge detect logic with previous-state registers.

Bugs & Issues - 3

Issue:
Horizontal and vertical scales on the oscilloscope don’t match the real time and voltage

Root Cause:
Our scale constants in the code didn’t meet match the actual ADC range and sampling rate, so the waveform was not displaying accurate values.

Fix:
We compared the expected scale to what we actually saw on the VGA, and multiplied/divided by that factor.

Future Improvements

- Keyboard Control
- Multi-Channel Support
- Cursor and Readout System
- Math Operations (Add/subtract channels, differentiate/integrate, absolute value)
- Trigger Function (edge, pause-width, single-shot triggering, etc).
- Auto Measurements (RMS voltage, peak-to-peak voltage, rise time, etc).
- Noise Reduction Function (averaging and band-width limit).

Final Work Distribution

Farid

- Internal test signal generator
- Capture engine & decimation
- Vertical gain and mapping to screen
- Signal sampling & buffering
- Vertical/Horizontal Scaling
- Ring buffer
- Dual port RAM
- Freeze control
- Debugging and testing

Chenglong

- Method of Signal Receiving
- User Interface and readouts
- User control logic(SWs, KEYs)
- VGA display logic testing
- VGA Timing Generator
- Vertical offset control
- Combine of ADC signal with user control & display logic
- Waveform Colour Control
- Debugging and testing

Appendix A

1. Full Circuit Block Diagram
   https://drive.google.com/file/d/15AV1lZgg3-bZUVjRKzgZeGRwoNb-yMxf/view?usp=sharing