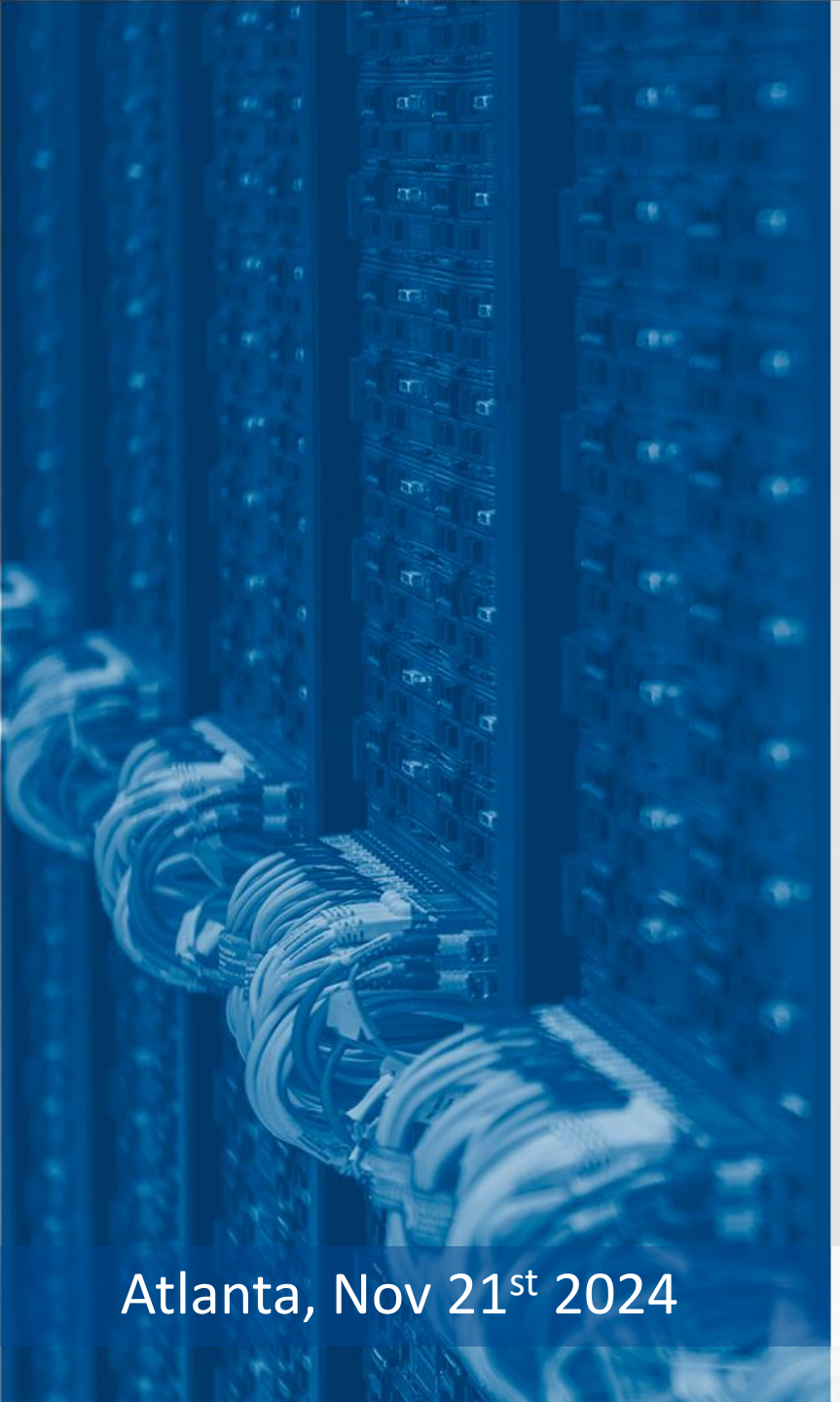

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

RISC-V testbeds

Bridging the gaps among performance analysis tools

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BoF: Advanced Architecture “Playgrounds”

Context and goals

⇨ **We are building RISC-V chips with an “extreme” design point**

- Vector Unit of 256 DP elements (i.e., registers of 16 kbits)
- Main drivers EPI and EUPILOT projects

Demo at BSC boot #3549 until 3pm

⇨ **Hardware design process takes long time**

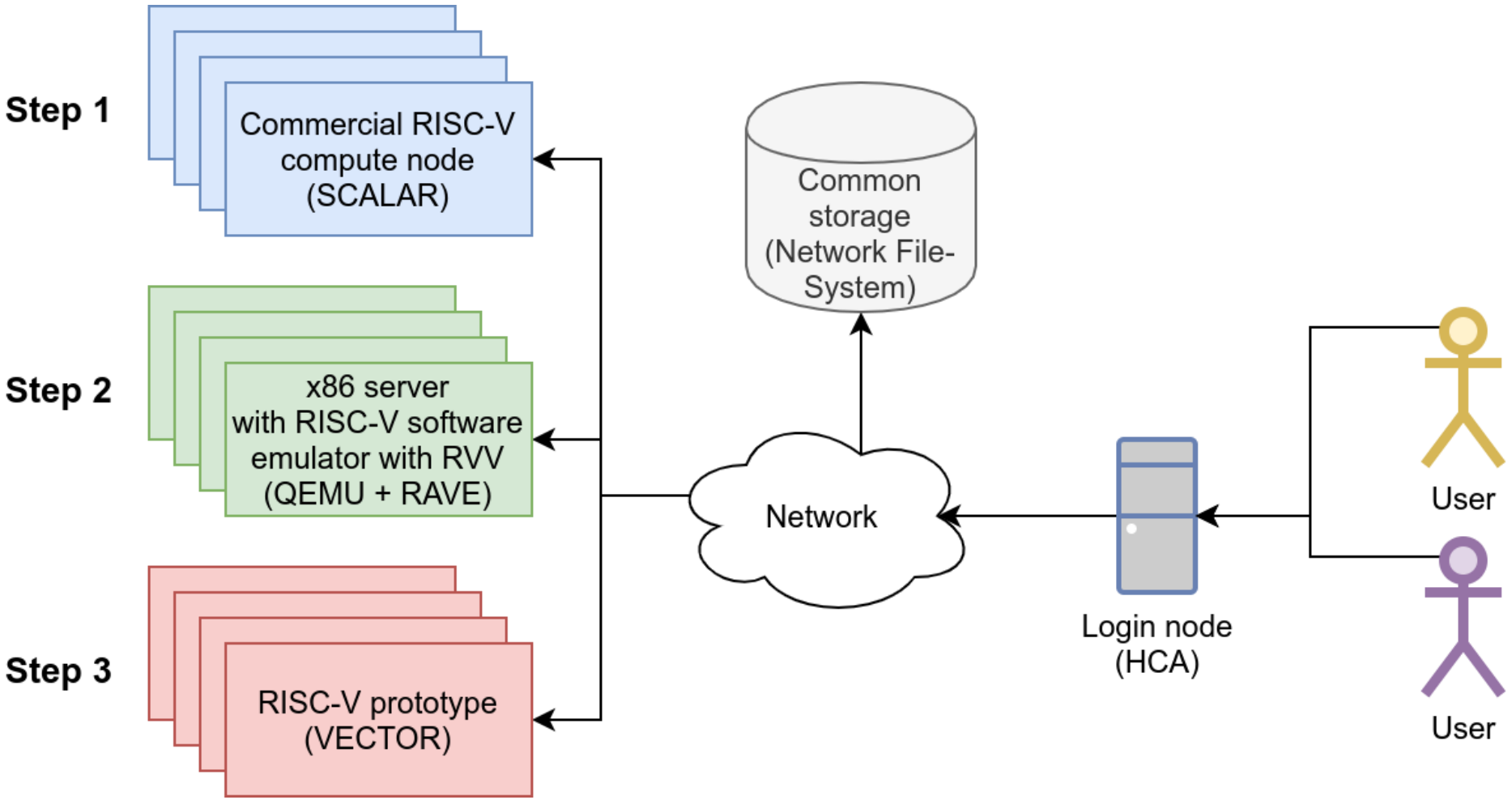
- EU project with several partners
- Coordination of the “handcraft” of making chips

⇨ **Software development needs to advance before hardware is ready**

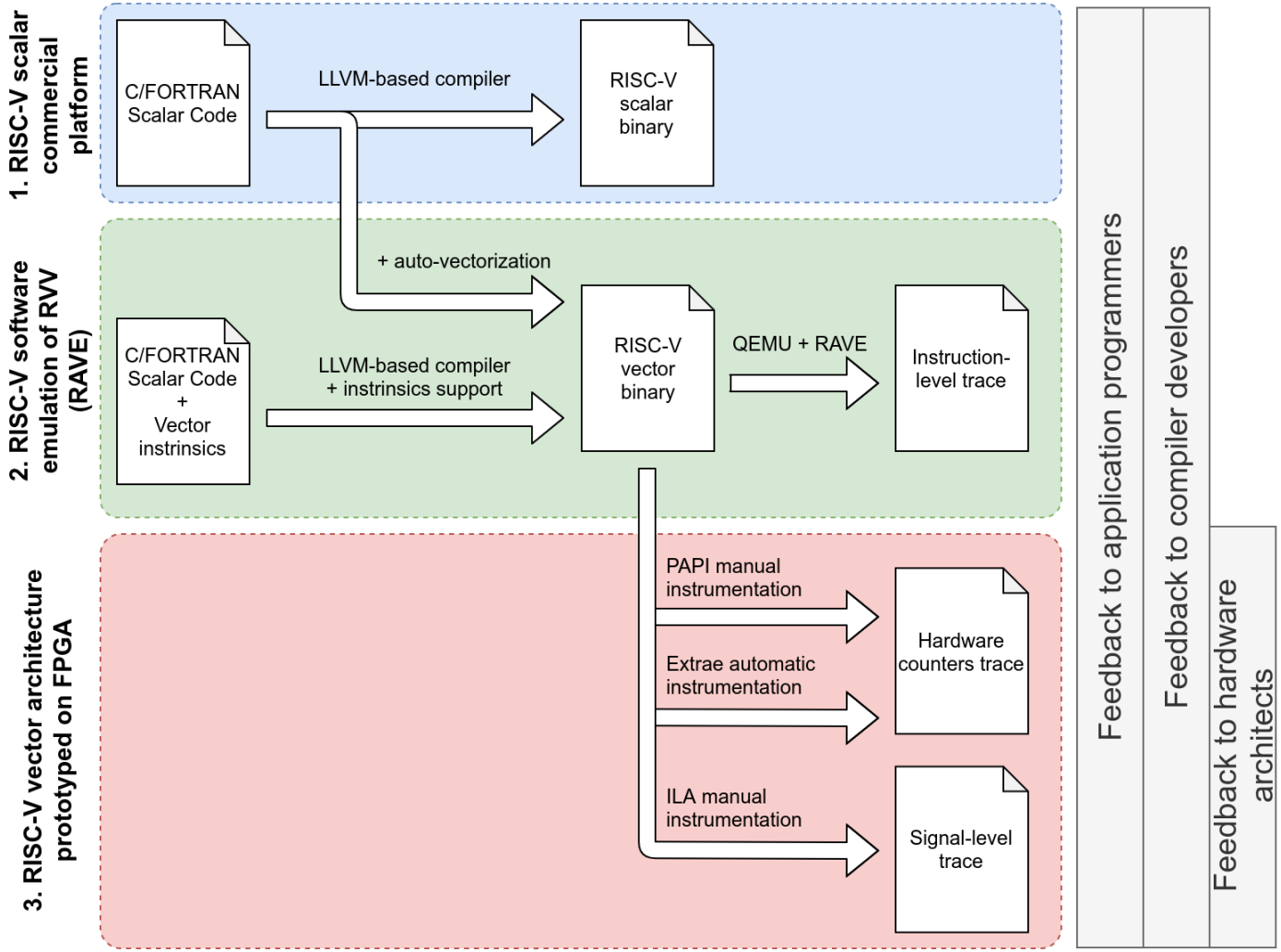
- How can we make software progress in a meaningful way even if hardware is not fully available?
- How can we explore our design point “at scale” without being even close to scale?

We call our approach
Software Development Vehicles

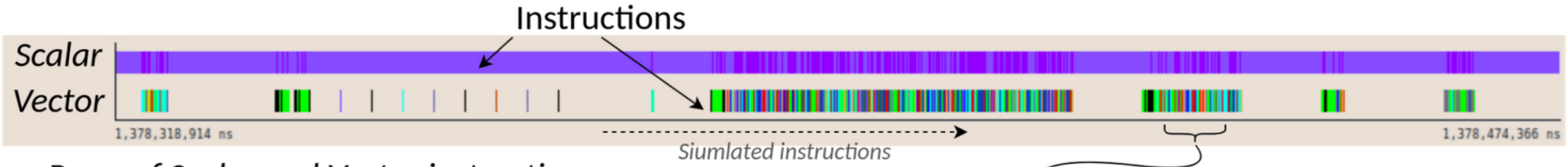
Software Development Vehicles (SDV)



Co-design with SDV

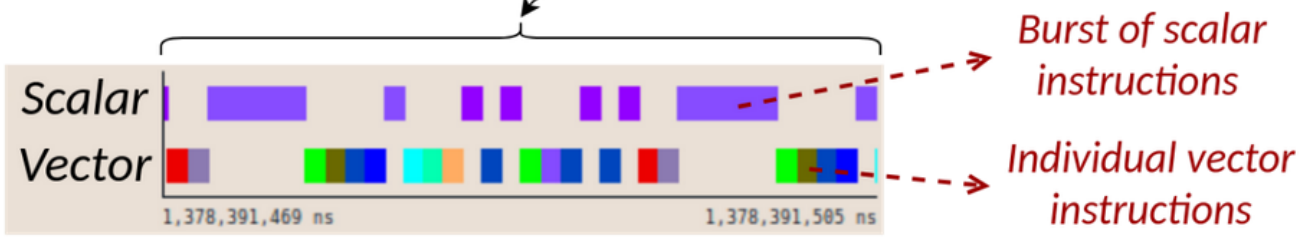


Navigate, visualize and quantify



Prop. of Scalar and Vector instructions

	Init	BU	TD	Bit->Q (c)	Q->Bit (e)
qemu_scalar	0.62	0.63	1.00	0.81	0.74
qemu_vector	0.38	0.37	0.00	0.19	0.26



Assembly of instructions (In phase Init)

	vsub	vsll	vsetvl	vle	vmerge	vmv	vsxe	vmseq	scalar
qemu_scalar	-	-	640	-	-	-	-	-	641
qemu_vector	128	128	-	256	128	128	128	128	-

Average bits per instruction (In phase Init)

vsub	vsll	vle	vmerge	vmv	vsxe	vmseq
16,382.50	16,382.50	16,382.50	16,384	16,384	16,382.50	16,382.50

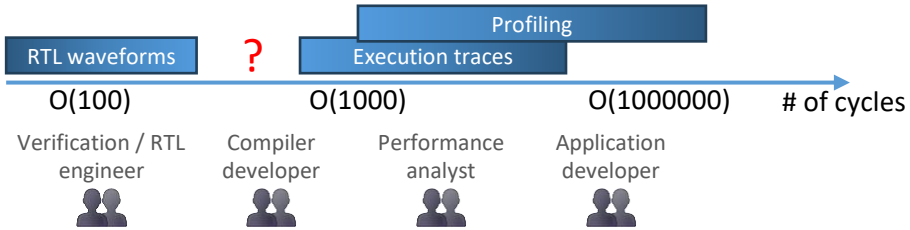
The lesson learned… and a crazy proposal

⇨ This is not only for benchmarks and mini-apps: we studied complex codes with meaningful use cases

- **Plasma physics**: Vlasiator, PIConGPU, BIT1, GENE-X
- **CFD**: Alya, WaLBerla
- **Earth Science**: miniFALL-3D
- **Molecular dynamics**: GROMACS
- **Weather forecast**: ECMWF dwarf

⇨ It is important to have tools for analyzing the performance

- At different scale
- With different granularity
- Dynamically



Technology providers may open visibility to some internals of their hardware?

- Provide emulators
- Tracing the PC and opcode of instructions?
- Monitoring addresses of memory accesses?
- Easily expose metrics (Bytes/FLOP)?

Resources

- Mantovani, Filippo, et al. "Software Development Vehicles to enable extended and early co-design: a RISC-V and HPC case of study." International Conference on High Performance Computing. Cham: Springer Nature Switzerland, 2023. https://arxiv.org/abs/2306.01797

- Vizcaino, Pablo, et al. "Short reasons for long vectors in HPC CPUs: a study based on RISC-V." Proceedings of the SC'23 Workshops of The International Conference on High Performance Computing, Network, Storage, and Analysis. 2023. https://arxiv.org/abs/2309.06865

- Vizcaino, Pablo, et al. "RAVE: RISC-V Analyzer of Vector Executions, a QEMU tracing plugin." https://arxiv.org/abs/2409.13639

- Blancafort, Marc, et al. "Exploiting long vectors with a CFD code: a co-design show case." 2024 IEEE International Parallel and Distributed Processing Symposium (IPDPS). IEEE, 2024. https://arxiv.org/abs/2411.00815

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