Chris Abajian

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OBJECTIVE

To build upon and utilize knowledge of digital design principles through full-time employment. Available January 2022.

EDUCATION

Rochester Institute of Technology, Rochester, NY
Bachelor of Science, Major in Computer Engineering, Minor in Mathematics. Expected December 2021.
GPA: 3.78/4.00
Awards: Dean's List Fall 2017 - present.

SKILLS

Languages:

- Most experience with: Verilog, VHDL, C, Java, Python, Matlab, HTML
- Some experience with: C++, JavaScript, Tcl, Bash, ARM Assembly

Software: Linux, Git, RCS, ModelSim/Riviera, Vivado Design Suite, Altera Quartus, MicroBlaze
Standards: IEEE 802.3 (Ethernet), ITU (OTN, Flex-O, FibreChannel, Sonet), IP-XACT

PROJECTS/LABS

Supplemental project information can be found on my portfolio, chrisabajian.com.

- Programmed an intelligent motorized race car in C that won first place in a competition against other classmates. A FRDM K64F microcontroller interfaced with a motor shield that drove two DC motors, a line scan camera, and a steering servo.
- Implemented a median-filter on an FPGA using UART and AXI protocols.
- Created a portable, solar-powered Bluetooth weather station using Arduino and developed an Android application for the User Interface. Published a detailed project write-up on instructables.com.
- Developed a web-app for nearby high school students to carpool to and from school during a bus shortage.
- Developed a color matching game for the Freedom KL46Z board which incorporated a serial I/O driver, a timer driver, and general-purpose IO pins for LED indicators. Written in both ARM Assembly and C.

EXPERIENCE

Digital Engineer Co-op, Xelic, Inc. *January 2020 – Present*

- Independently designed new IP on the cutting edge of networking standards. Produced RTL diagrams, Verilog design components, and elementary SystemVerilog testbenches.
- Converted a pre-existing core designed for an ASIC to a design suitable for the Stratix V FPGA family. Timing critical paths were pipelined and optimized for an FPGA target.
- Characterized a new Forward Error Correction (FEC) core in hardware by modifying a TCL test environment for improved data logging. Net Code Gain charts were constructed using Microsoft Excel.
- Consistently worked to minimize resource utilization and timing-critical paths on high-bandwidth designs.

Teaching Assistant, RIT *August 2020 – December 2020*

- Provided in-lab assistance and graded assignments for the Applied Programming in C course.

Web Developer, Schill Insurance Group, LLC. *May 2018 – September 2018*

- Designed and built the company website from the ground-up using Grav CMS for dynamic client creation and page edits. Implemented PGP encryption for enrollment forms.

ACTIVITIES/INTERESTS

Consumer PC hardware; Paddleboarding; Weight lifting; Soccer; Guitar; STEM Academy 2013-2017.