CMPE-260 Laboratory Project Part Two

Pipelined MIPS Processor

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students; however, other than code provided by the instructor for this exercise, all code was developed by me.

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Results and Analysis

In digital logic, a flip-flop assigns its output to its input on a clock edge. Theoretically, if a signal were to change right before this edge, the flip-flop will respond accordingly. However, due to the transistor-level design of the flip-flop, this isn't the case. In fact, because the signals within a flip-flop can only update so fast, there are times preceding and following the clock edge that require the input signal to be stable for the flip-flop to produce a stable result. These times are called the setup and hold times. A setup time is the time a signal must be constant before the clock edge, and a hold time is the time after a clock edge where the signal must remain stable. If a clock is too fast in a design, one or both timing constraints may be violated. Table 1 shows several clock frequencies and where timing violations occurred.

Table 1: Clock Frequency Implementation Results

Clock Frequency (MHz)	Violations
10	0
20	0
70	0
100	0
110	0
120	28

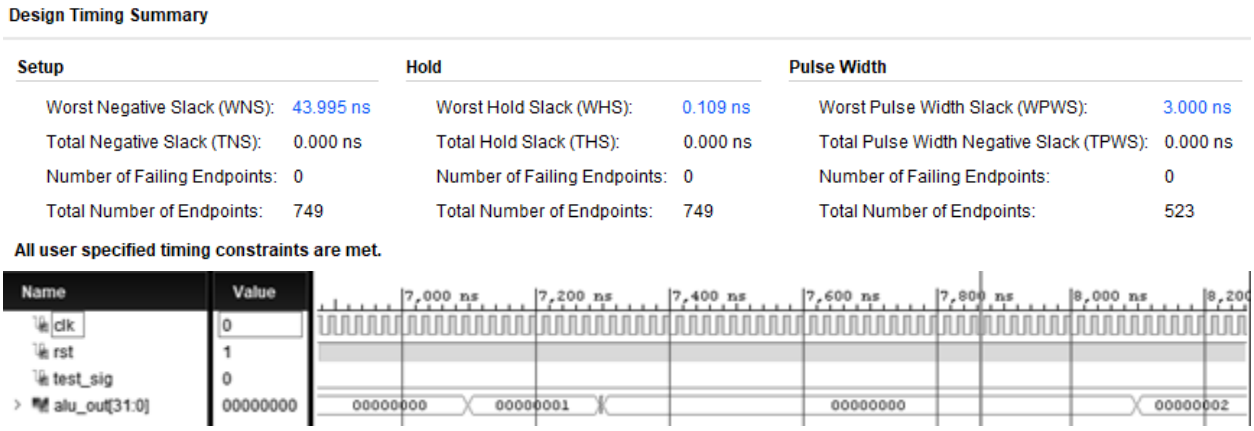

Figure 1: Implementation summary for a clock frequency of 10 MHz.

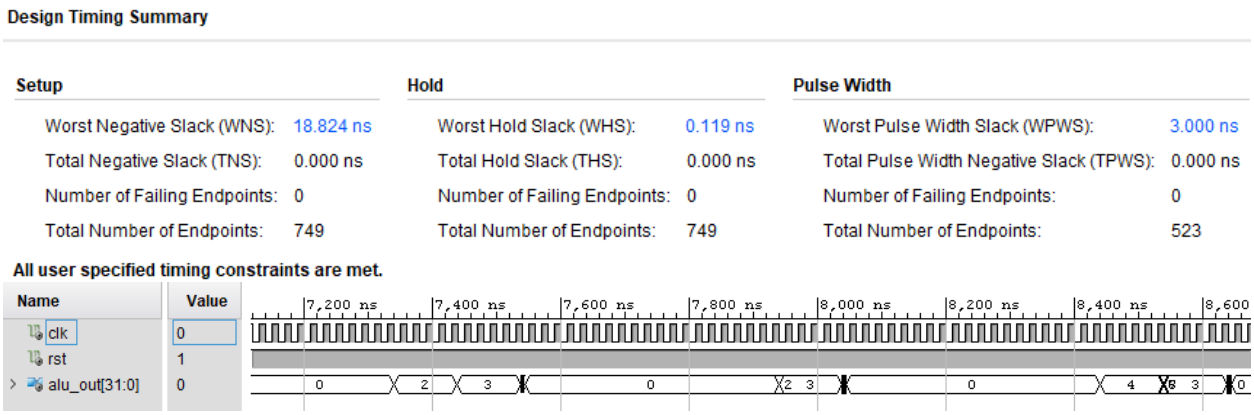

Figure 2: Implementation summary for a clock frequency of 20 MHz.

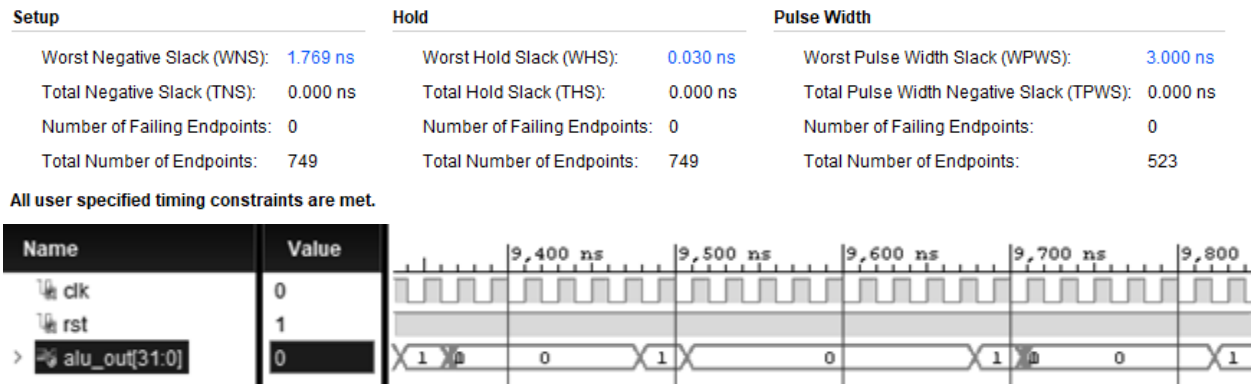

Figure 3: Implementation summary for a clock frequency of 70 MHz.

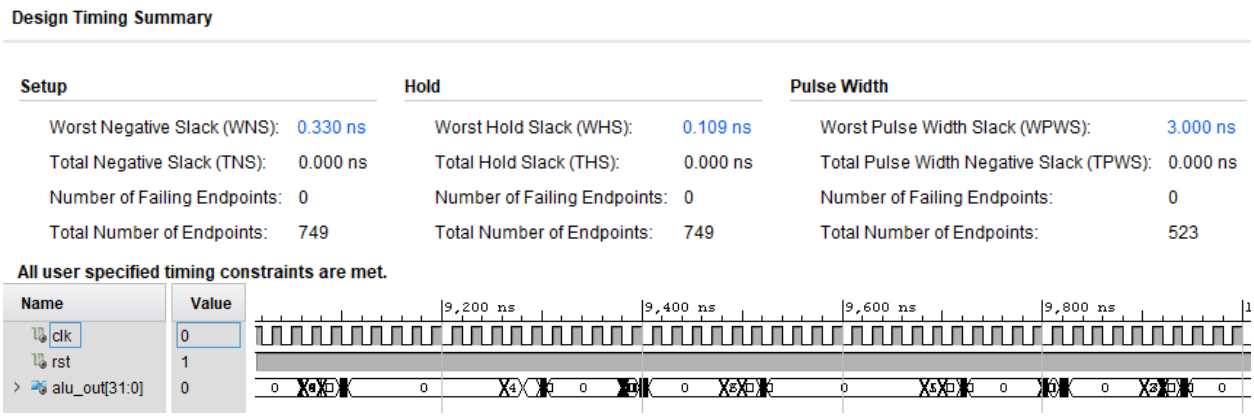

Figure 4: Implementation summary for a clock frequency of 100 MHz.

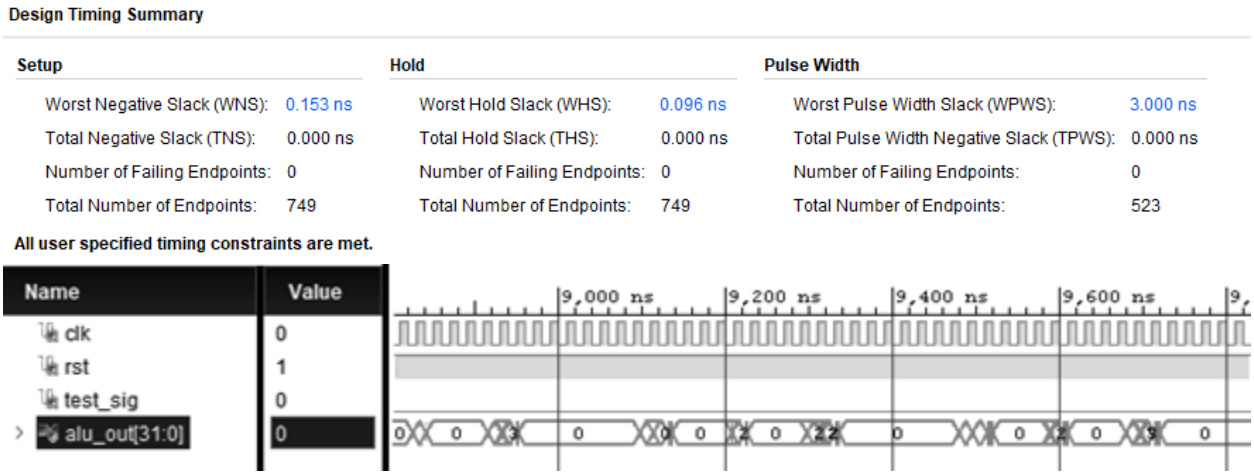

Figure 5: Implementation summary for a clock frequency of 110 MHz.

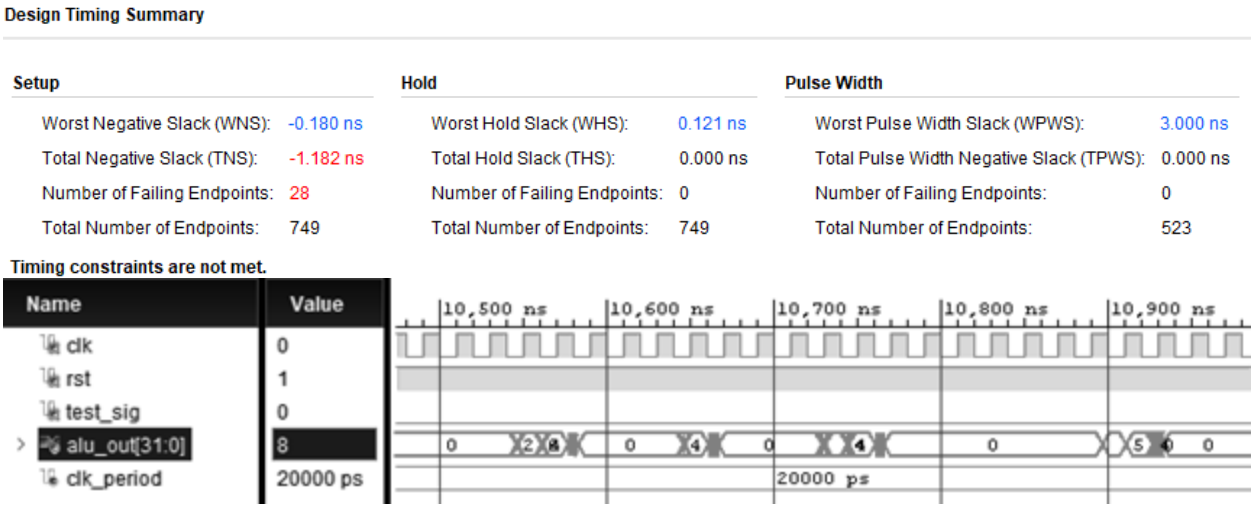

Figure 6: Implementation summary for a clock frequency of 120 MHz.

The clock frequency of 120 MHz violated the setup time of flip-flops 28 times. The maximum operating frequency of this design is at 110 MHz (assuming clock intervals of 10 MHz).