Directed Test Generation for Validation of Cache Coherence Protocol

Abhinaba Chakraborty

¹ ISI, Kolkata, cs2109@isical.ac.in

August 24, 2022



Table of Contents

- 1 Introduction
- 2 ON THE FLY Test Generation
- 3 Algorithm
- 4 Analysis

SHORT TITLE

Main Author

Introduction

ON THE FLY
Test

Algorithm

Introduction

SHORT TITLE

Main Author

Introduction

ON THE FLY Test

A.1. *.1

Algorithm

Background

- Modern Computers employed different cache coherence protocols to ensure the consistency of data (the goal is to ensure that a cache should read the latest most recently read data)
- However modern cache coherence protocols are very complicated, so their global finite state spaces are very complicated to analyze.

SHORT TITLE

Main Author

Introduction

ON THE FLY
Test
Generation

Algorithm

Background Continued ...

- One naive solution to generate random test cases. But for that, there are timing constraints, that we have to generate a huge number of test cases.
- Better improvement is to use Breadth First Search (BFS) to cover all the transitions. But the problems are twofold:
- For BFS worst-case space complexity is $\mathcal{O}(2^n)$
- For BFS number of repeated transactions is higher.

SHORT TITLE

Main Author

Introduction

ON THE FLY
Test
Generation

Algorithm

_

ON THE FLY Test Generation

SHORT TITLE

Main Author

Introduction

ON THE FLY
Test
Generation

Algorithm

Algorithm

SI Protocol

Reference: [1]

- SI is basically a trimmed version of MSI Protocol, in which we don't allow cores to allow to issue store operation.
- Let's say a system has n cores, a global valid state would be: m cores are in I state, and other n-m states are in S state.
- So it can be easily seen that global state space has 2^n states.
- Any core can change its state (S->I) or (I->S) within one transaction.
- ullet For every state there would be n outgoing edges and n incoming edges.

SHORT TITLE

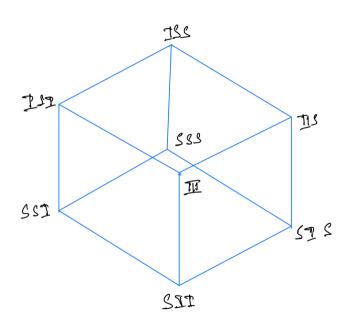
Main Author

Introduction

ON THE FLY
Test
Ceneration

Algorithm

SI Protocol Continued...



SHORT TITLE

Main Author

ntroduction

ON THE FLY
Test
Generation

Algorithm

Algorithm

SHORT TITLE

Main Author

ntroduction

ON THE FLY Test Generation

Algorithm

Algorithm 1 Test generation for SI protocol with n cores

Create Tests SI(n)

- 1: **for** r = 0 to n 1 **do**
- 2: VisitHypercube(n, r)

VisitHypercube(m,r)

- 3: $p = (m+r) \mod n$
- 4: Output "load(p)"
- 5: **for** i = 1 to m 1 **do**
- 6: VisitHypercube(i, r)
- 7: Output "evict(p)"
- 8: return

SHORT TITLE

Main Author

Introduction

ON THE FLY
Test
Generation

Algorithm

Analysis

SHORT TITLE

Main Author

ntroduction

ON THE FLY
Test
Generation

Algorithm

Aigoritiiii

Time and Space Complexity

• The n-dimensional hypercube is partitioned into n isomorphic trees with no overlapping edges.

SHORT TITLE

Main Author

Introduction

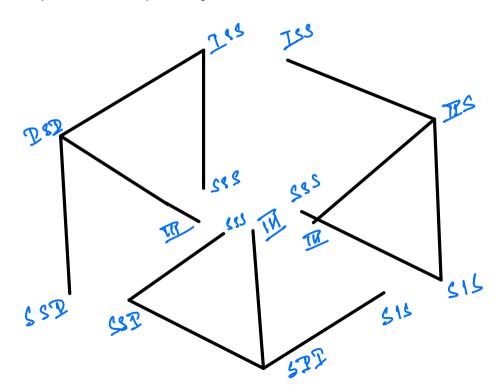
ON THE FLY
Test

Maarithm

Algorithm

nalvsis

Time and Space Complexity Continued...



SHORT TITLE

Main Author

ntroduction

ON THE FLY
Test
Generation

Algorithm

Time and Space Complexity Continued...

- Once the hypercube is correctly formed we performed an Euler tour on the tree as all the edges are bidirectional.
- There are $n2^n$ transitions within state space.
- Transition sequence produced by the algorithm is $n2^n$
- No transition is visited more than once when we apply this algorithm.

SHORT TITLE

Main Author

Introduction

ON THE FLY Test Generation

Algorithm

مادراه

Time and Space Complexity Continued...

- Time Complexity is still the same as BFS i.e $\mathcal{O}(2^n)$
- Space complexity is low i.e $\mathcal{O}(n)$

SHORT TITLE

Main Author

Introduction

ON THE FLY Test

Generation

References I



Y. Lyu, X. Qin, M. Chen, and P. Mishra, "Directed test generation for validation of cache coherence protocols," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 38, no. 1, pp. 163–176, 2019.

SHORT TITLE

Main Author

Introduction

ON THE FLY Test Generation

Macrithm

Algorithm

Analysis

◆□▶◆□▶◆壹▶◆壹▶