Lab 2 Postlab

1. Why can’t you use both pins PA0 and PC0 for external interrupts at the same time?

Both of those pins are inputs to the same multiplexer for the 0th pin of each GPIO. There are only 16 external interrupt slots but many more GPIO pins, so they must be divided in some way. We can only use one gpio for each of the 16 pins.

2. What software priority level gives the highest priority? What level gives the lowest?

0 is the highest, 3 is the lowest

3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?

Each interrupt has 8 bits for the priority level, only the 2 most significant are used for the 4 priority levels. The remaining 6 are unused.

4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.

I measured an exactly zero delay with the Discovery board’s logic analyzer. I suspected the discovery board didn’t have the capabilities for this so I used the lab oscilloscope to measure about a 0.95ms delay between the start of the button voltage rise and the start of the LED voltage change.

5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?

There is no default code anywhere to clear the status bit. The only code run is inside the interrupt handler, so it needs to be responsible for clearing the bit.