Hazard Lab

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1. Calculated CPI with stalls = 1.6414
   Ideal CPI = 1.0
   CPI With Stalls Calculation
   CPI = total number of cycles/total number of instructions
   = (total instructions + num of 1 cycle stalls + 2 * num of 2 cycle stalls)/total instructions
   = 1.6414
   = 64.14 % slowdown

2. Calculated CPI with stalls = 1.4129
   CPI With Stalls Calculation
   CPI = (total instructions + num of 1 cycle stalls + 2 * num of 2 cycle stalls)/total instructions
   = 1.4129
   =41.29 % slowdown

   The two cycle stall was a load to use hazard because it's WX forwarding. The one cycle stall is a normal raw hazard which uses MX forwarding.

3. Calculated CPI with stalls = 1.1584
   CPI With Stalls Calculation
   CPI = (total instructions + num of 1 cycle stalls + 2 * num of 2 cycle stalls)/total instructions
   = 1.1584
   =15.84 % slowdown

   The one cycle stall can be caused by a WAW dependency with 1 interweaved independent instruction or a structural hazard. The two cycle stall is a back to back WAW dependency.

   We used the O1 compilation flag. We have two loops, the first loop creates a 2 cycle stall for MAX_2CYCLE iterations. The second loop creates a 1 cycle stall for MAX_1CYCLE iterations.

   To calculate 2 cycle stall it would be 2 consecutive dependent instructions. First instruction writes to a register, while the second reads from the same register. Refer to line 53 which points out that variable a is being written to and then read from by the subsequent instruction on line 54. This will cause a RAW hazard that forces the pipeline to stall for 2 cycles. Refer to the comments from line 42 to 48 which has the assembly code clearly showing register 2 having the RAW hazard.

   To calculate 1 cycle stall it would be 2 dependent instructions seperated by 1 independent instruction. Refer to line 72 which points out that variable h is written to, and then on line 73 an independent instruction is added for padding. The next instruction on line 74 reads from h, and causes a RAW hazard that forces the pipeline to stall for 1 cycle. Refer to the comments from line 62 to 68 which has the assembly code clearly showing register 2 having the RAW hazard.