CET 141: Day 13

Dr. Noori KIM

Current – Voltage relationship $I = f(V)$ for two terminal devices.

Linear elements

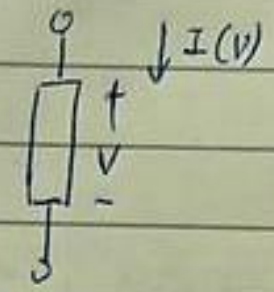
$I = V/R$

$I = C \cdot dV/dt$

$I = \frac{1}{L} \int V dt$

Nonlinear elements

$I = I_s [e^{V/nV_T} - 1]$



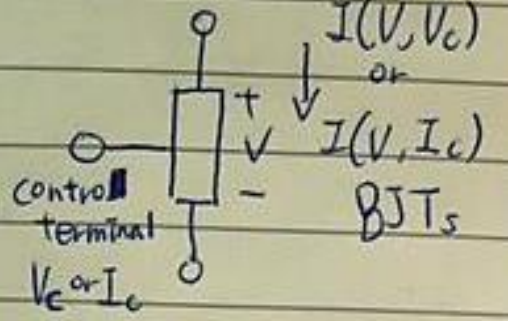
Transistors ⇒ adding a third terminal

① Type 1 : BJT

⇒ Current – controlled current flow.

② Type 2 : FETs

⇒ Voltage – controlled current flow

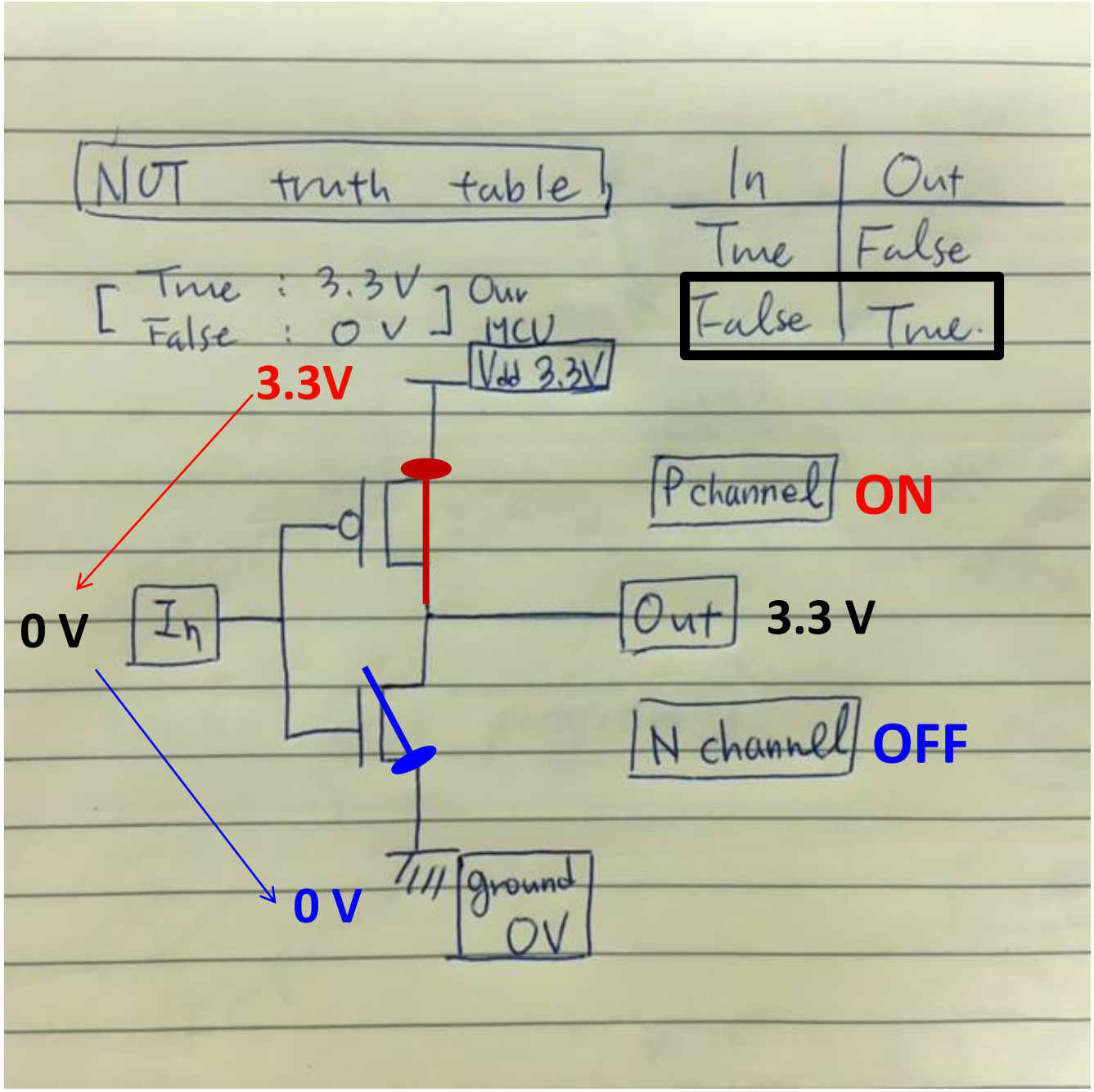


Transistor

- Basic: Back-to-back two diode connection
- Three terminal component
  - i.e., Gate Source Drain / Collector Base Emitter
  - Transistor as a switch: Push button, + and – terminals
  - Transistor as an amplifier

Logic gate

- An idealized or physical device implementing a Boolean function
  - Performs a logical operation on one or more logical inputs
  - Produces a single logical output
- **Basic building elements: transistors**
  - In modern practice, most gates are made from field-effect transistors (FETs), particularly **MOSFETs**.



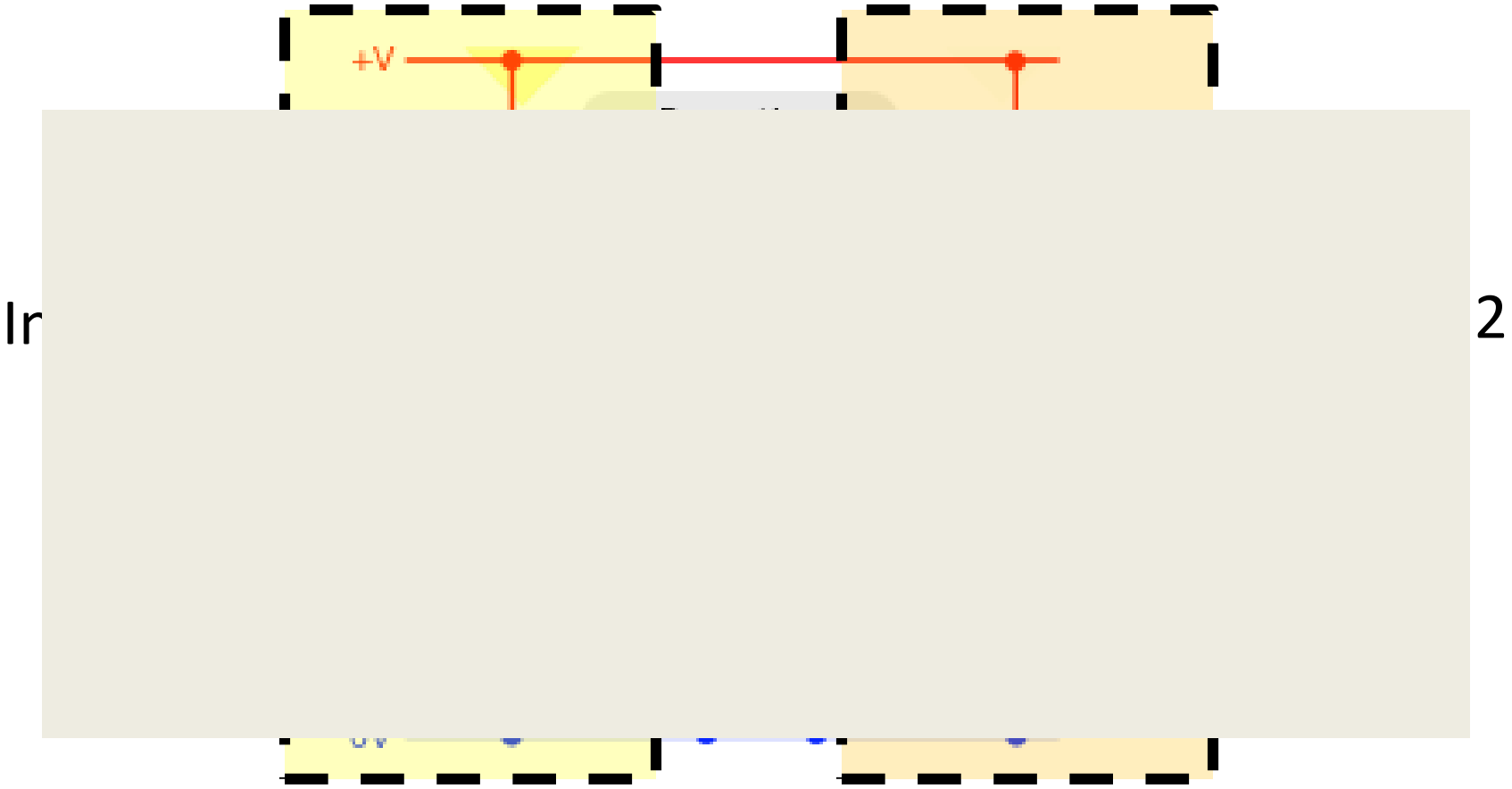
A basic element to represent a bit

This is a NOT symbol

Or an inverter

Latch

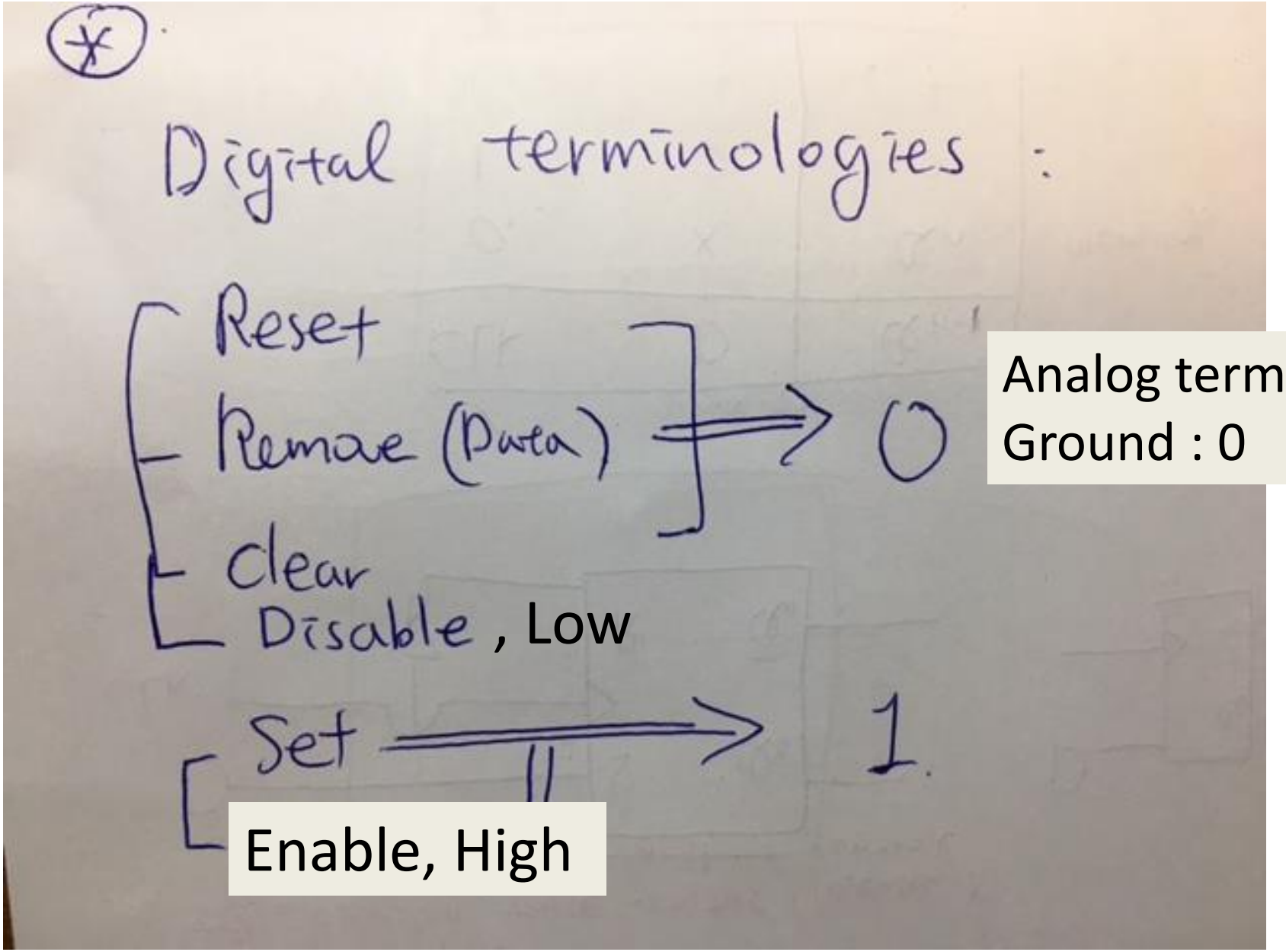
- Basic element: Two inverters



- A bistable multivibrator

Flip flop

- Basic storage elements for todays registers and memories
  - Bistable multivibrator
  - Feedback path
- Basic element: two latches (master and slave) with a forcing switch
  - Synchronous devices
  - Operates on clock edges
- Example: SR, D, T flip flops


Digital terminologies :
Reset
Remae (Data)
0
clear
Disable , Low
Set
1.
Enable, High
Analog term.
Ground : 0

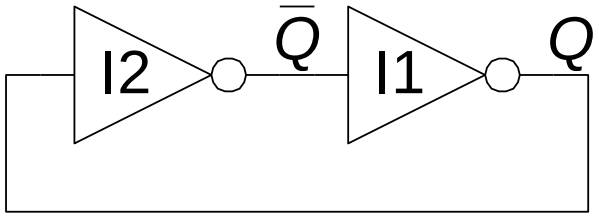
- Outputs of sequential logic depend on current *and* prior input values – it has ***memory***.
- Some definitions:
  - **State:** all the information about a circuit necessary to explain its future behavior
  - **Latches and flip-flops:** **state elements** that store one bit of state
  - **Synchronous sequential circuits:** combinational logic followed by a bank of flip-flops

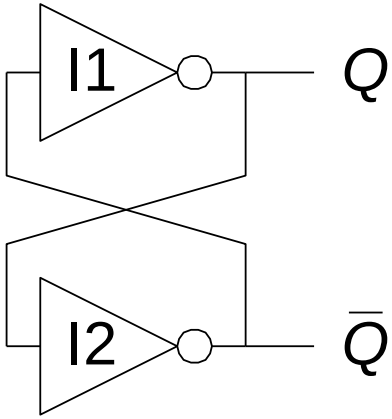
More about State Elements

- The state of a circuit influences its future behavior
- State elements store state
  - Bistable circuit
  - SR Latch
  - D Latch
  - D Flip-flop
  - JK, T Flip-flops

Bistable Circuit

- Fundamental building block of other state elements
- Two outputs: Q, $\overline{Q}$
- No inputs

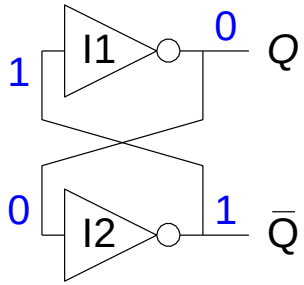




Bistable Circuit Analysis

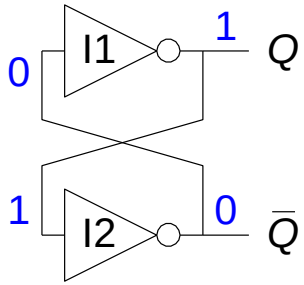
- Consider the two possible cases:
  - ***Q* = 0:**

    then $Q = 0$, $\bar{Q} = 1$ (consistent)



  - ***Q* = 1:**

    then $Q = 1$, $\bar{Q} = 0$ (consistent)



- Stores 1 bit of state in the state variable, Q (or $\bar{Q}$)
- But there are **no inputs to control the state**

A Latch

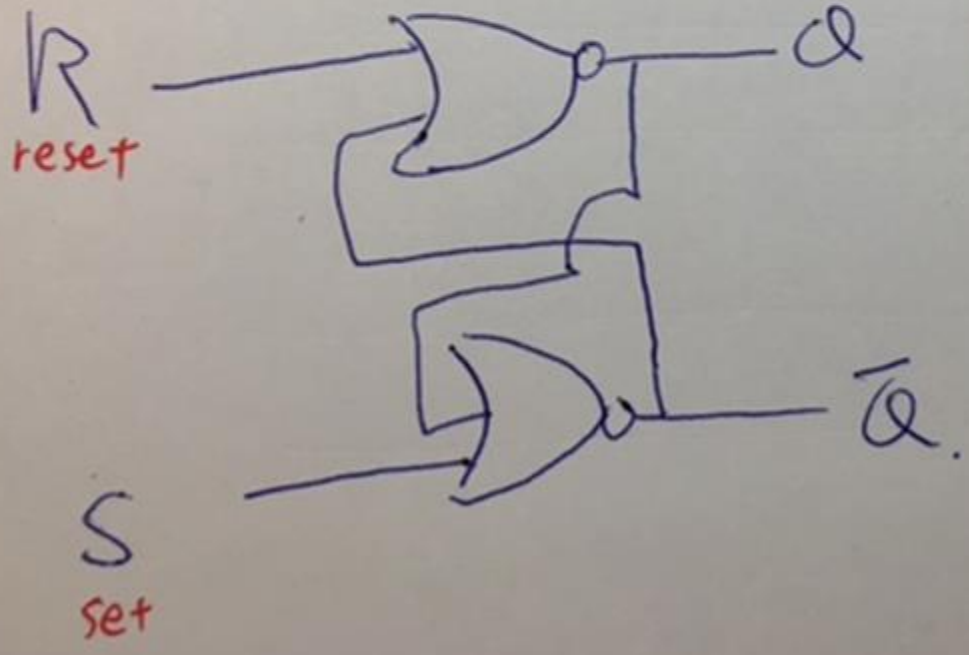
- We want to latch a bit information from input

SR Latch : NOR type ✓

NAND type.

⇓

It latches "0" or "1"



$\bar{Q}$ ↘

[Reset means Output = 0

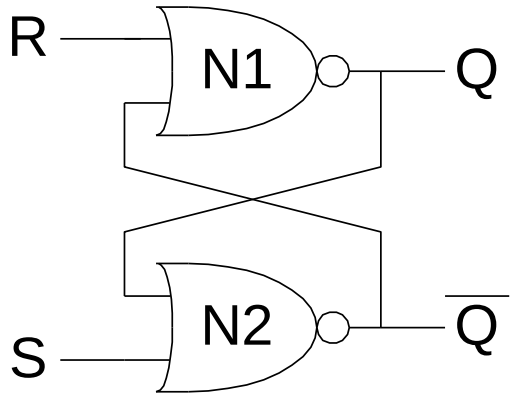
[Set " 0 = 1

R=1 $\bar{Q}$=0

S=1 $\bar{Q}$=1

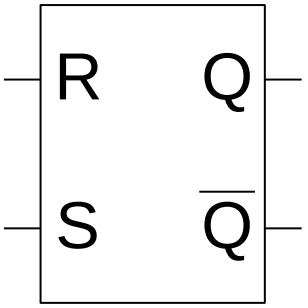
SR (Set/Reset) Latch

- SR Latch



- Consider the four possible cases:
  - $S = 1, R = 0$ SET
  - $S = 0, R = 1$ RESET
  - $S = 0, R = 0$ MEMORY
  - $S = 1, R = 1$ INVALID

SR Latch Symbol



A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

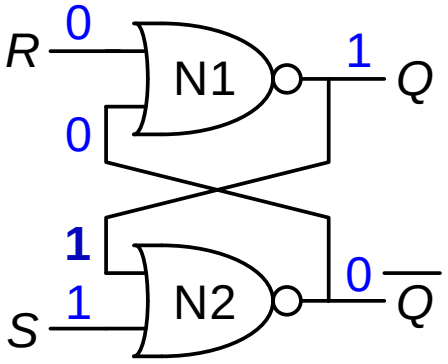
0 when one of inputs is high

SR Latch Analysis

– ***S* = 1, *R* = 0:**

then $Q = 1$ and $\overline{Q} = 0$

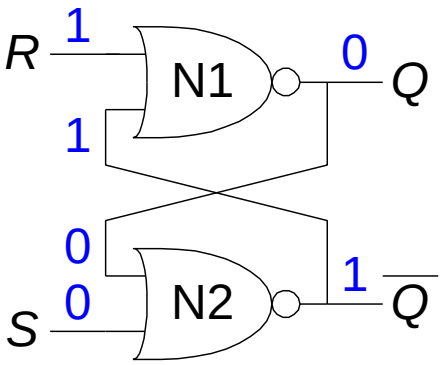
***Set* the output**



– ***S* = 0, *R* = 1:**

then $Q = 0$ and $\overline{Q} = 1$

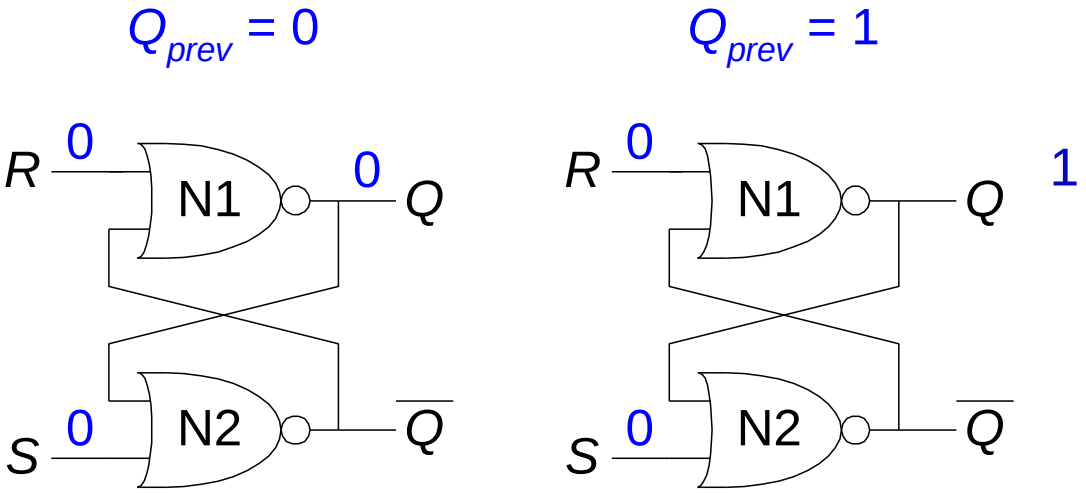
***Reset* the output**



– ***S* = 0, *R* = 0:**

then $Q = Q_{prev}$

Memory!

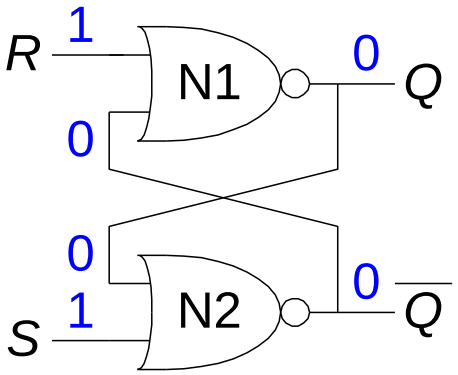


– ***S* = 1, *R* = 1:**

then $Q = 0, \overline{Q} = 0$

Invalid State

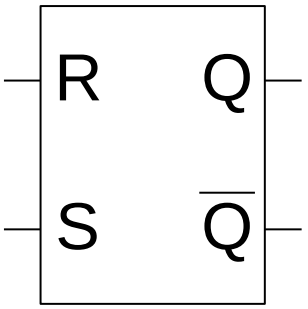
$Q \neq$ NOT Q



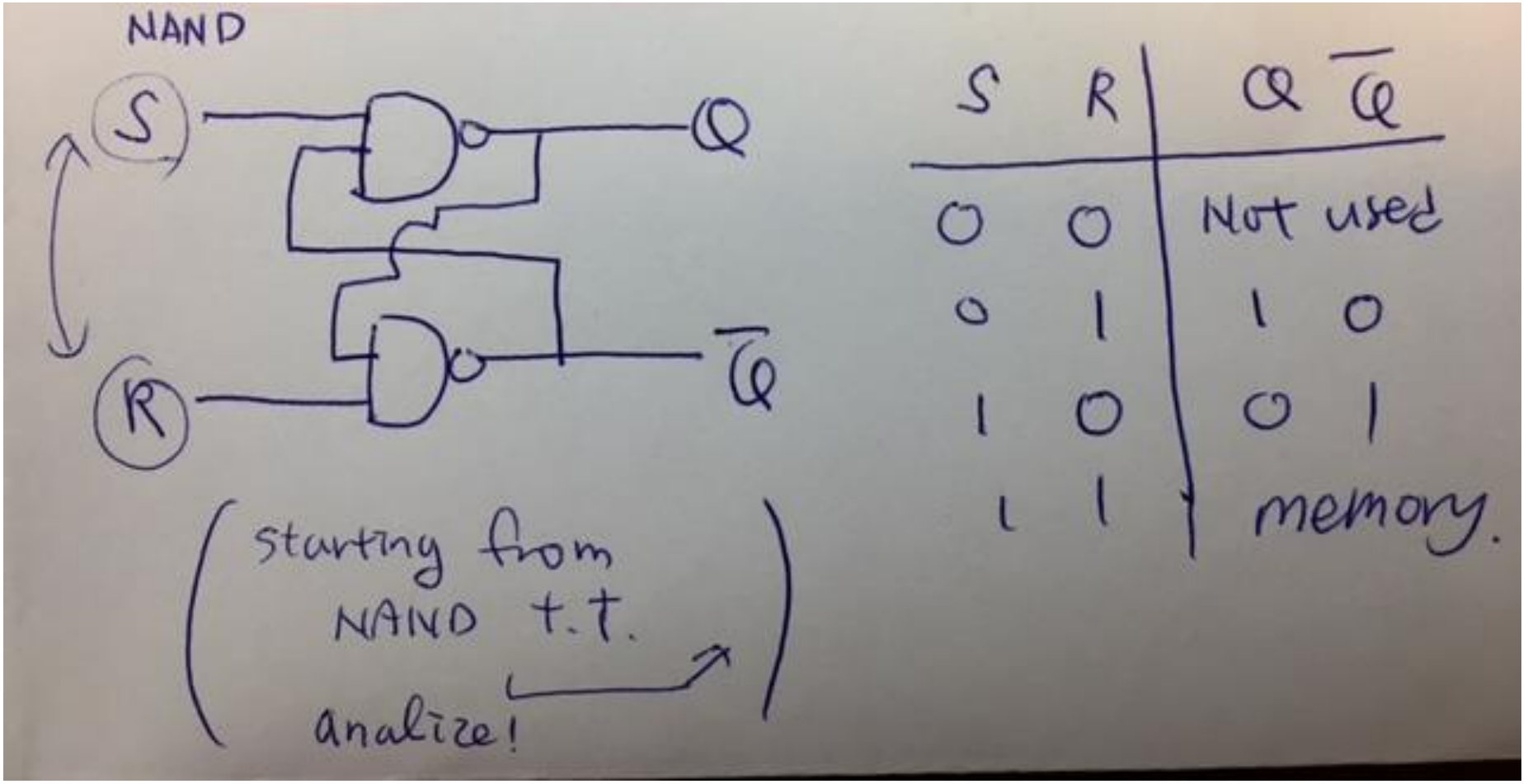
SR Latch Symbol

- SR stands for Set/Reset Latch
  - Stores one bit of state (Q)
- Control what value is being stored with S, R inputs
  - **Set:** Make the output 1 ($S = 1, R = 0, Q =$ **1**)
  - **Reset:** Make the output 0 ($S = 0, R = 1, Q =$ **0**)
- **Must do something to avoid invalid state (when $S = R = 1$)**

SR Latch Symbol



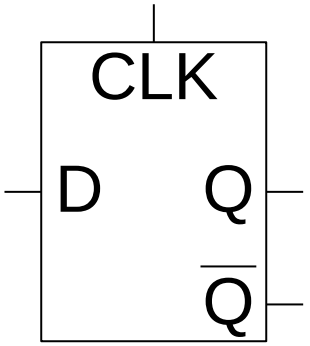
Try NAND type SR latch as well



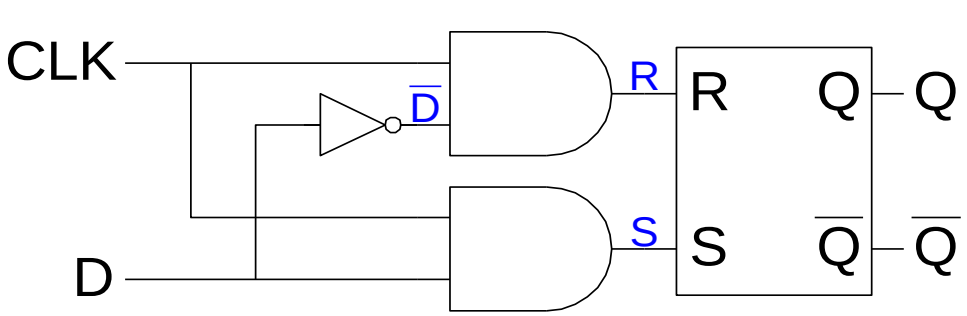
D Latch

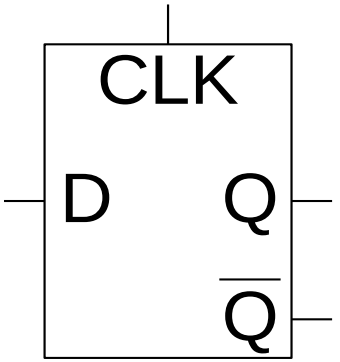
- Two inputs: *CLK*, *D*
  - ***CLK*:** controls *when* the output changes
  - ***D*** (the data input): controls *what* the output changes to
- Function
  - When ***CLK* = 1**,
    D passes through to *Q* (*transparent*)
  - When ***CLK* = 0**,
    Q holds its previous value (*opaque*)
- Avoids invalid case when
  $Q \neq \text{NOT } \overline{Q}$

D Latch Symbol



D Latch Internal Circuit



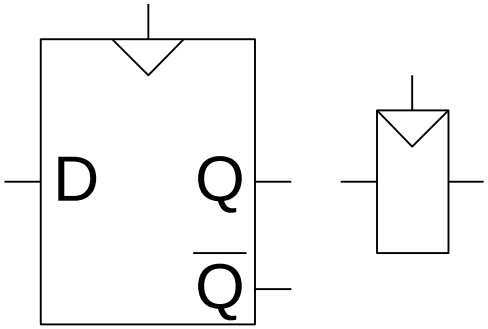


CLK	*D*	$\overline{D}$	*S*	*R*	*Q*	$\overline{Q}$
0	X					
1	0					
1	1					

D Flip-Flop

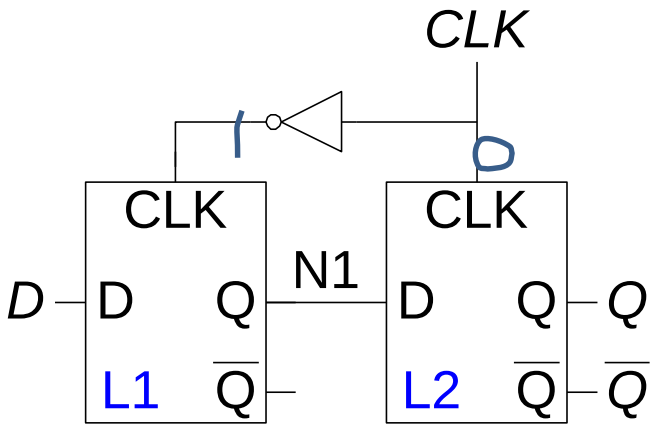
- **Inputs:** *CLK*, *D*
- **Function**
  - Samples *D* on rising edge of *CLK*
    - When *CLK* rises from 0 to 1, *D* passes through to *Q*
    - Otherwise, *Q* holds its previous value
  - *Q* changes only on rising edge of *CLK*
- Called *edge-triggered*
- Activated on the clock edge

D Flip-Flop Symbols



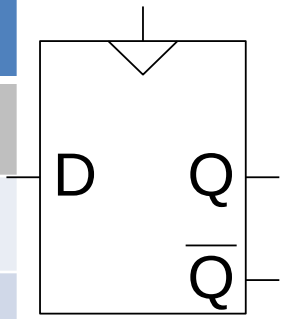
D Flip-Flop Internal Circuit

- Two back-to-back latches (L1 and L2) controlled by complementary clocks
- When ***CLK* = 0**
  - L1 is transparent
  - L2 is opaque
  - *D* passes through to N1
- When ***CLK* = 1**
  - L2 is transparent
  - L1 is opaque
  - N1 passes through to *Q*
- Thus, on the edge of the clock (when ***CLK* rises from 0→1**)
  - *D* passes through to *Q*

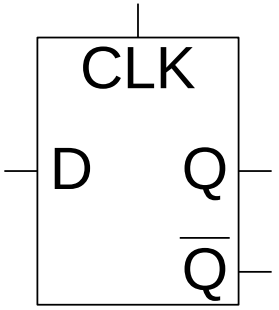


D flip flop vs. D latch truth tables

CLK	D	Q_{n+1}
0	x	Q_n (No Change - memory)
1	0	0
1	1	1

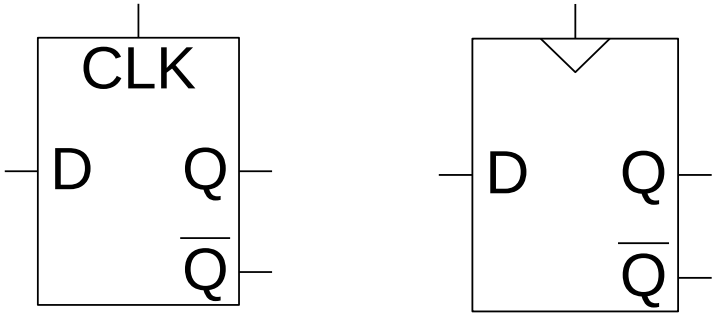


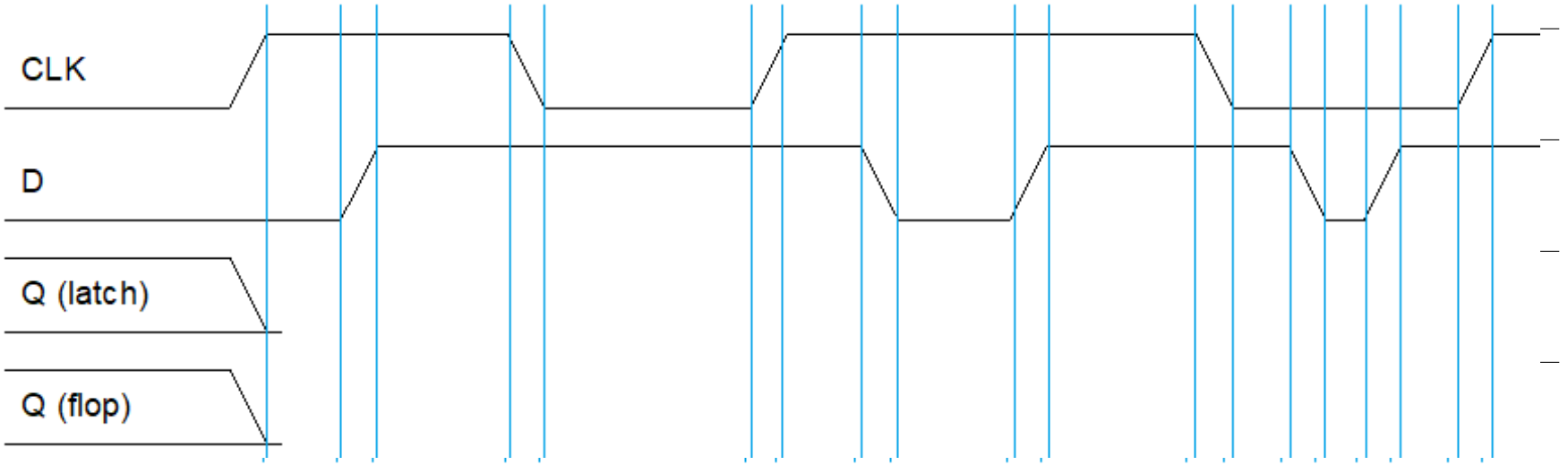
CLK	D	$\overline{D}$	S	R	Q	$\overline{Q}$
0	X	$\overline{X}$	0	0	Q	$\overline{Q}$
1	0	1	0	1	0	1
1	1	0	1	0	1	0



SAME?

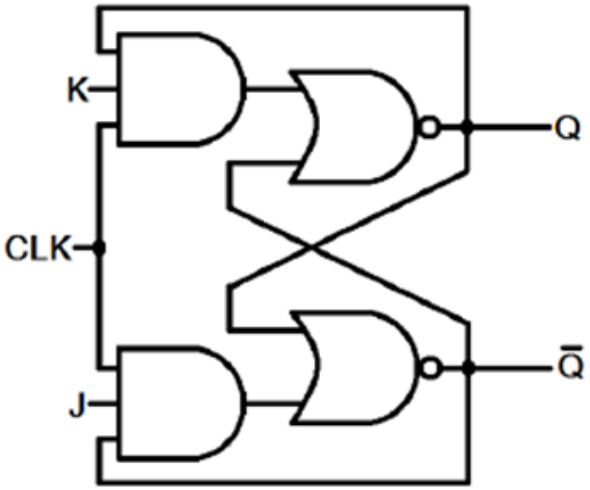
D Latch vs. D Flip-Flop

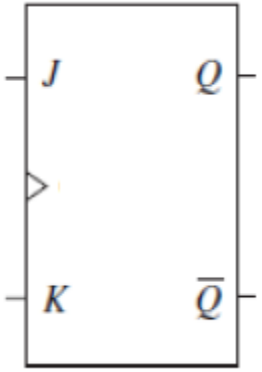




Level sensitive?
Edge sensitive?

JK Flip-Flops

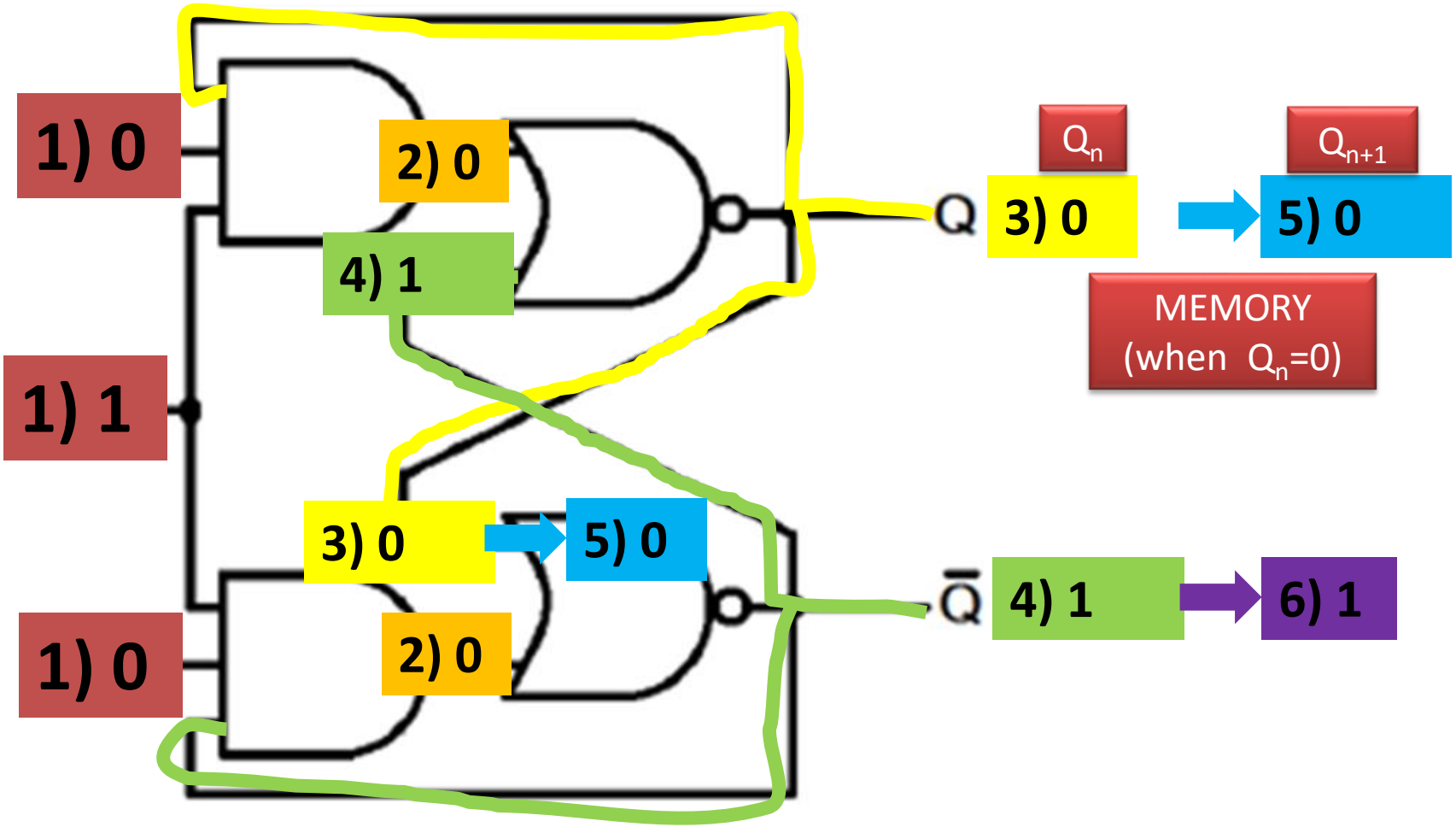




J	K	Q_{n+1}
0	0	Memory, Set, Reset, Toggle
0	1	
1	0	
1	1	

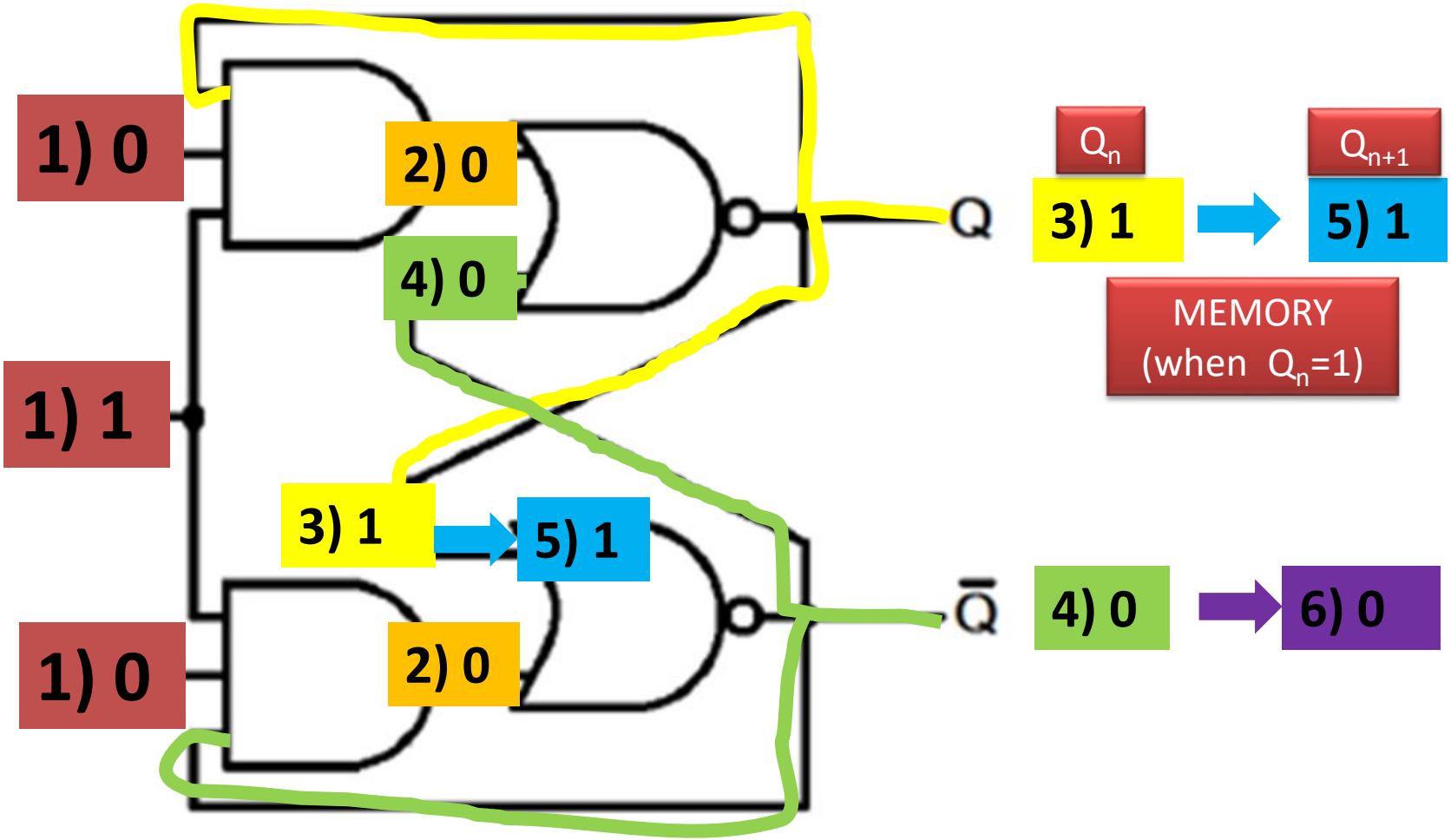
		NOR
0	0	1
0	1	0
1	0	0
1	1	0

J=0, K=0 (case I:Q=0)



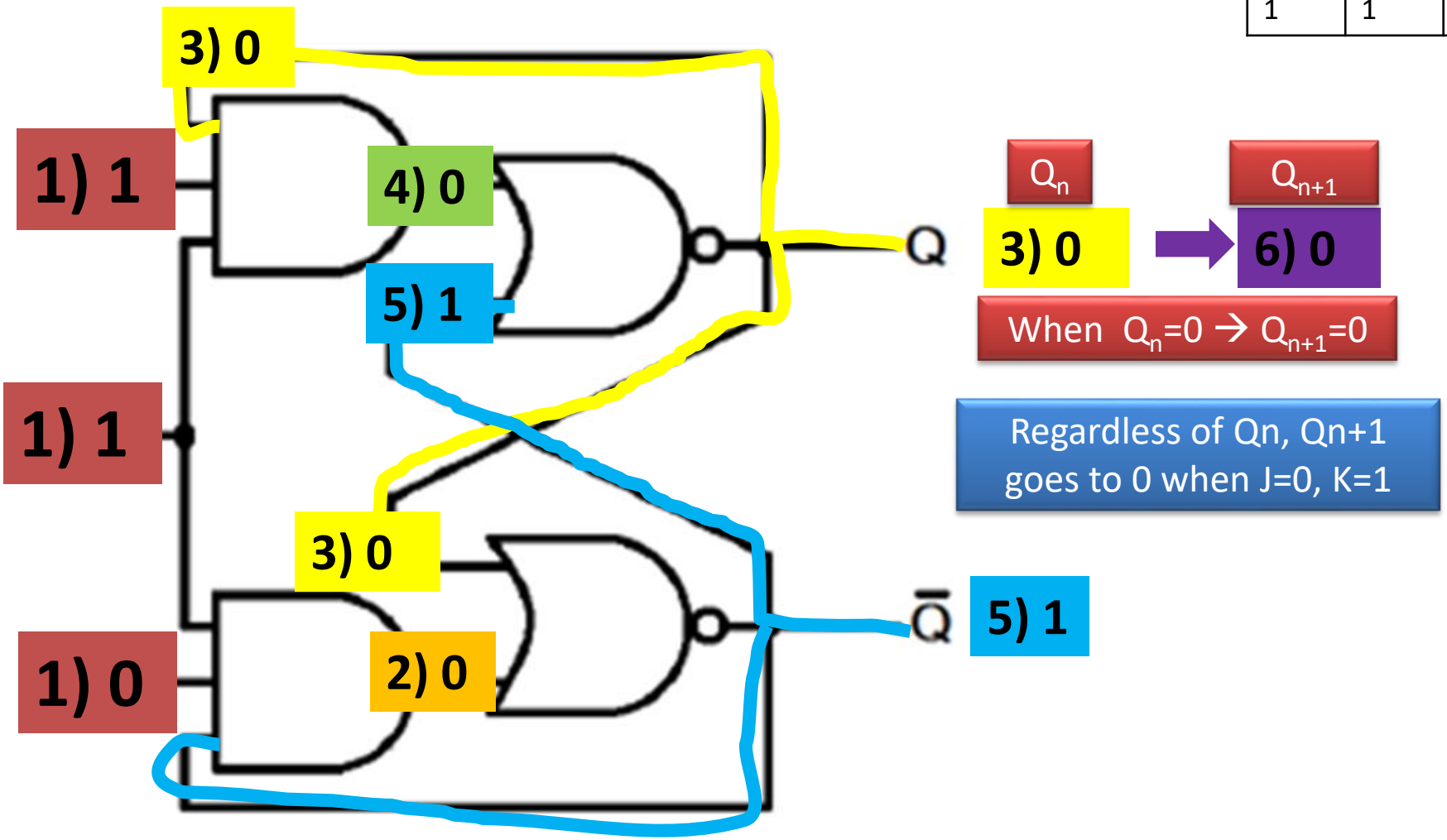
J=0, K=0 (case II:Q=1)

		NOR
0	0	1
0	1	0
1	0	0
1	1	0



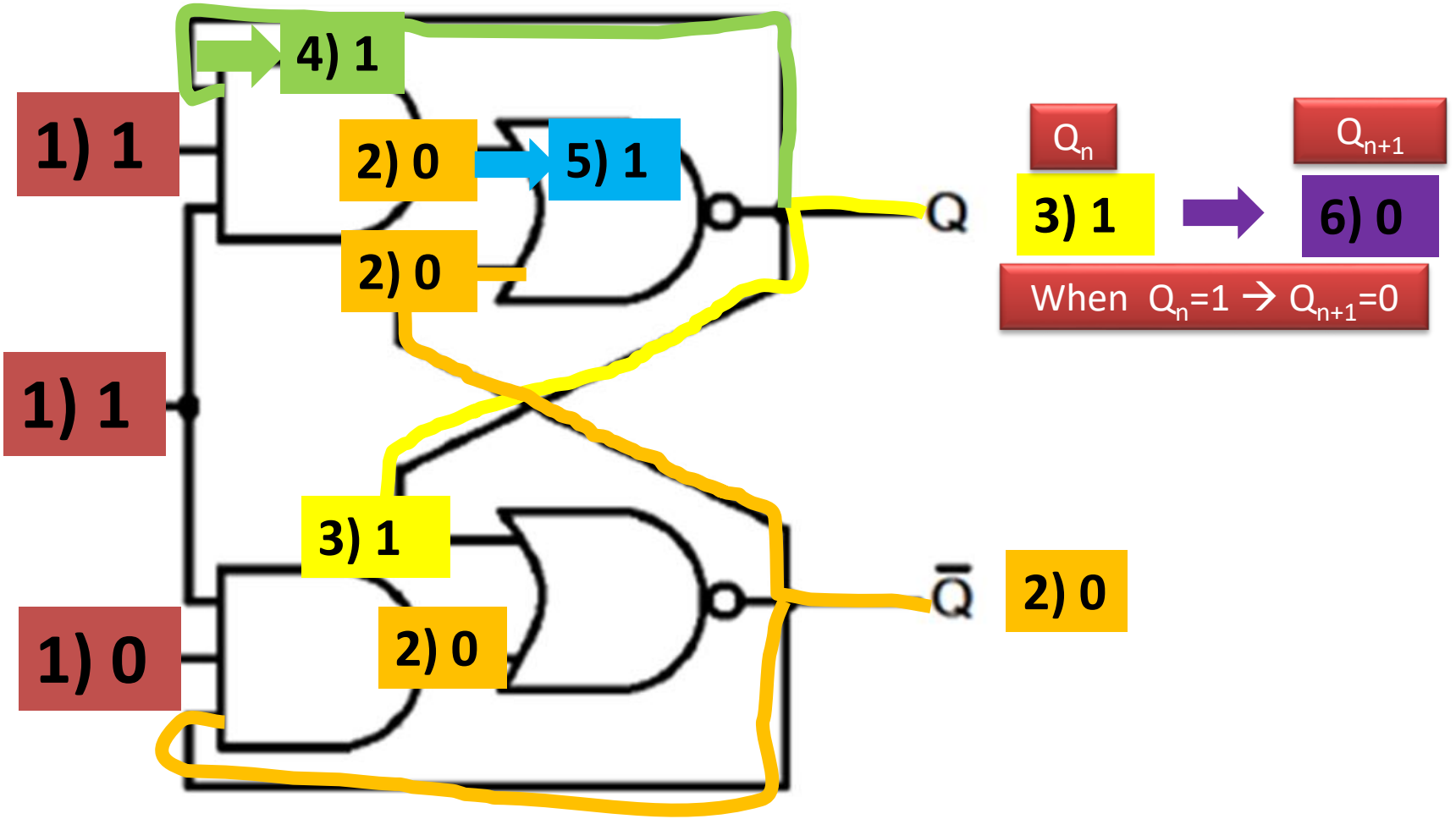
J=0, K=1 (Case I:Q=0)

		NOR
0	0	1
0	1	0
1	0	0
1	1	0



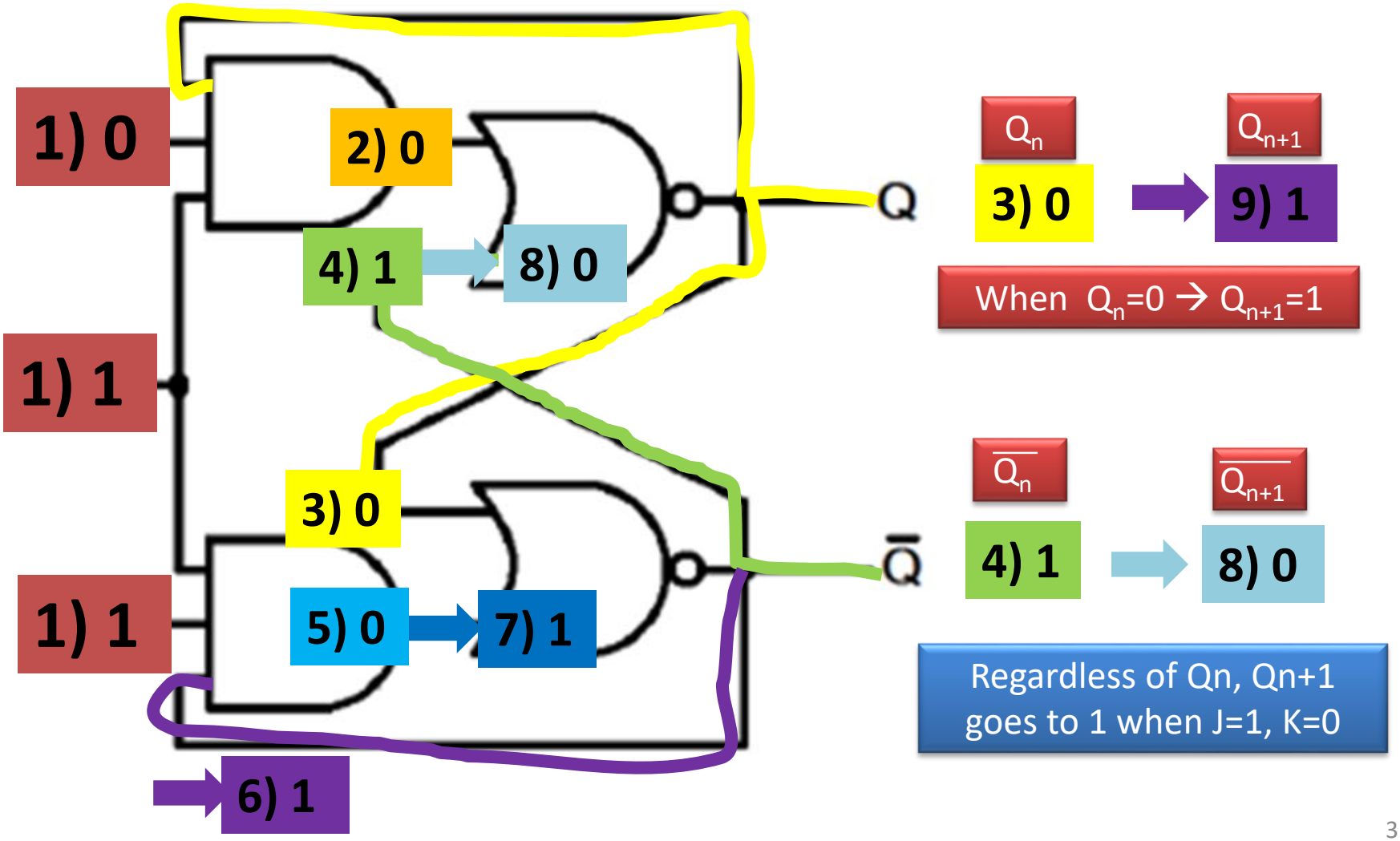
J=0, K=1 (Case II:Q=1)

		NOR
0	0	1
0	1	0
1	0	0
1	1	0



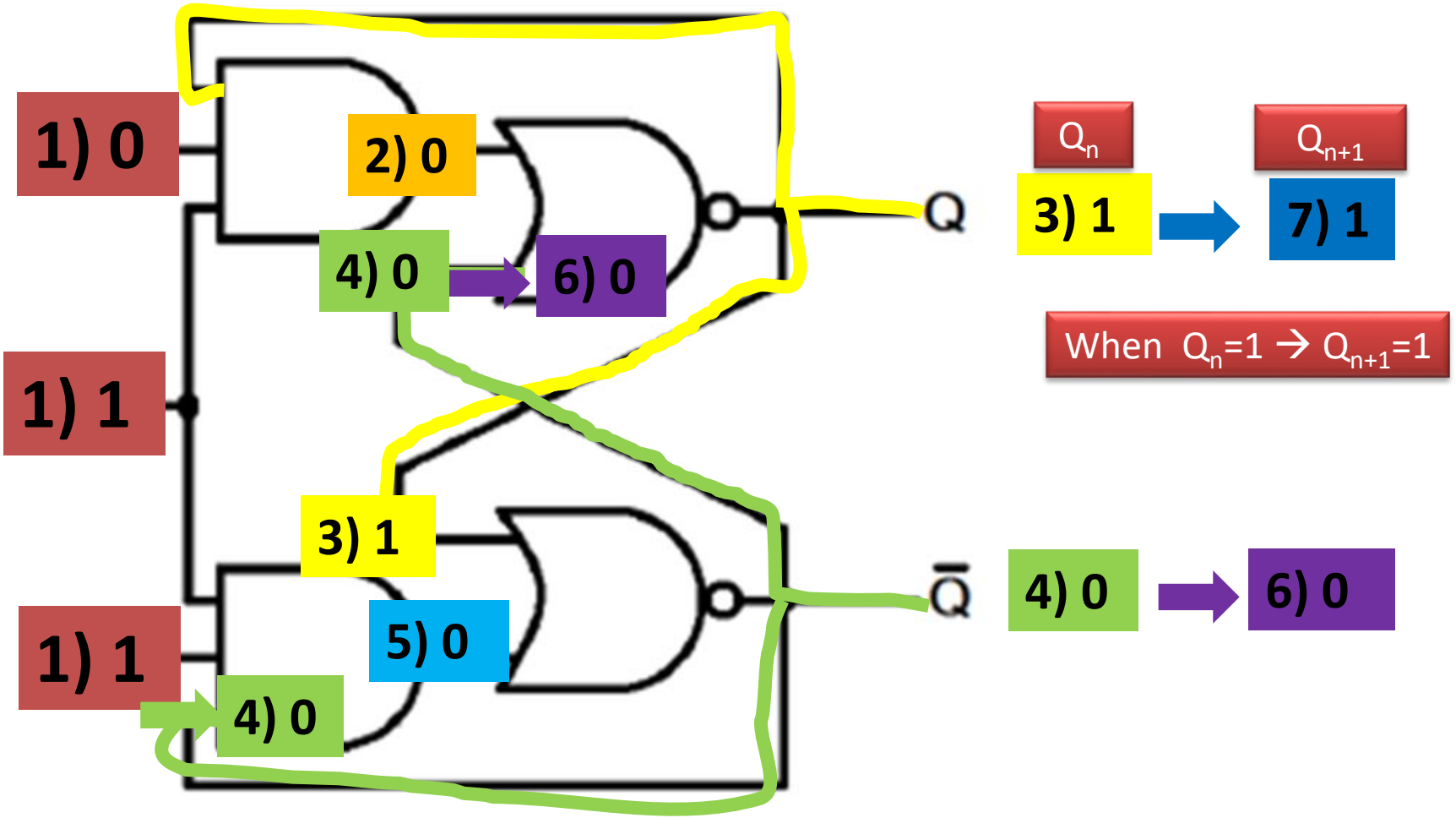
J=1, K=0 (Case I: Q=0)

		NOR
0	0	1
0	1	0
1	0	0
1	1	0



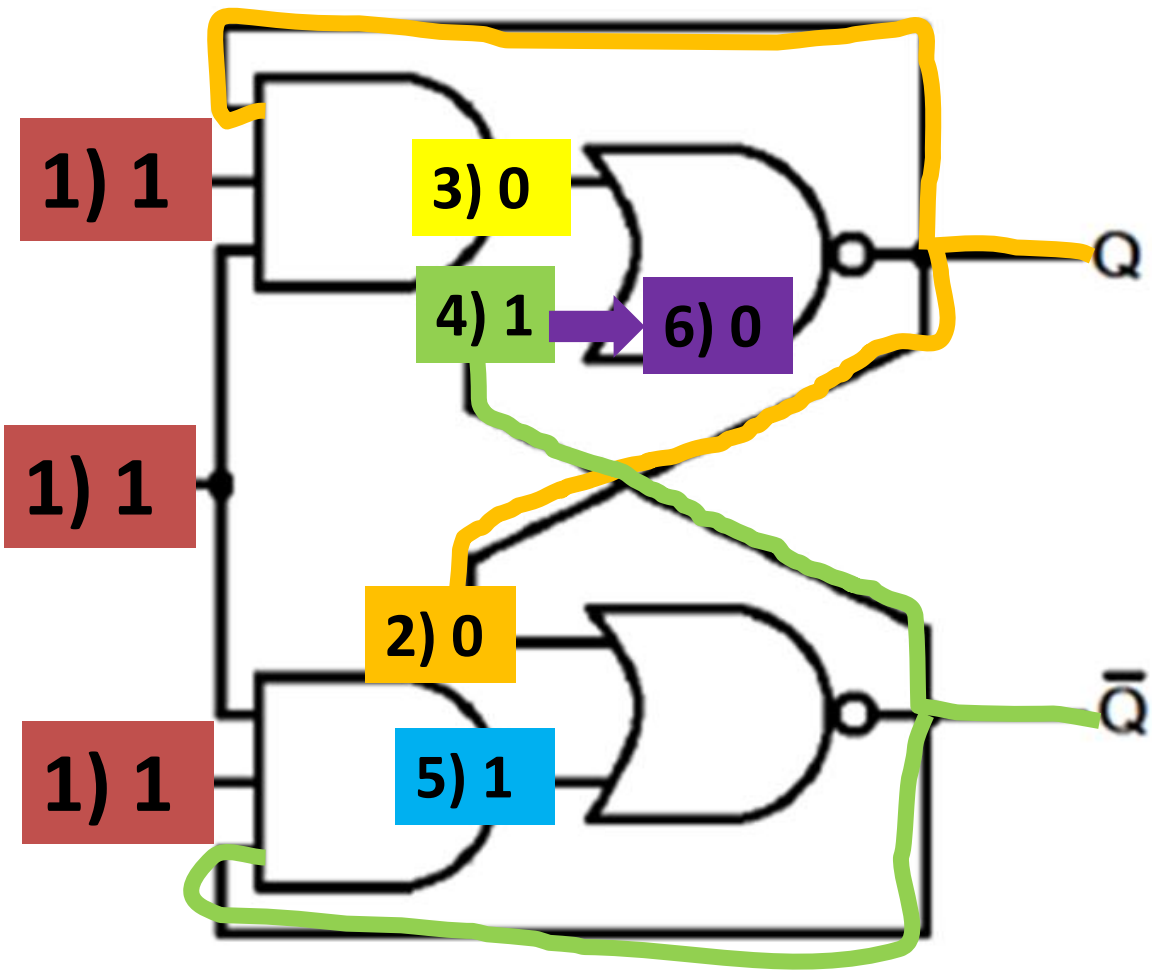
J=1, K=0 (Case II:Q=1)

		NOR
0	0	1
0	1	0
1	0	0
1	1	0



J=1, K=1 (Case I: Q=0)

		NOR
0	0	1
0	1	0
1	0	0
1	1	0



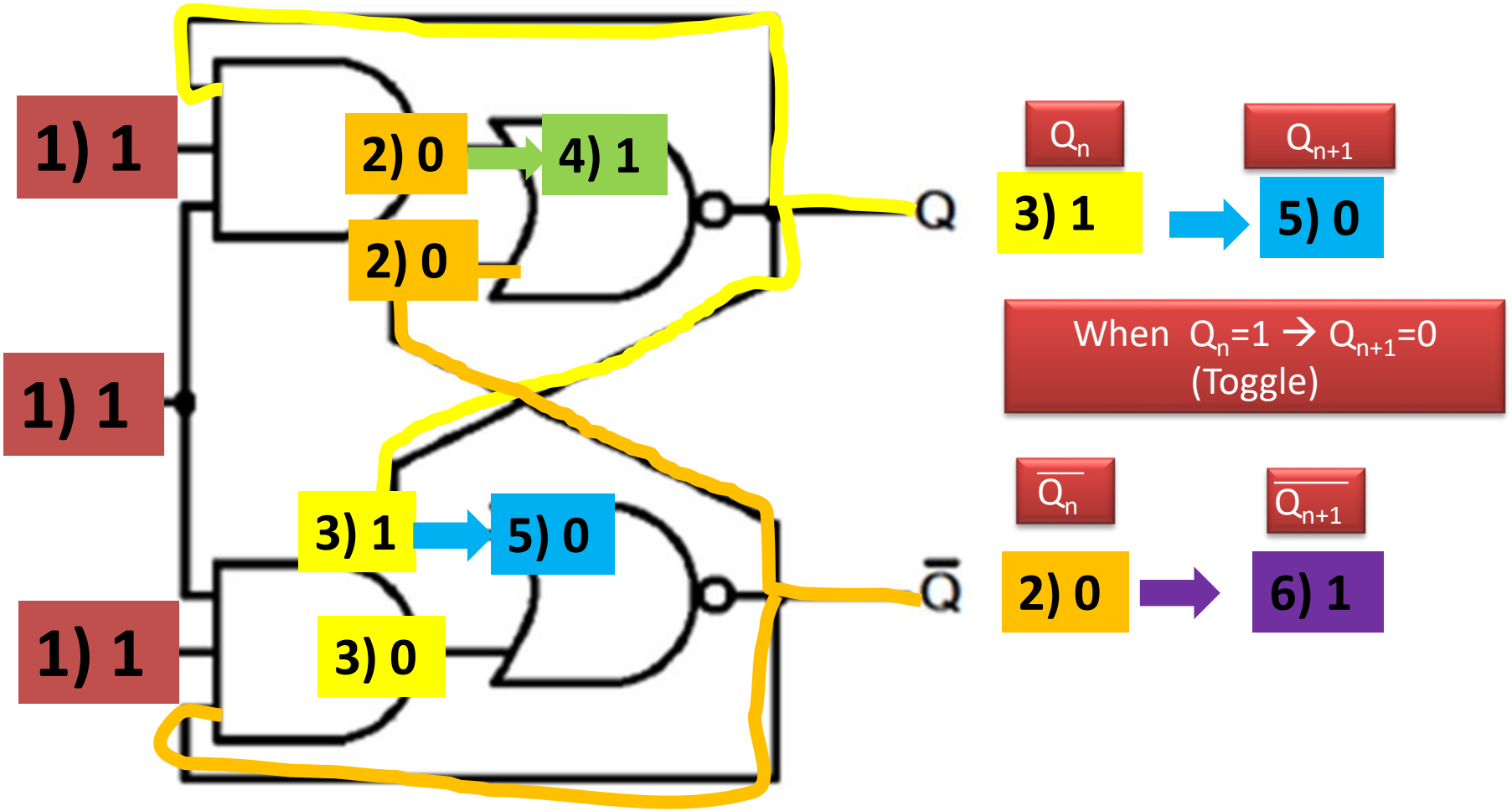
Q_n 2) 0 → Q_{n+1} 7) 1

When $Q_n=0 \rightarrow Q_{n+1}=1$ (Toggle)

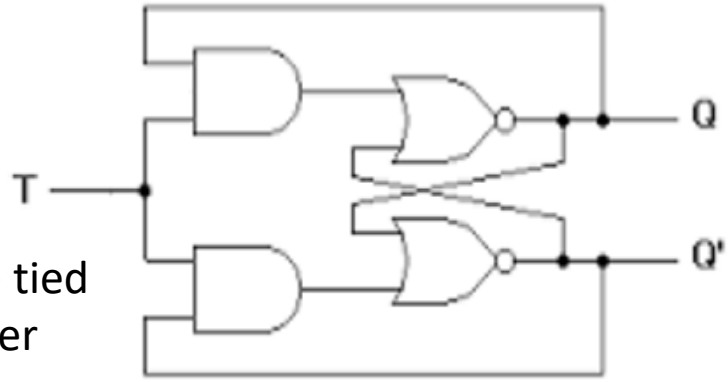
$\overline{Q_n}$ 4) 1 → $\overline{Q_{n+1}}$ 6) 0

J=1, K=1 (Case II:Q=1)

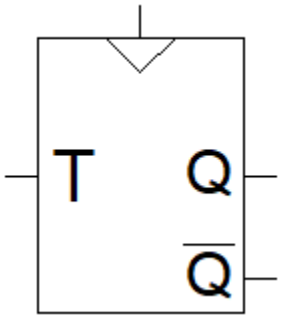
		NOR
0	0	1
0	1	0
1	0	0
1	1	0



T Flip-Flops



J/K are tied together



CLK	T	Q_{n+1}
1	0	Memory, Toggle
1	1	

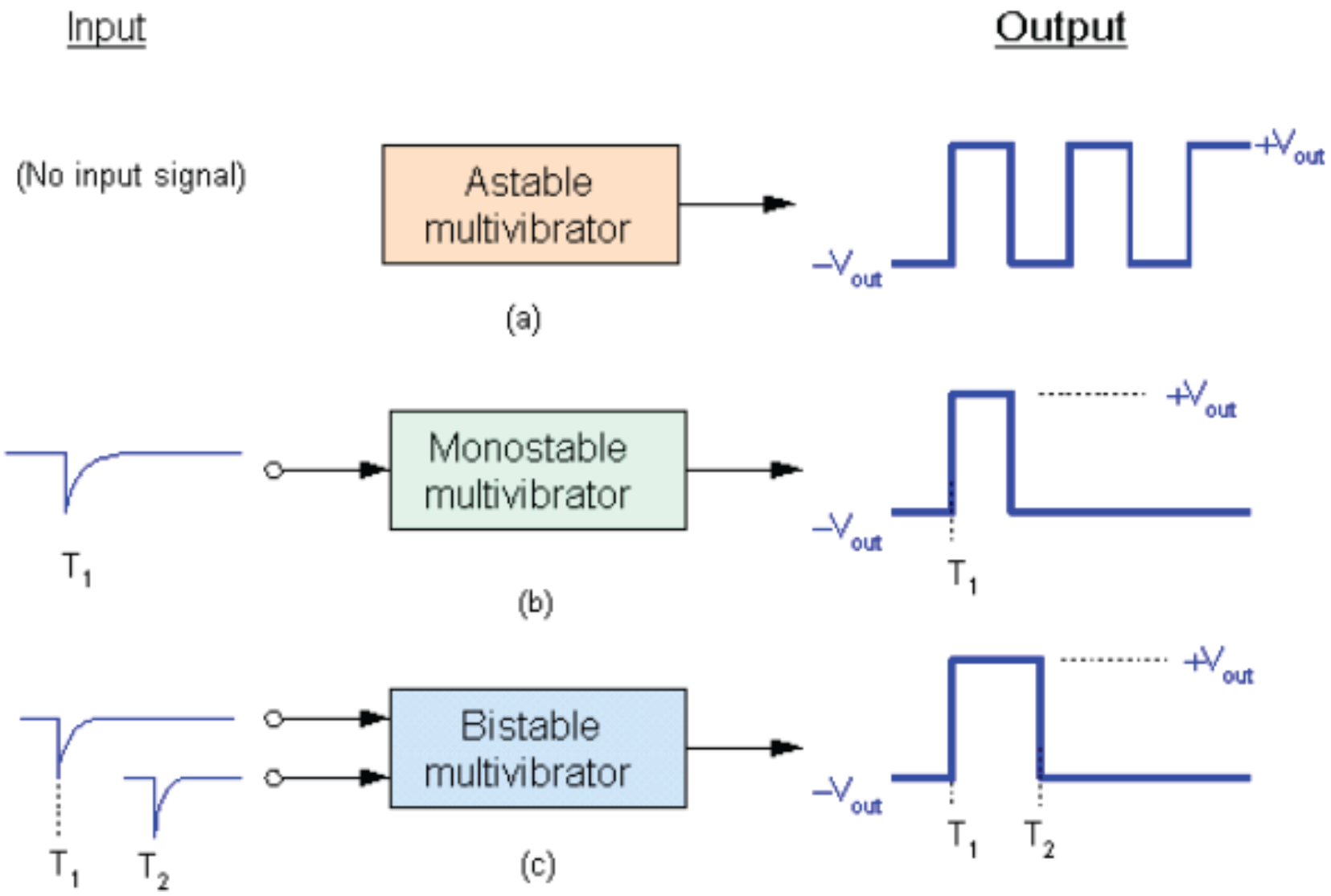
SR Latch -> D Latch

2 * D Latch -> D FF

JK FF -> T FF

Multivibrators

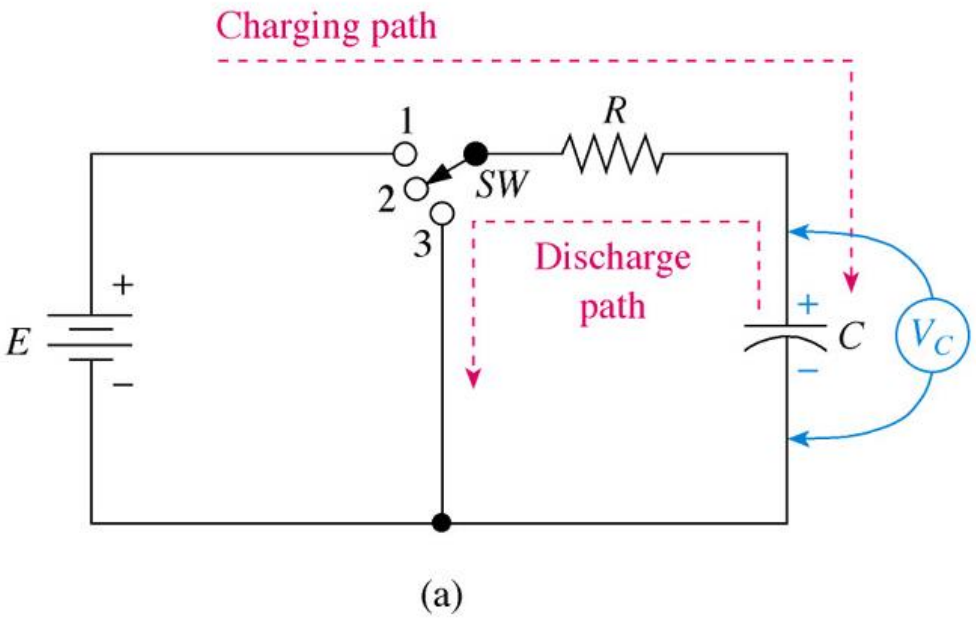
- Change between two digital levels
  - Continuous (free-running)
  - On demand from an external trigger
- Three types:
  1. **Astable (free running): constantly changing states**
  2. **Monostable (one shot): single output for a specific length of time**
  3. Bistable: changes states when triggered and holds state until next trigger


Input
Output
(No input signal)
Astable multivibrator
+Vout
-Vout
(a)
Monostable multivibrator
T1
(b)
Bistable multivibrator
T1
T2
(c)

We need RC charging/discharging knowledge to understand the multi-vibration

Capacitor Charge and Discharge

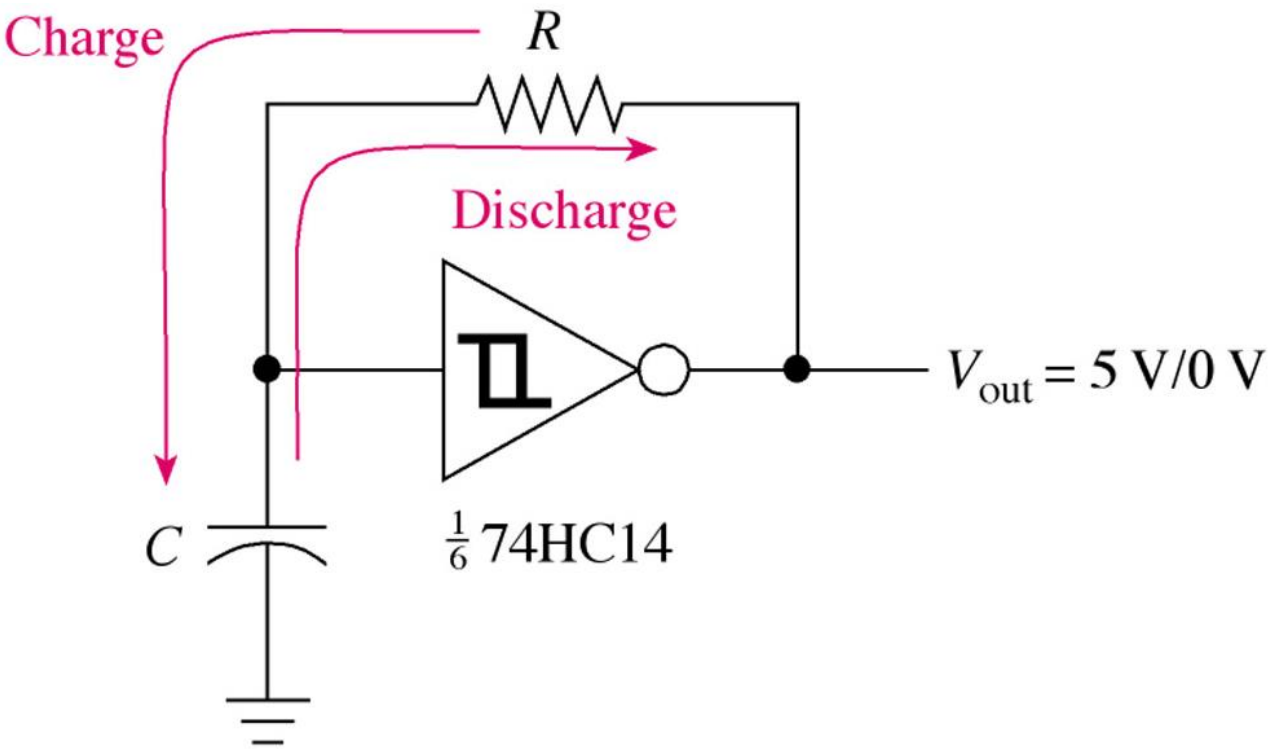
- RC circuit charge and discharge curves



(a)

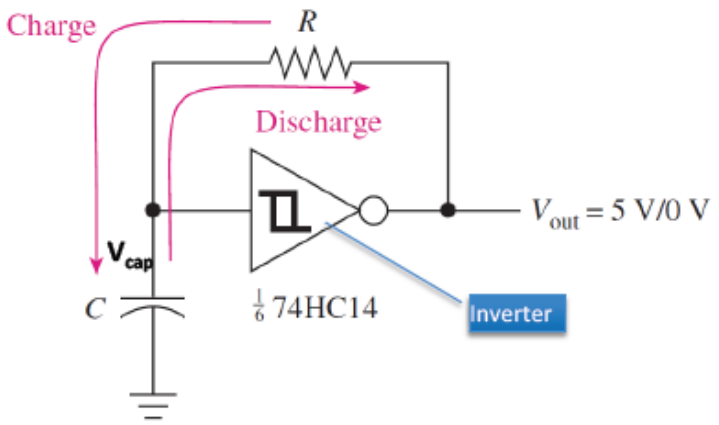
1. Astable Multivibrators (free-run)

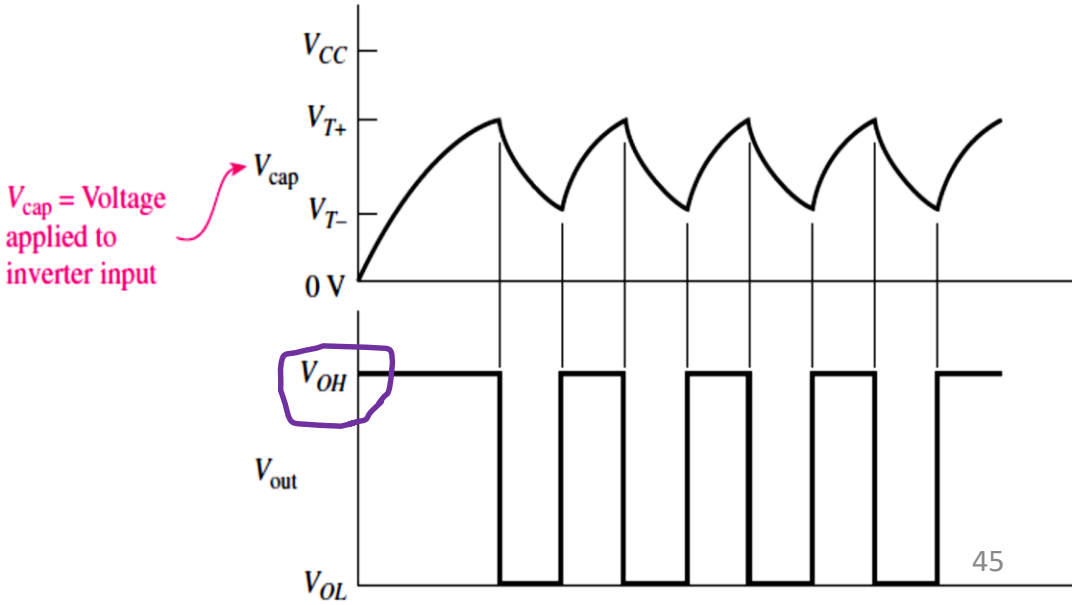
- A Schmitt Inverter and an RC circuit produces a simple astable multivibrator
- We will study waveforms from **Schmitt inverter-based oscillator**; Free-run or auto-run



- The Schmitt trigger was invented by American scientist Otto H. Schmitt in 1934 while he was a graduate student, later described in his doctoral dissertation (1937) as a "thermionic trigger.“ It was a direct result of Schmitt's study of the neural impulse propagation in squid nerves. [wiki]

1) When the IC supply power is first turned on, V_{cap} is 0V, so V_{out} will be HIGH (inverter)
2) The capacitor will start charging toward the 5V at V_{out}
3) When V_{cap} reaches the *positive-going threshold (V_{T+})* of the Schmitt trigger, the output of the trigger will change to a LOW
4) When V_{out} is near 0V, the capacitor will start discharging.
5) When V_{cap} drops below the *negative-going threshold (V_{T-})*, the output of the Schmitt will change back to a HIGH and repeat the cycle

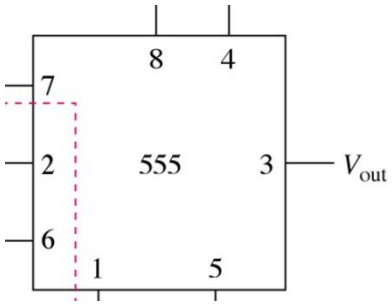




555 Timer Astable Multivibrator implementation

- 555 timer: Very popular general-purpose IC
  - Can be used as a one shot or astable oscillator
  - Also custom designs

555 IC Timer Pin Functions



The operation and function of the 555 pins are as follows:

Pin 1 (ground): System ground.

Pin 2 (trigger): Input to the lower comparator, which is used to Set the flip-flop. When the voltage at pin 2 crosses from above to below $\frac{1}{3}V_{CC}$, the comparator switches to a HIGH, setting the flip-flop.

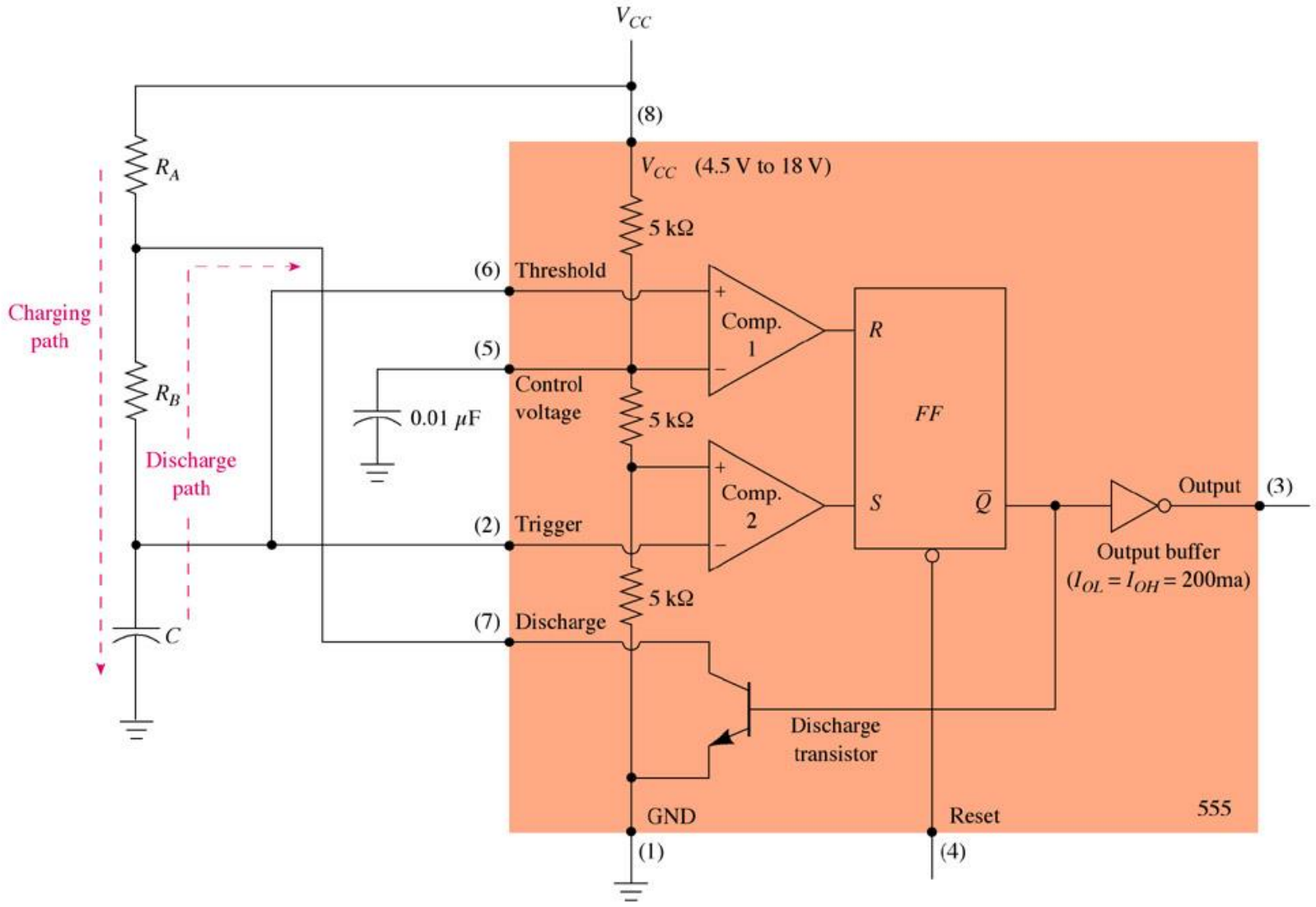
Pin 3 (output): The output of the 555 is driven by an inverting buffer capable of sinking or sourcing 200 mA. The output voltage levels are dependent on the output current but are approximately $V_{OH} = V_{CC} - 1.5\,V$ and $V_{OL} = 0.1\,V$.

Pin 4 (Reset): Active-LOW Reset, which forces $\overline{Q}$ HIGH and pin 3 (output) LOW.

Pin 5 (control): Used to override the $\frac{2}{3}V_{CC}$ level, if required. Usually, it is connected to a grounded 0.01-μF capacitor to bypass noise on the V_{CC} line.

Pin 6 (threshold):	Input to the upper comparator, which is used to Reset the flip-flop. When the voltage at pin 6 crosses from below to above $\frac{2}{3}V_{CC}$, the comparator switches to a HIGH, resetting the flip-flop.
Pin 7 (discharge):	Connected to the open collector of the *NPN* transistor. It is used to short pin 7 to ground when $\overline{Q}$ is HIGH (pin 3 LOW), which will discharge the external capacitor.
Pin 8 (V_{CC}):	Supply voltage. V_{CC} can range from 4.5 to 18 V.

Astable 555 IC Timer Block Diagram

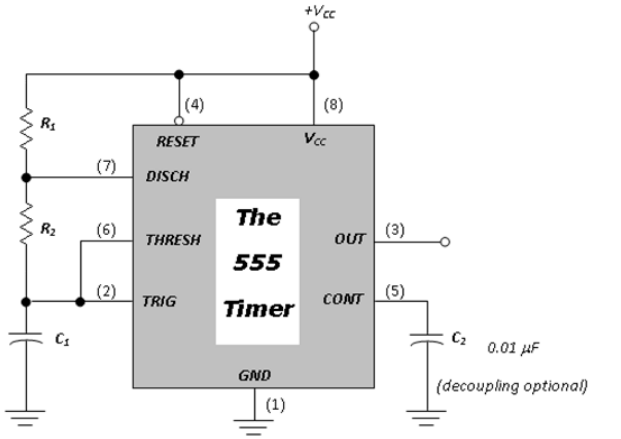


As we are learning this chip (555timer), we have to learn how this chip works

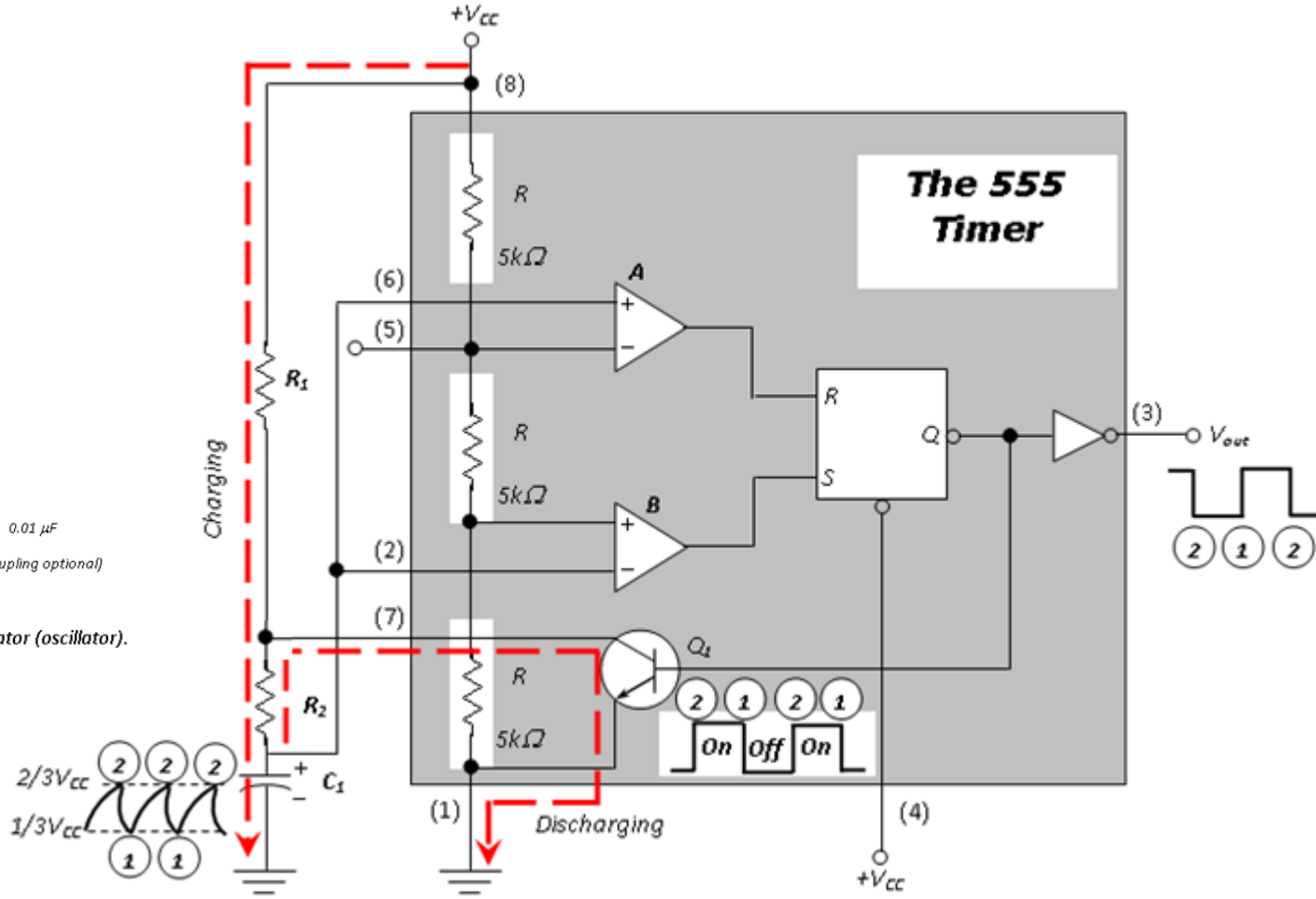
This chip basically consists of 5 components

- 3 internal 5k resistors (555?)
- Two comparators
- One SR flip-flop
- One transistor (BJT- Source/Drain/Gate: on-off is determined by voltage between S and G)
- One inverter

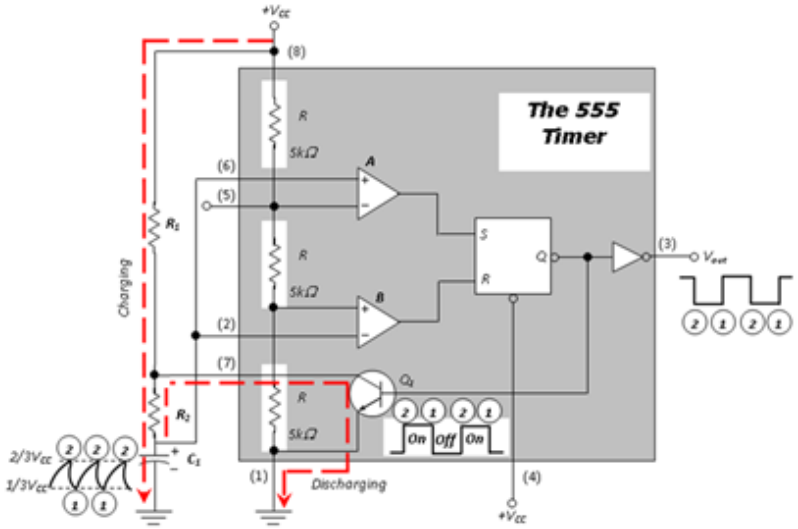
555 timer



The 555 timer connected as an astable multivibrator (oscillator).



Looks very complicated!



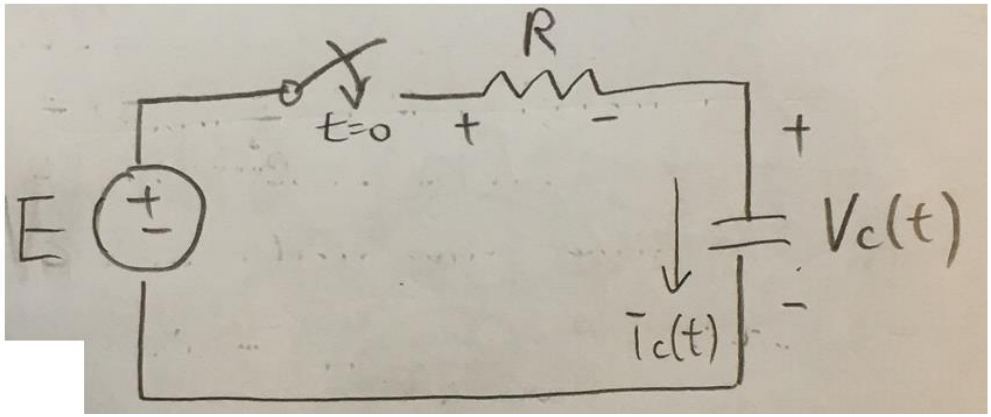
To understand this system fully, you will need the following knowledge (background)

1. Capacitor charging/ discharging circuits
2. How a comparator works?
3. SR Flip-flop/Latch (truth table)
4. How a transistor works? How can we turn it on?

Based on all of the above, you should be able to analyze the 555 internal circuits. Timing graphs/truth table for the voltage across the capacitor ($V_c(t)$), Q, and Vout

1. Capacitor charging/ discharging circuits

- A capacitor (a cap)→ capacitance C
  - The current through the cap: $i_c(t) = \mathrm{C}\frac{d}{dt}v_C(t)$
- A capacitor charging circuit



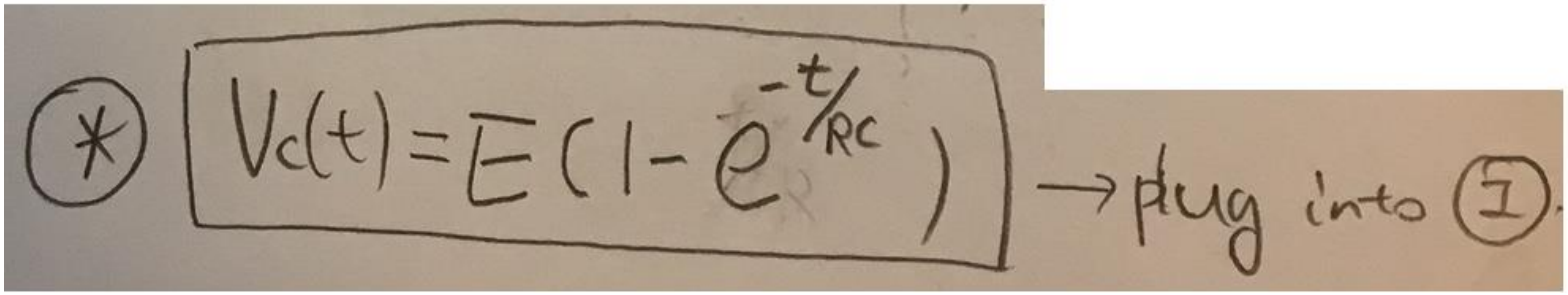
Voltage across R

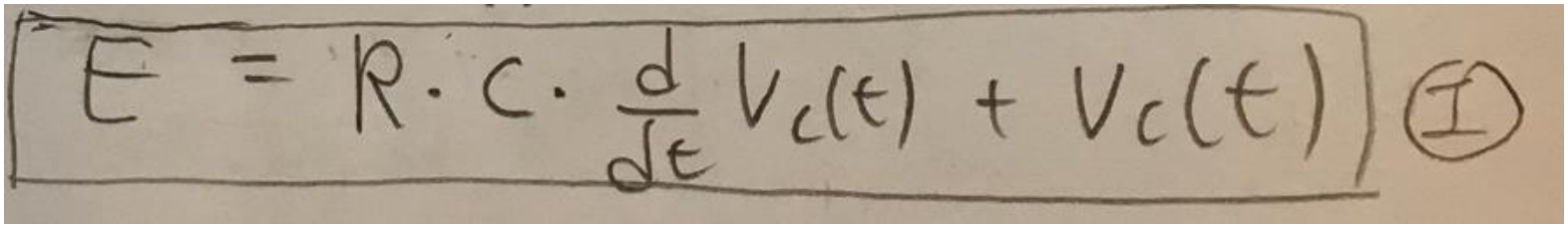
$$E = R \cdot I_c(t) + V_c(t)$$

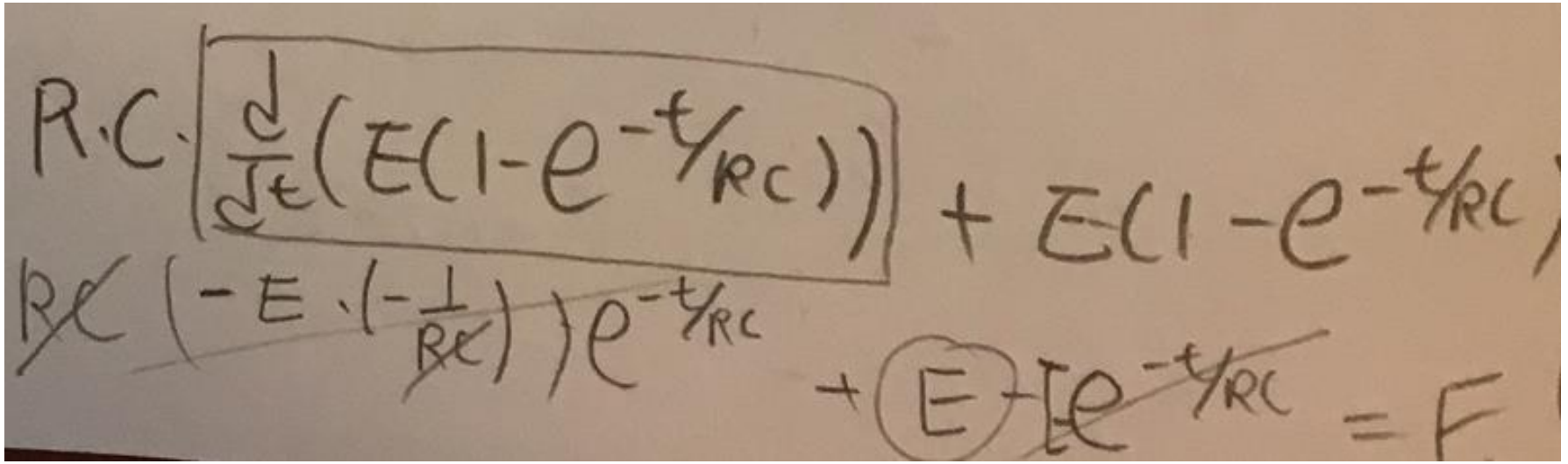
$$E = R \cdot C \cdot \frac{d}{dt} V_c(t) + V_c(t) \quad (I)$$

Solve for I means find $V_c(t)$

(*) $V_c(t) = E(1 - e^{-t/RC})$ → plug into (I).


(*) $V_c(t) = E(1 - e^{-t/RC})$ → plug into (I).

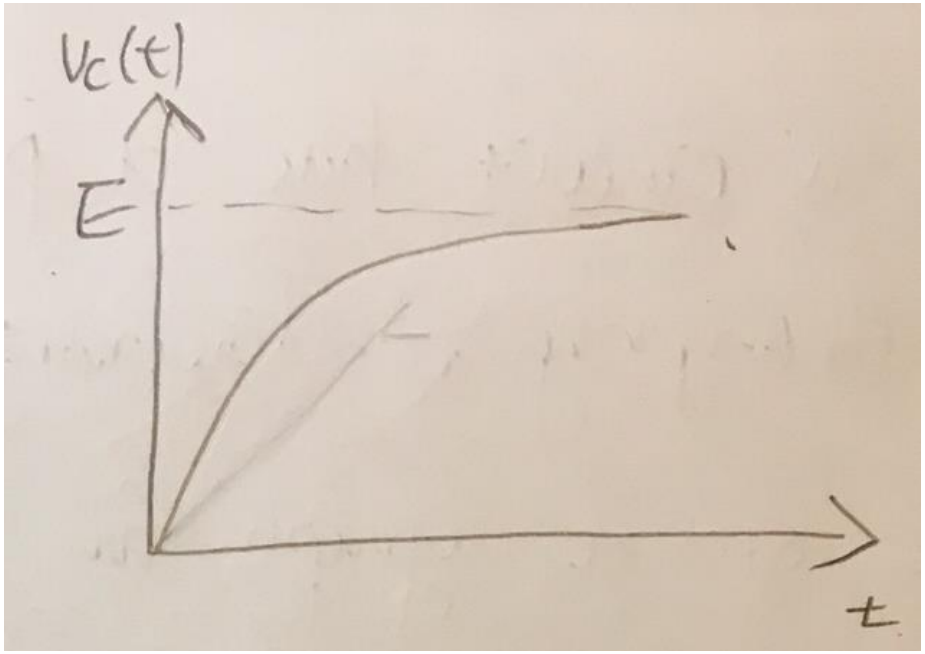

$E = R \cdot C \cdot \frac{d}{dt} V_c(t) + V_c(t)$ (I)

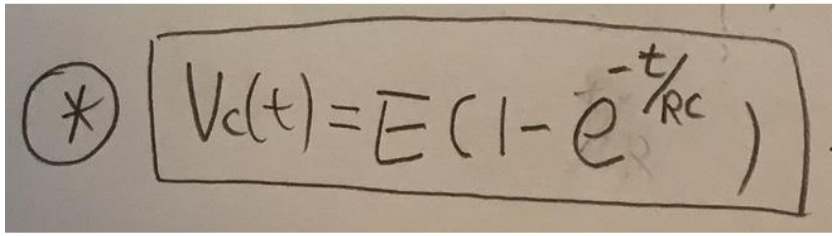

$R \cdot C \cdot \left[\frac{d}{dt}(E(1 - e^{-t/RC}))\right] + E(1 - e^{-t/RC})$
$RC\left(-E \cdot \left(-\frac{1}{RC}\right)\right)e^{-t/RC}$
$+ E - Ee^{-t/RC} = E$

Done.

- A graph for this case, assuming $V_c(0)=0$

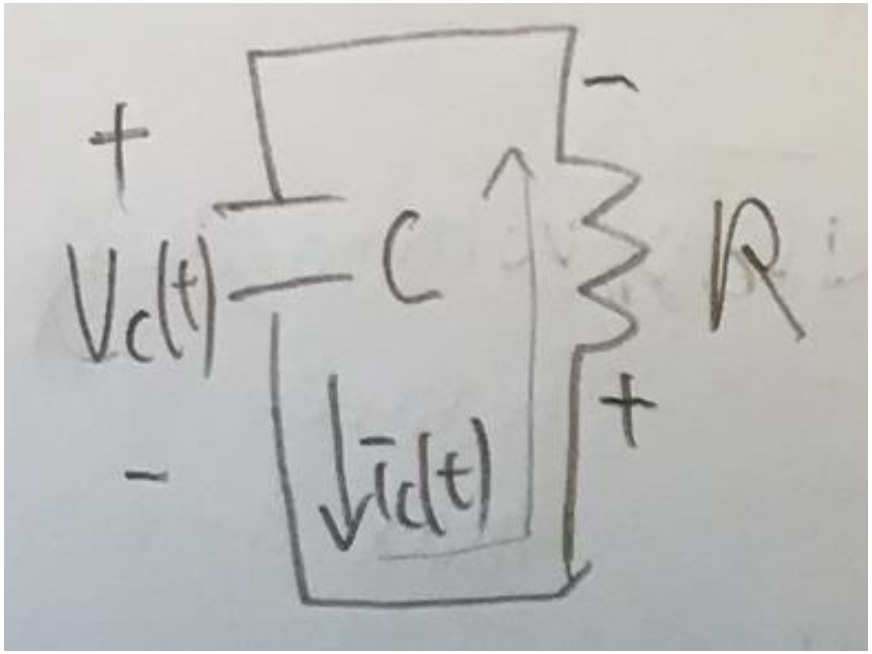
(means initially the cap was discharged)





Voltage across a charging capacitor

- A capacitor discharging circuit, $V_c(0)=E$
  - Means initially the cap was charged.



$$V_c(t) + R \cdot \bar{i}_c(t) = 0$$

$$V_c(t) + R \cdot C \cdot \frac{d}{dt} V_c(t) = 0 \quad \text{(II)}$$

Solve for II means find $V_c(t)$

$$\text{(*)} \quad V_c(t) = E \cdot e^{-t/CR}$$

Plug this into II to confirm the answer

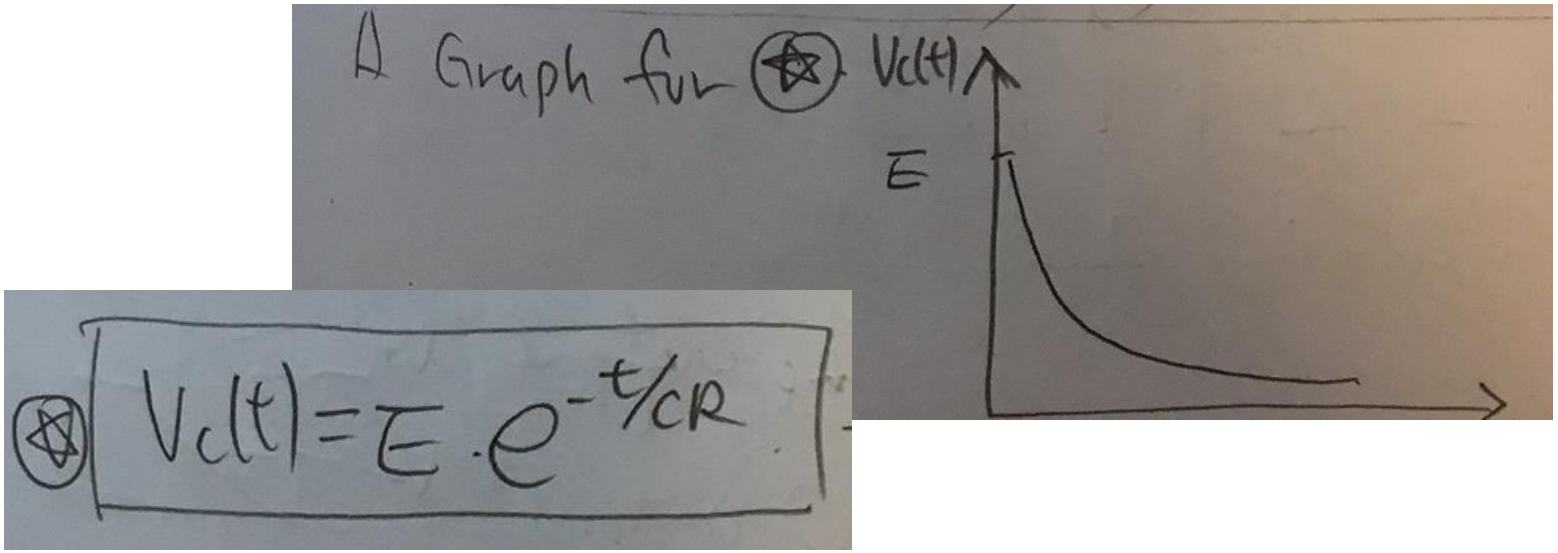
$$V_c(t) + R \cdot C \cdot \frac{d}{dt} V_c(t) = 0 \quad \text{(II)}$$

$$V_c(t) = E \cdot e^{-t/CR}$$

$$E \cdot e^{-t/CR} + R \cdot C \cdot \frac{d}{dt}\left(E \cdot e^{-t/CR}\right)$$

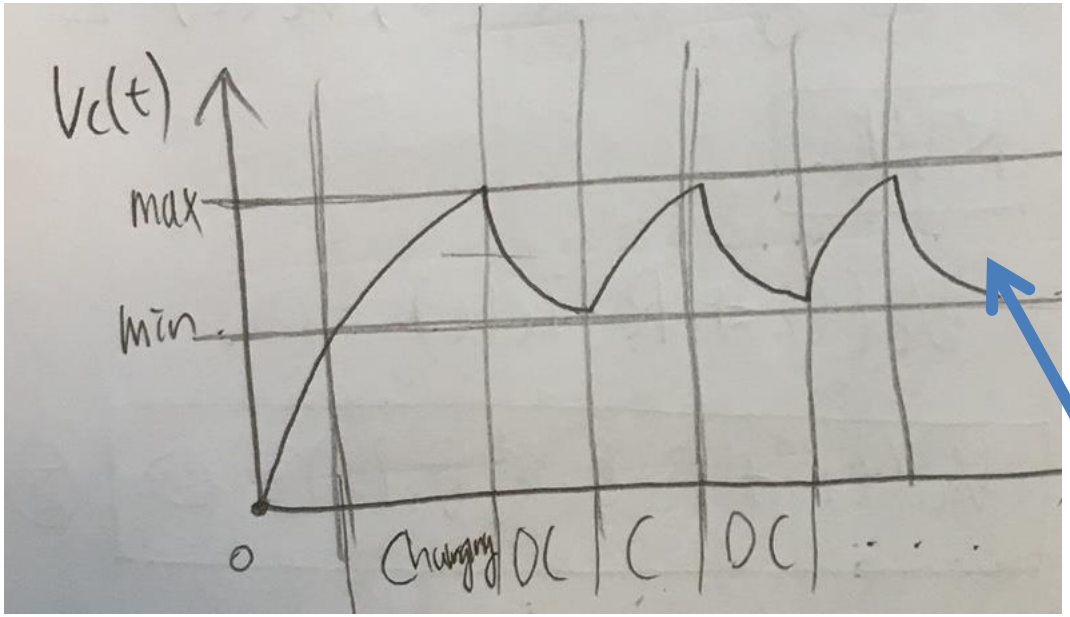
$$= E \cdot e^{-t/CR} + RC \cdot \frac{-1}{RC} \cdot E \cdot e^{-t/RC} = 0 \quad // \text{ proof } (V)$$

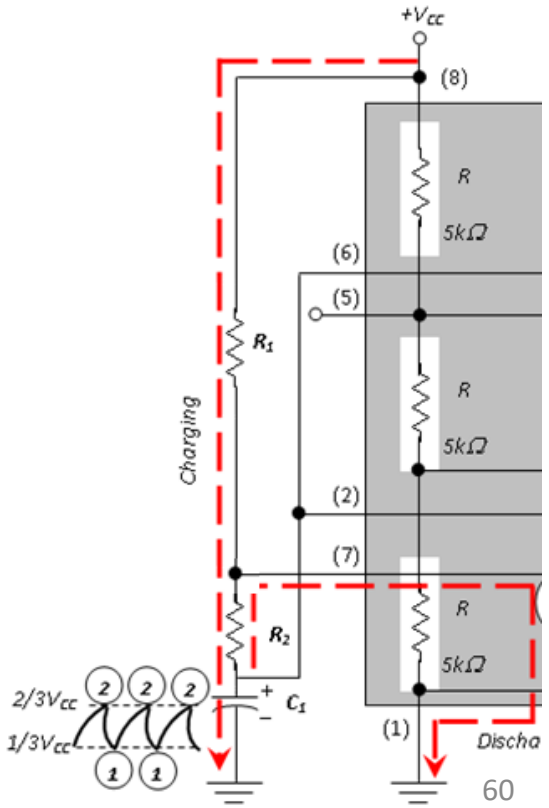
- A graph for this case (initially the cap was fully charged with E [V])

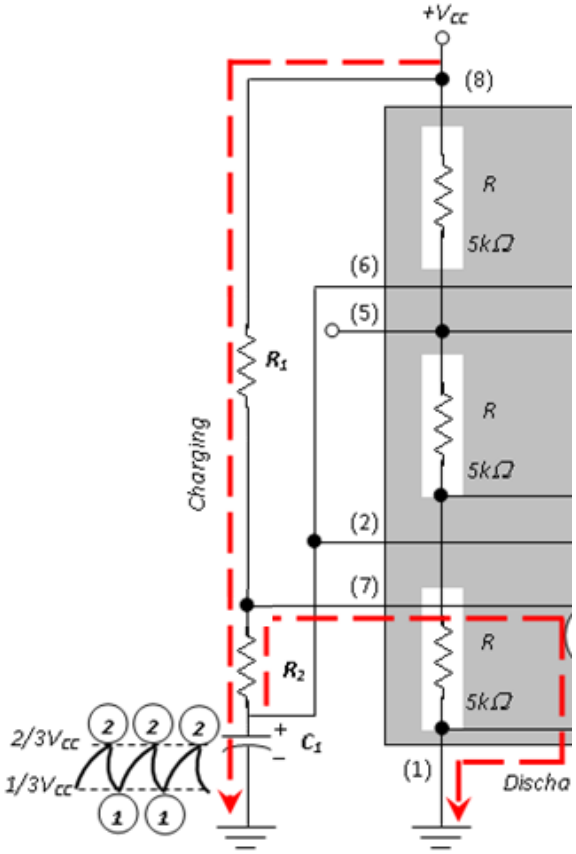


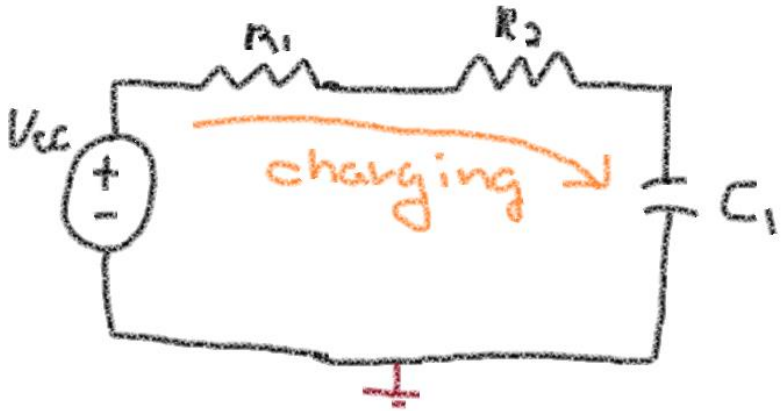
Voltage across a discharging capacitor

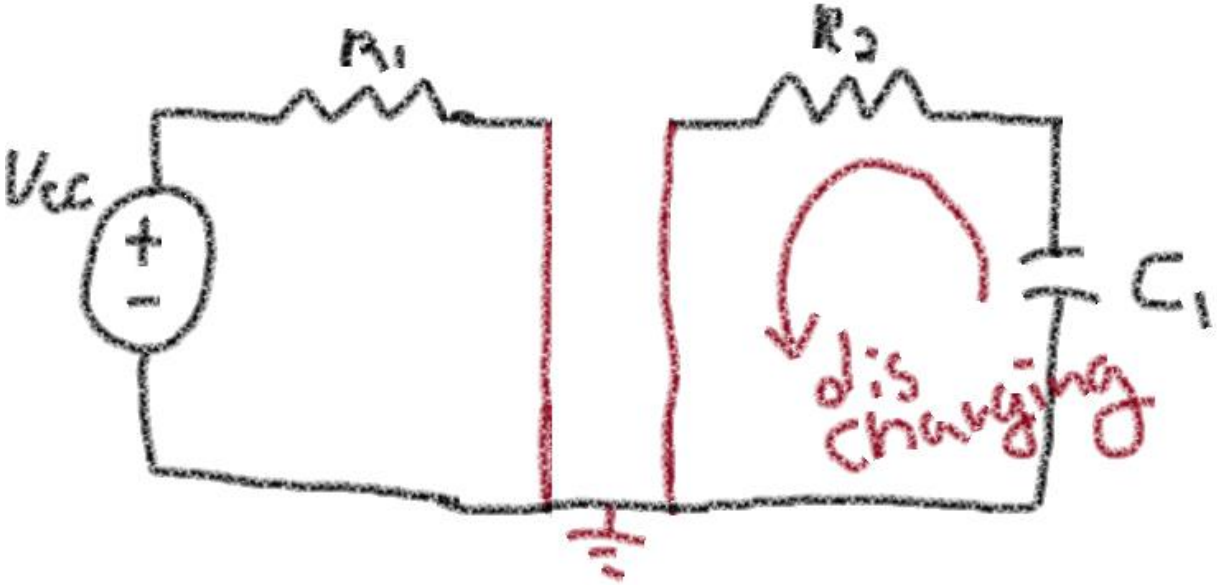
- If a circuit has a pattern (charging → discharging → charging → discharging….)
- $V_c(t)$ will look like this (assuming that it was discharged initially)





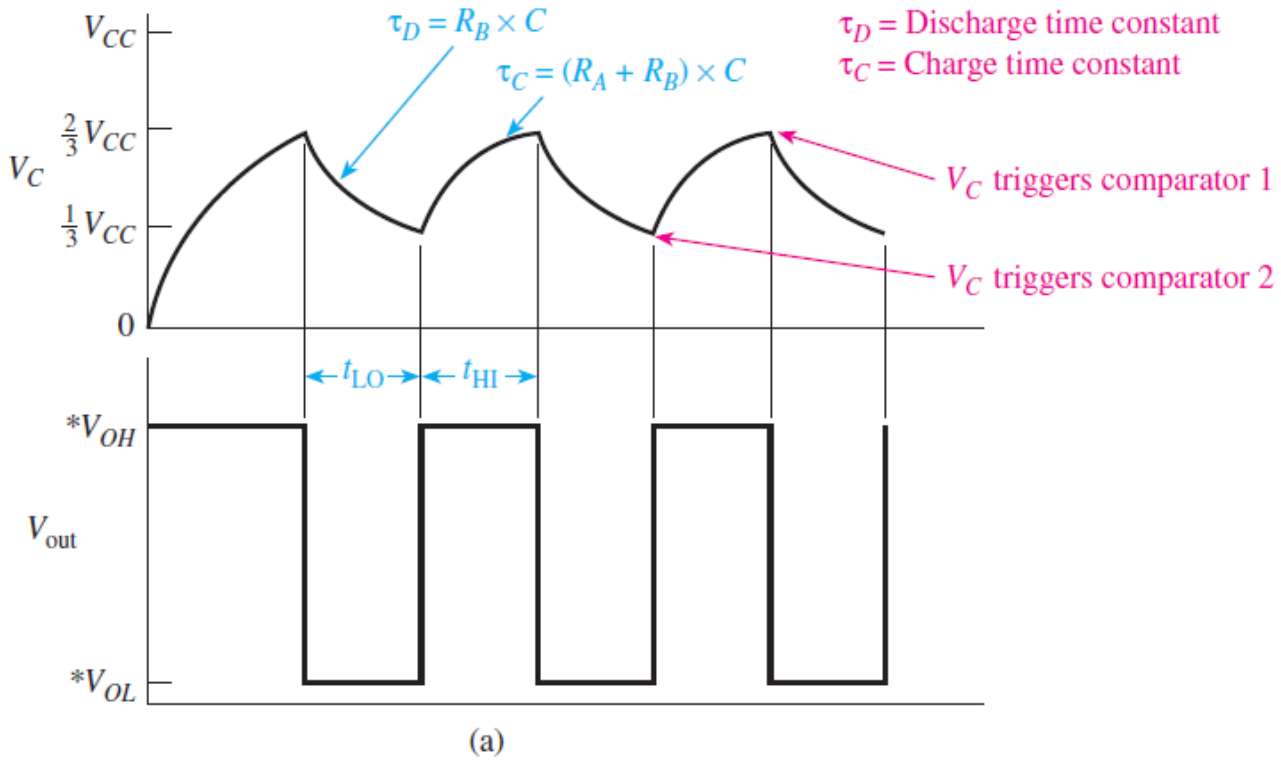

+Vcc
(8)
R
5kΩ
(6)
(5)
R1
R
5kΩ
Charging
(2)
(7)
R
5kΩ
R2
C1
2/3Vcc
1/3Vcc
(1)
Discha


R1
R2
Vcc
charging
C1

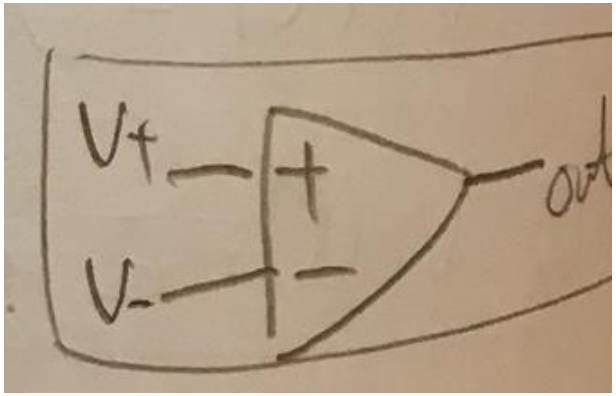

R1
R2
Vcc
C1
d:s
charging

555 Timer Astable Time Durations

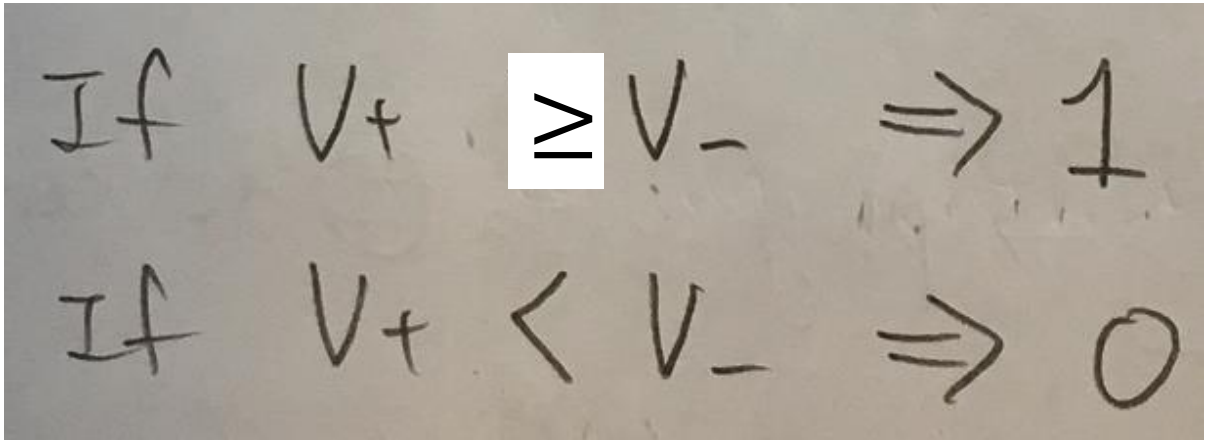
- $t_{LO} = 0.693R_BC$
- $t_{HI} = 0.693(R_A + R_B)C$



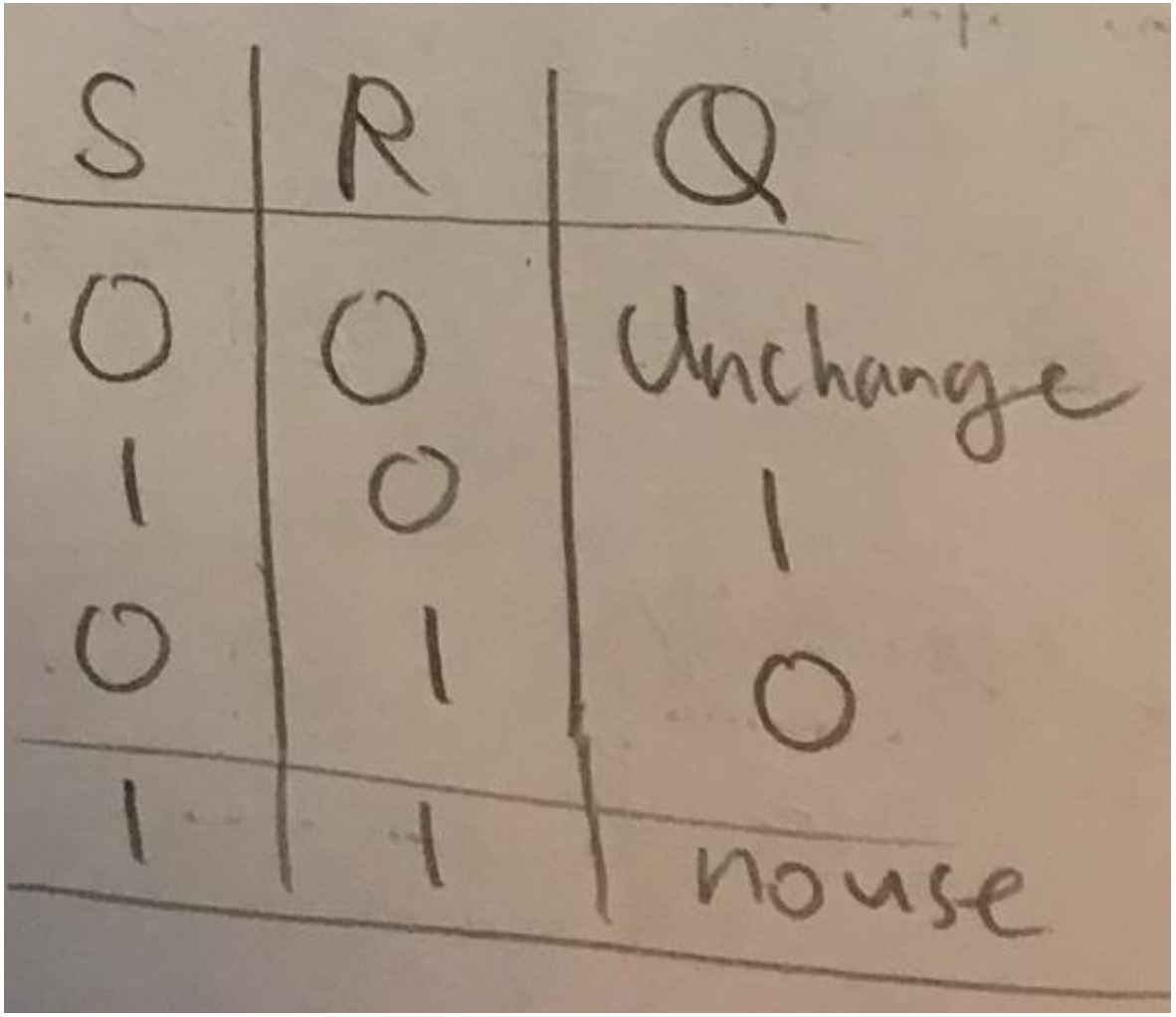
2. Comparators



Keep comparing V- and V+

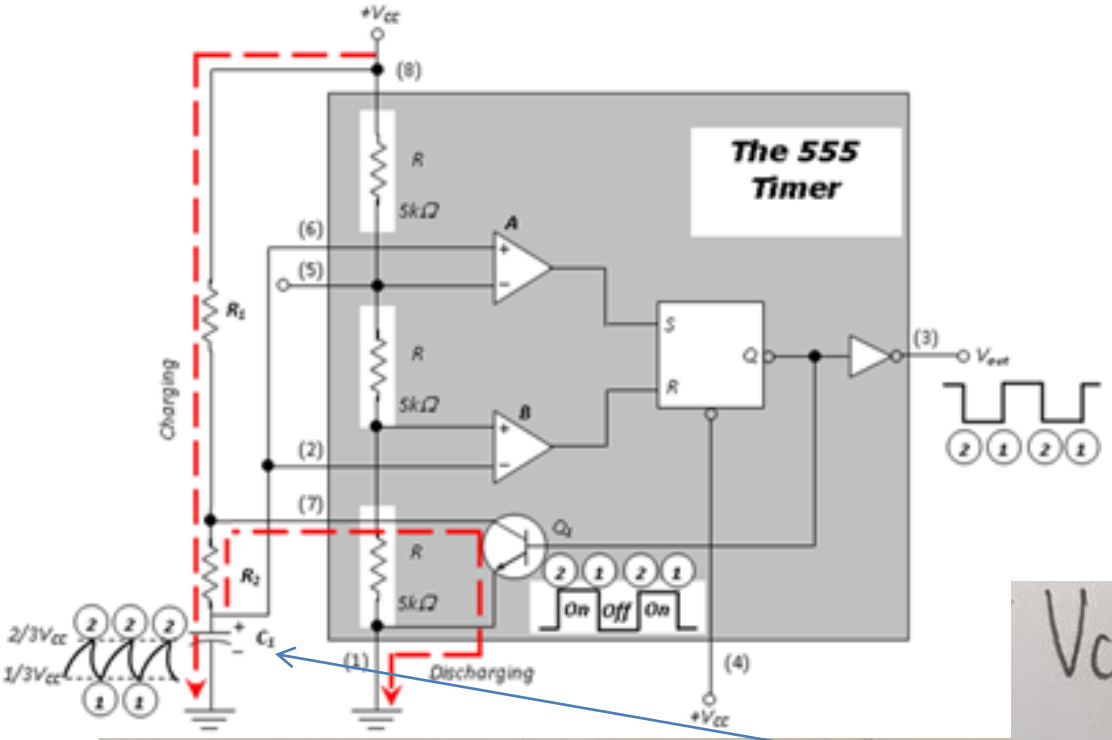


3. SR Latch

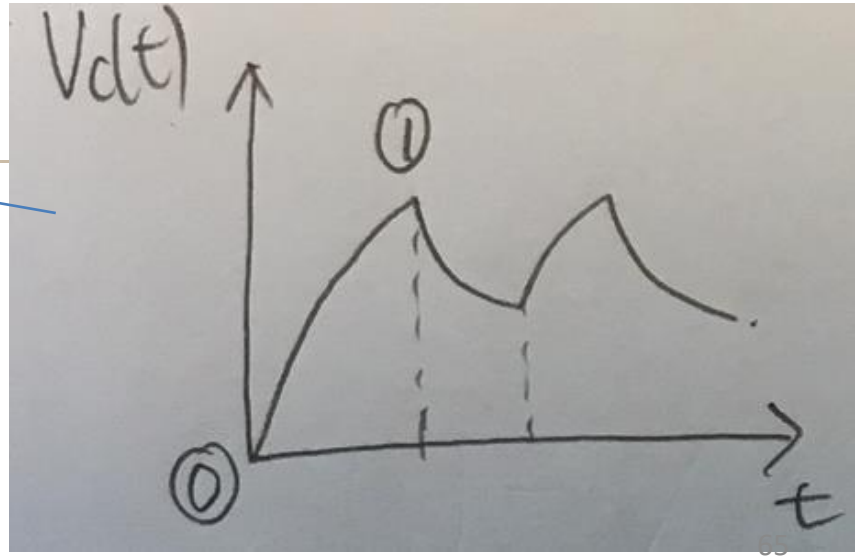


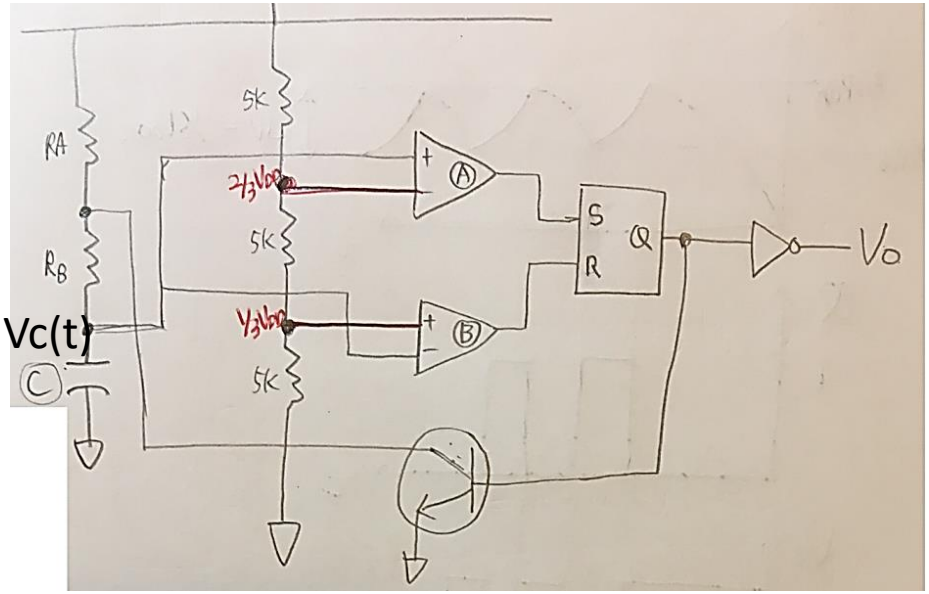
S	R	Q
0	0	Unchange
1	0	1
0	1	0
1	1	nouse

555 timer circuits



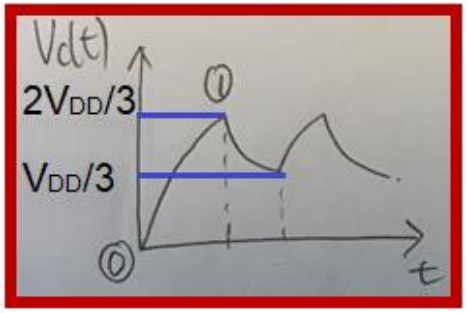
Let's investigate the path 0→1
The cap was initially discharged
$V_c(0)=0$





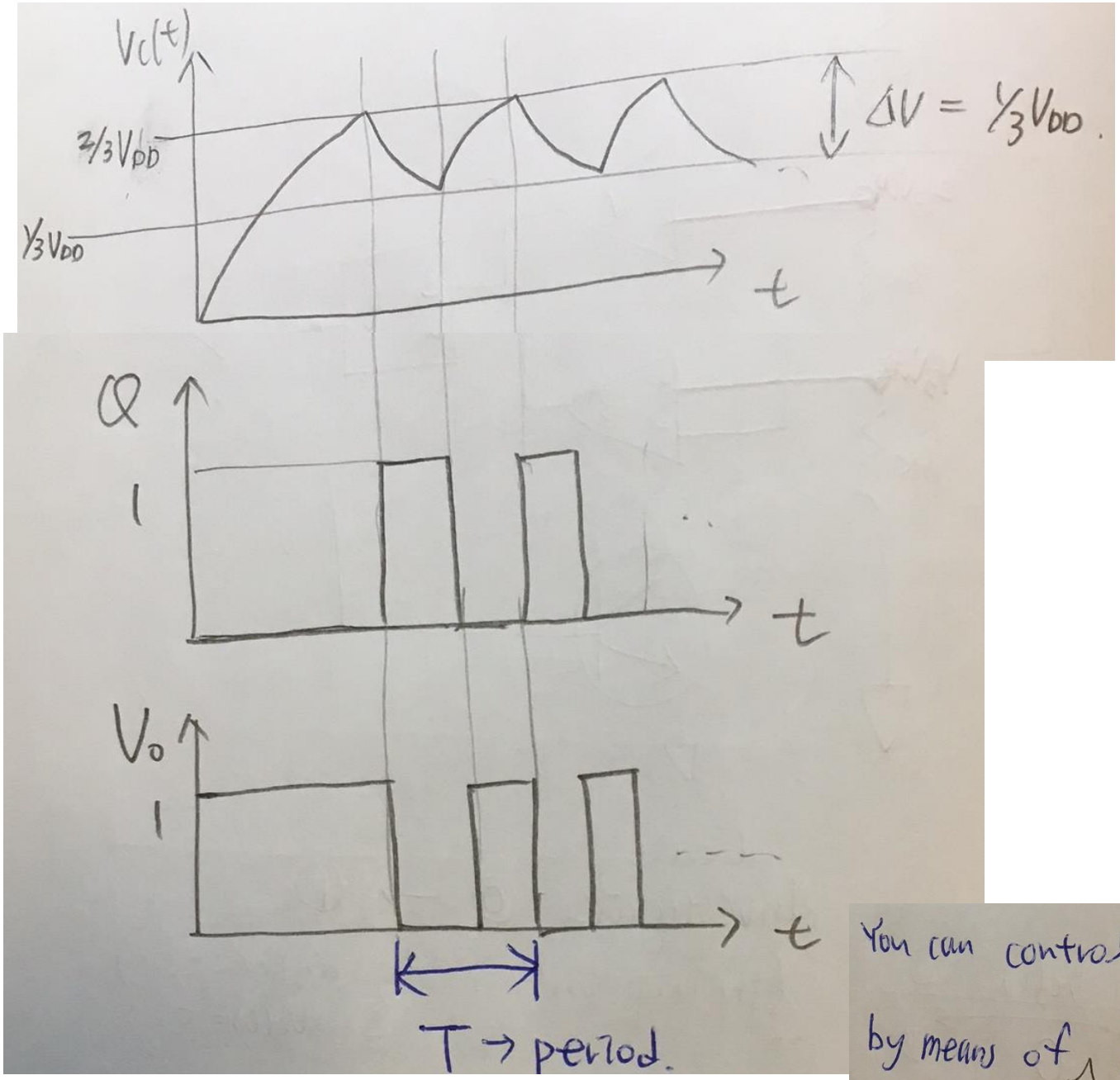
If $V_+ \geq V_- \Rightarrow 1$

If $V_+ < V_- \Rightarrow 0$



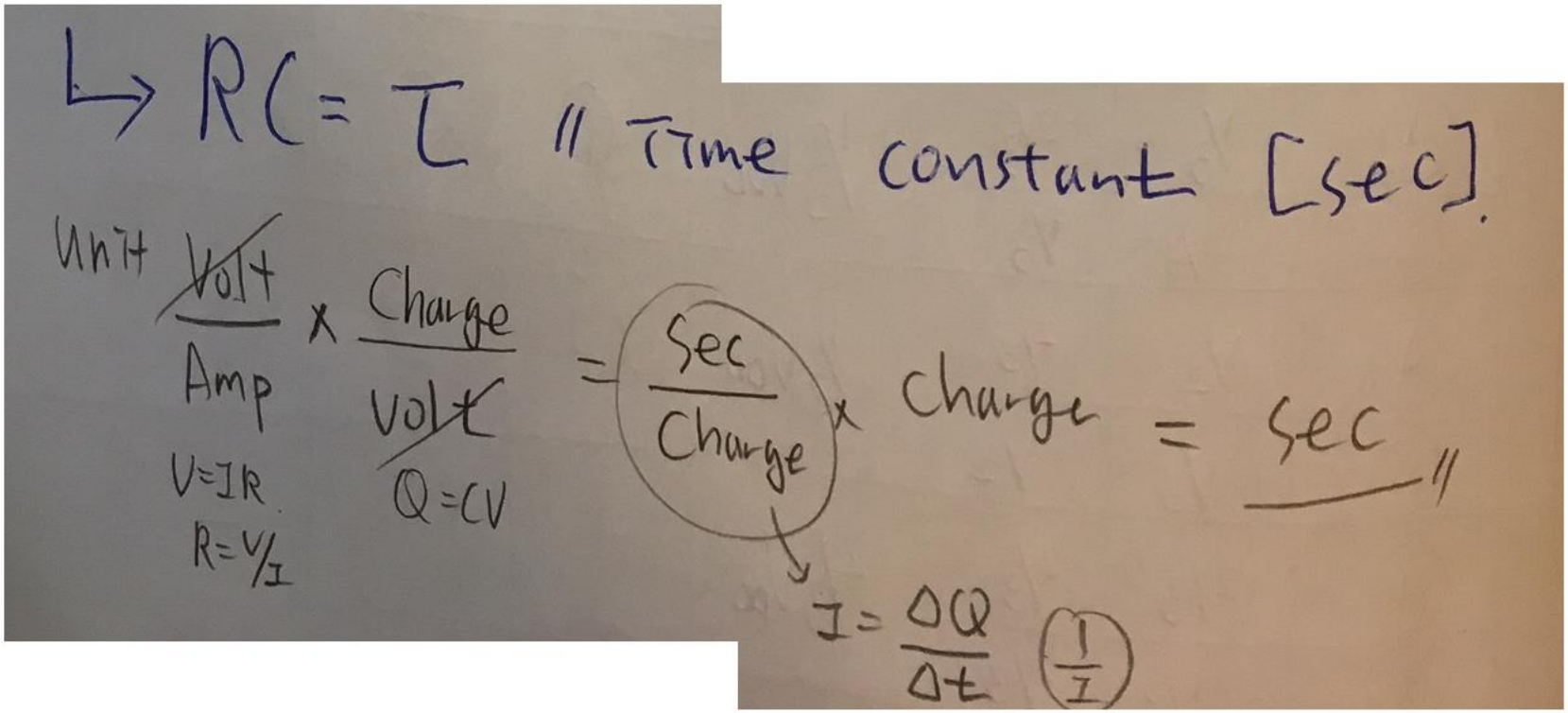
S	R	Q
0	0	Unchange
1	0	1
0	1	0
1	1	nouse

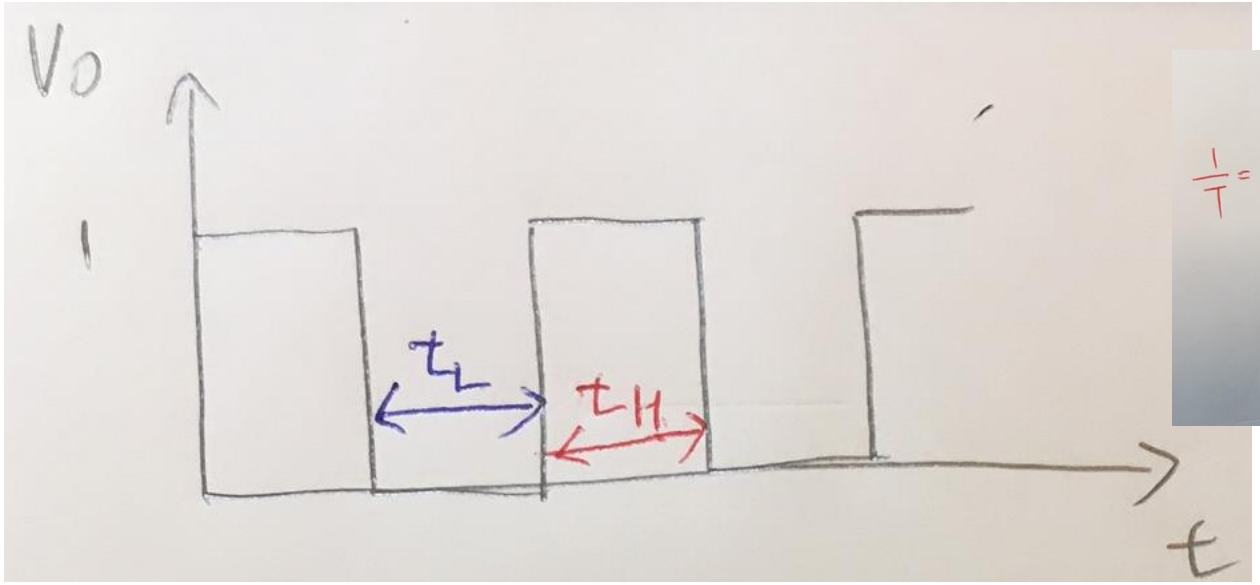
t	Comp	+	-	Vc(t)
⓪				0
				$\frac{1}{3}V_{DD}$
				$\frac{1}{2}V_{DD}$
①				$\frac{2}{3}V_{DD}$



You can control $T = \frac{1}{f}$

by means of External R_A, R_B, and C.


↳ RC = τ // Time constant [sec].
Unit Volt/Amp x Charge/Volt = Sec/Charge x Charge = Sec //
V=IR
R=V/I
Q=CV
I = ΔQ/Δt (1/I)



$$T = t_L + t_H$$

$$\frac{1}{T} = f = \frac{1.44}{(R_1 + 2R_2)C}$$

$$t_H = 0.7(R_1 + R_2)C \quad , \quad t_L = 0.7 R_2 C$$

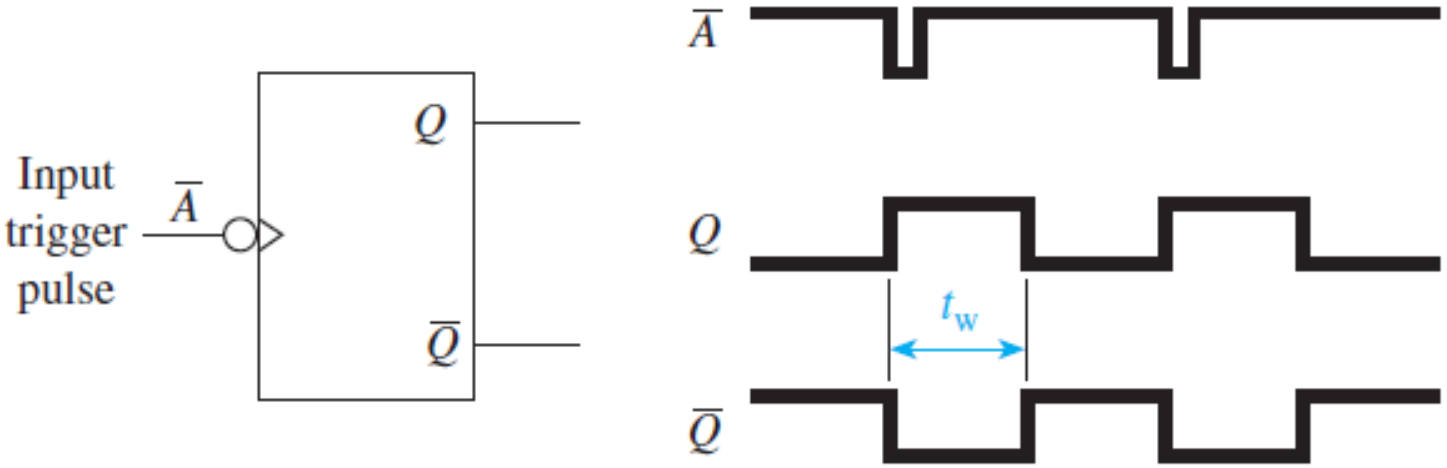
$$\text{Duty cycle} = \frac{t_H}{T} = \left(\frac{R_1 + R_2}{R_1 + 2R_2}\right) \times 100\%$$

Since C charges through RA and RB and discharges through only RB:

- <u>The duty cycles approaching a minimum of 50% can be achieved if RB>>RA</u>
- If that happens the charging and discharging times are approximately equal

2. Monostable Multivibrators (one-shot)

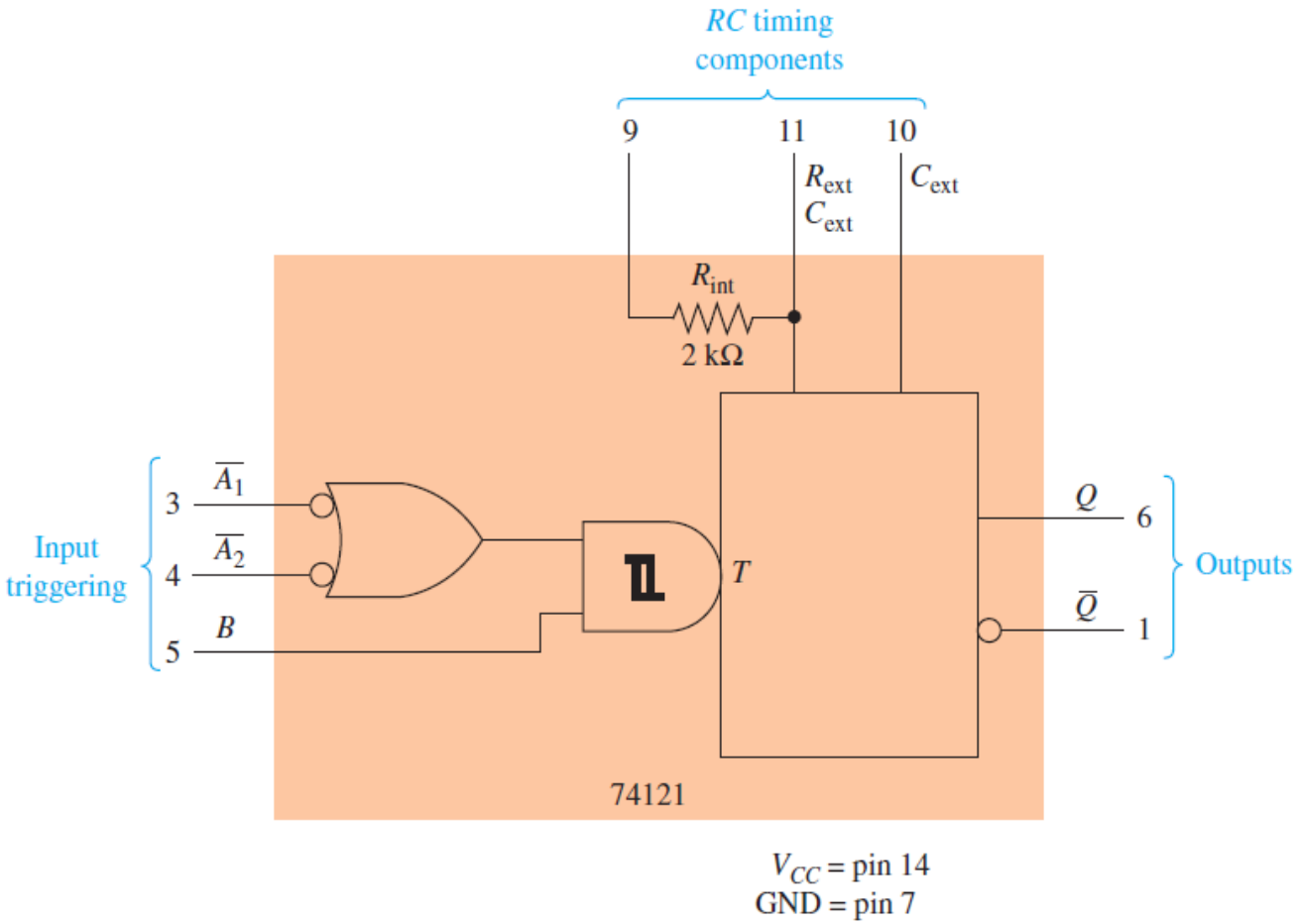
- Also called as “one-shot”
  - Has one stable state (Q=LOW, Q’=HIGH)
  - Outputs change state for a specific length of time (t_w) when A’ is triggered (negative edge)



IC Non-retiriggerable Monostable Multivibrators

- **74121**
  - Connect RC components for proper pulse width
  - Two active-LOW trigger inputs
  - One active-HIGH trigger input
- $t_w = R_{ext}C_{ext}\ln 2 = R_{ext}C_{ext}0.693$

- 74121 block diagram and function table

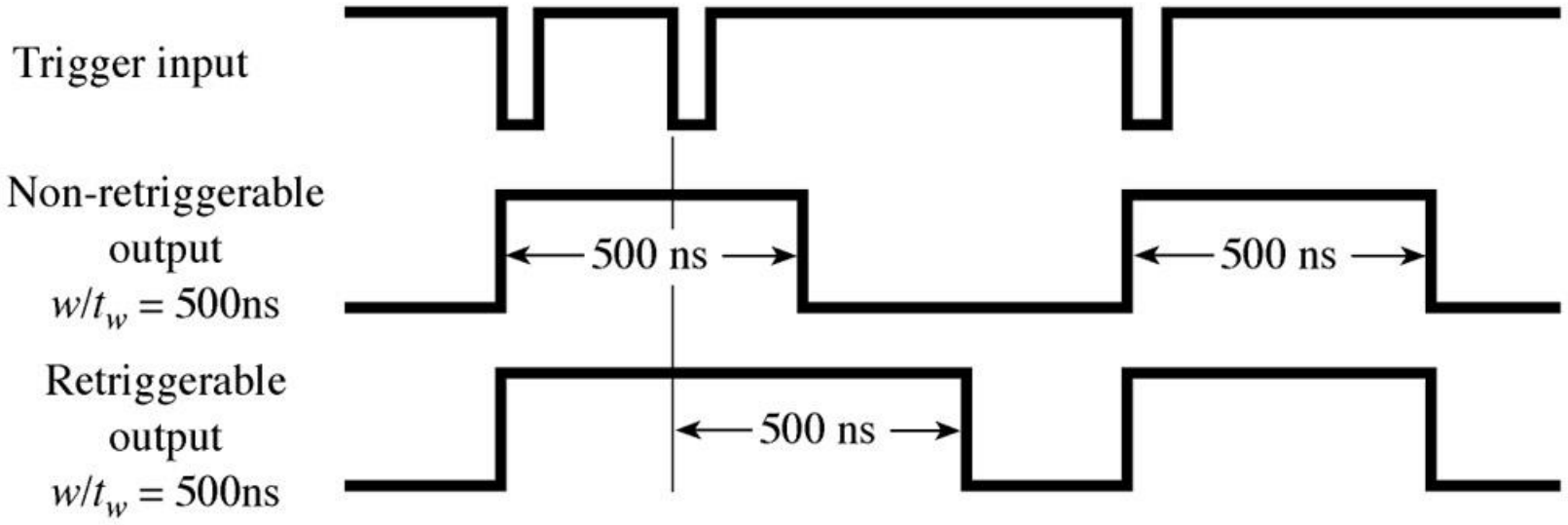


Inputs			Outputs	
$\overline{A}_1$	$\overline{A}_2$	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⊓	⊓
↓	H	H	⊓	⊓
↓	↓	H	⊓	⊓
L	X	↑	⊓	⊓
X	L	↑	⊓	⊓

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

IC Retiriggerable Monostable Multivibrators

- **74123**
  - New timing cycle each time new trigger applied

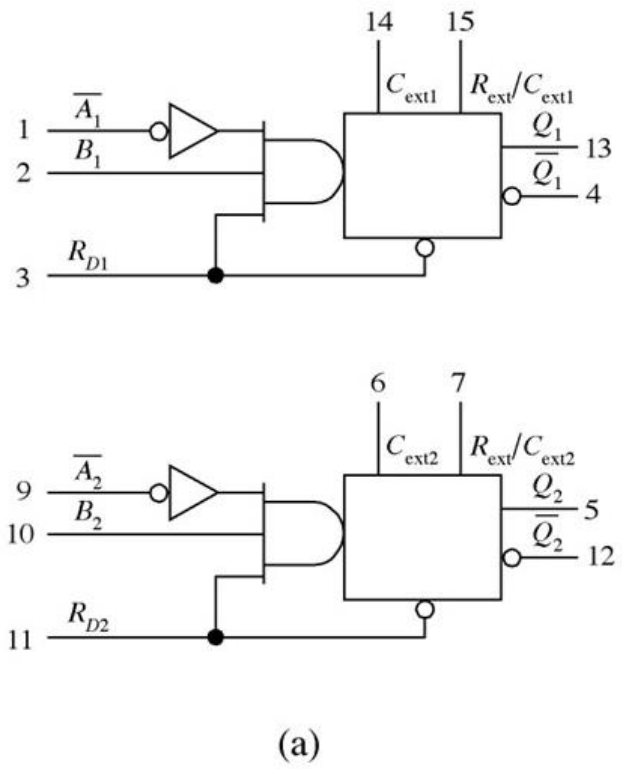


- **74123**
  - Dual multivibrator
  - Active low reset (R_D) which forces Q low
  - No internal timing resistor
  - Pulse width is determined using, If C_{ext} is greater than or equal to 1000 pF

$$t_w = 0.28 R_{ext} C_{ext} \left(1 + \frac{700}{R_{ext}} \right)$$

  - C_{ext}<1000pF, the graph in Figure 14-18 can be used to select components.

- 74123 logic symbol and function table



(a)

Input			Output	
R_D	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = One HIGH-level pulse
⎎ = One LOW-level pulse

(b)

Design a circuit using a 74121 to convert a 50-kHz, 80% duty cycle square wave to a 50-kHz, 35% duty cycle square wave. The structure and connection of a 74121 chip is given on the figure below.

(a) Determine R_{ext} value, if $C_{ext} = 1nF$

(b) Determine period of the 50kHz signal (t_{period})

(c) Determine pulse width (t_w)

$t_w = t_{period} * dutycycle$

Summary

- Multivibrator circuits are used to produce free-running clock oscillator waveforms or to produce a timed digital level change triggered by an external source.
- Capacitor voltage charging and discharging rates are the most common way to produce predictable time duration for oscillator and timing operations.

- An astable multivibrator is a free-running oscillator whose output oscillates between two voltage levels at a rate determined by an attached RC circuit.
- A monostable multivibrator is used to produce an output pulse that starts when the circuit receives an input trigger and lasts for a length of time dictated by the attached RC circuit.

- The 74121 is an IC monostable multivibrator (non-retriggerable) with two active-LOW and one active-HIGH input trigger sources and an active-HIGH and an active-LOW pulse output terminal.
- Retriggerable monostable multivibrators (74123) allow multiple input triggers to be acknowledged even if the output pulse from the previous trigger had not expired.

- The 555 IC is a general-purpose timer that can be used to make astable and monostable multivibrators and perform any number of other timing functions.

ECE210 Final Exam

Capacitor charging/discharging curve

$$\Delta v = E(1 - e^{-t/RC})$$

74121 output pulse width t_w

$$t_w = R_{ext} C_{ext} \ln(2)$$

$$t_w = 0.693 R_{ext} C_{ext}$$

555 timer t_{HI} and t_{LO}

$$t_{LO} = 0.693 R_B C$$

$$t_{HI} = 0.693(R_A + R_B)C$$

Monostable Multivibrators by 74123

- **If Cext>1000 pF, the output pulse width t_w: .**

$$t_w = 0.28 R_{ext} C_{ext} (1 + \frac{700}{R_{ext}})$$

- **If Cext <= 1000 pF, the output pulse width t_w can be found the right chart.**