Agenda

- Lecture: Timing in sequential logics
  - Setup/hold time
  - Clock skew

Sequential timing equations (all we need)

1. Hold Time Constraint:

   $t_{\text{hold}} < t_{ccq} + t_{cd}$

2. Hold Time Constraint with Skew:

   $t_{\text{hold}} + t_{\text{skew}} < t_{ccq} + t_{cd}$

3. Setup Time Constraint:

   $T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$

4. Setup Time Constraint with Skew:

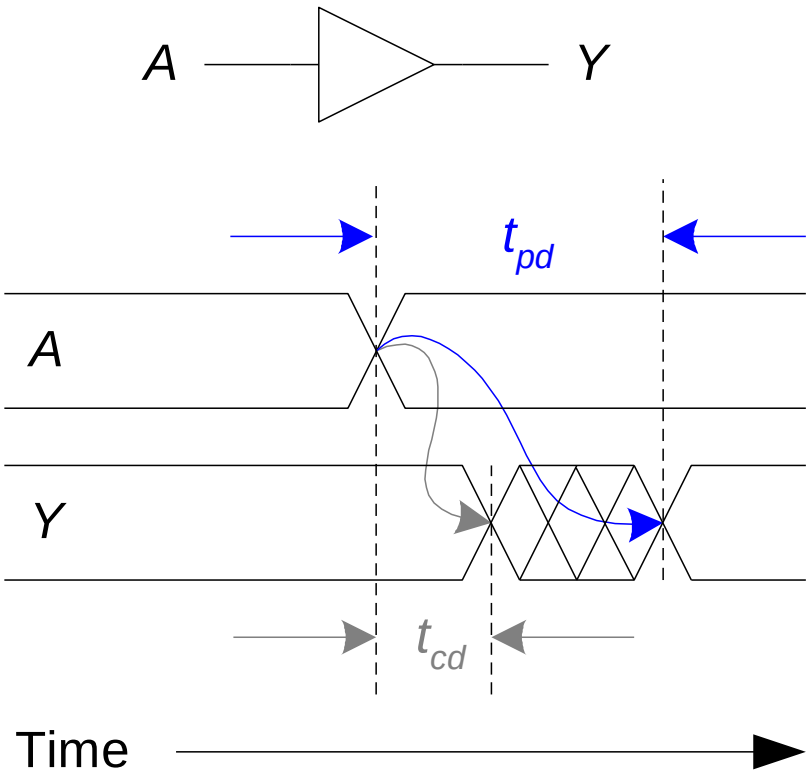
   $T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} + t_{\text{skew}}$

Let's go over all subscripts first.

Recap: timing in combinational logics

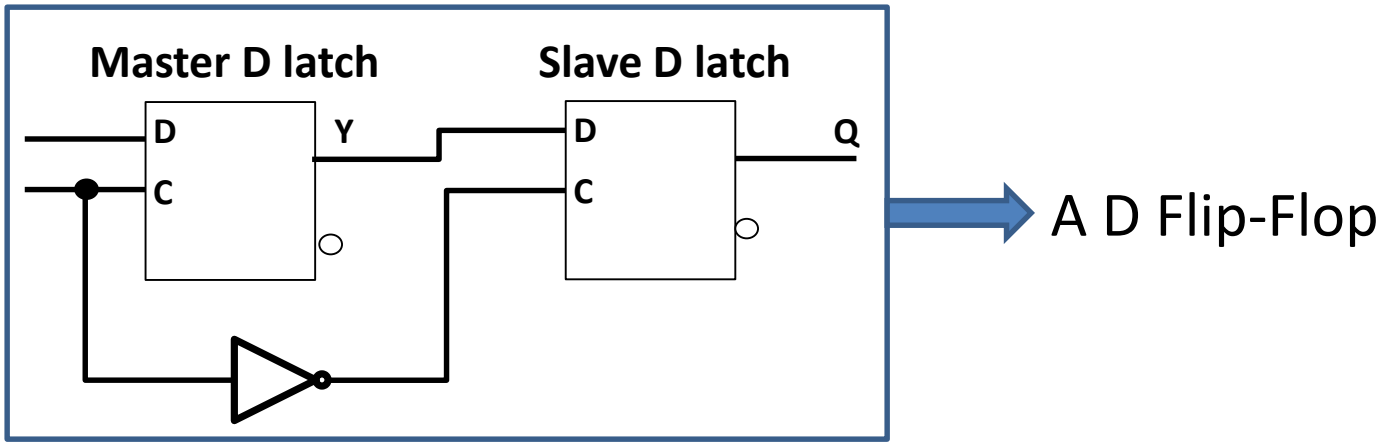
Propagation & Contamination Delay

- Propagation delay: t_{pd} =
- Contamination delay: t_{cd} =



Actual signal arriving time **at outputs**

Intro to timing in sequential logics



Flip-flop samples *D* at clock edge

- *D* must be stable when sampled
- *D* must be stable around clock edge

If not, metastability can occur

Let's explain this idea in an academic manner

- Describe the situation using terminologies as like we did in combinational logics study; propa– d, combin—d

A big picture of timing analysis in SLs:

- A step by step consideration of

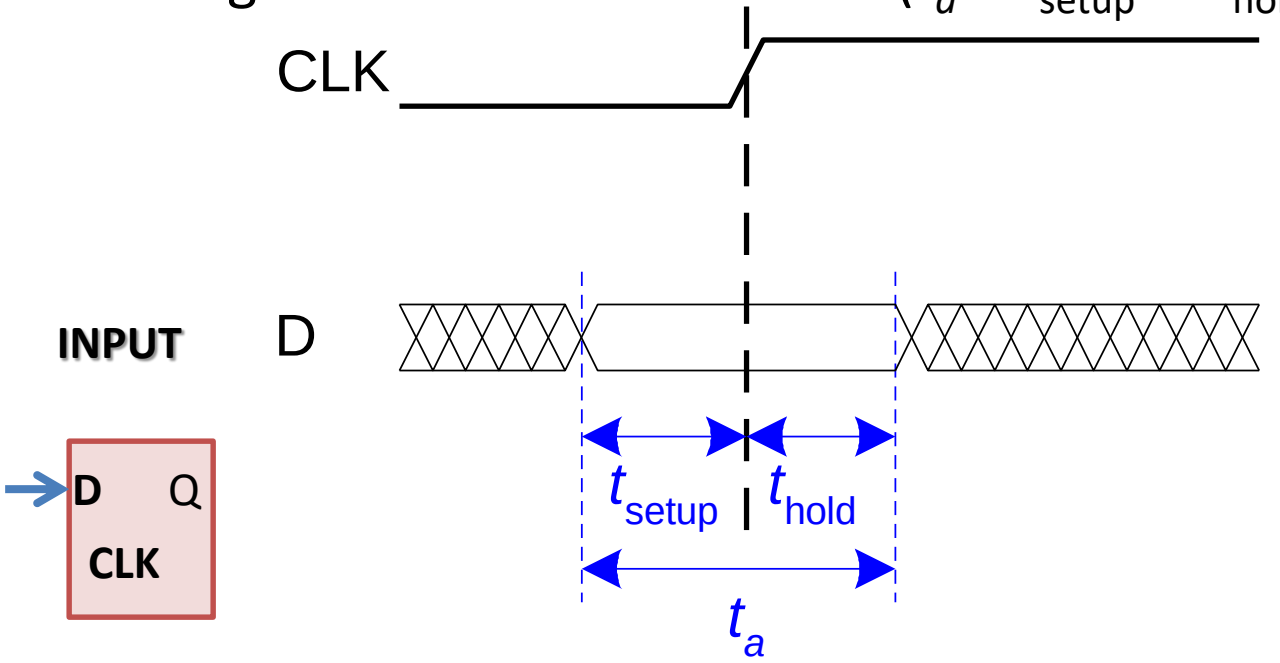
  inputs,

  outputs,

  and clock

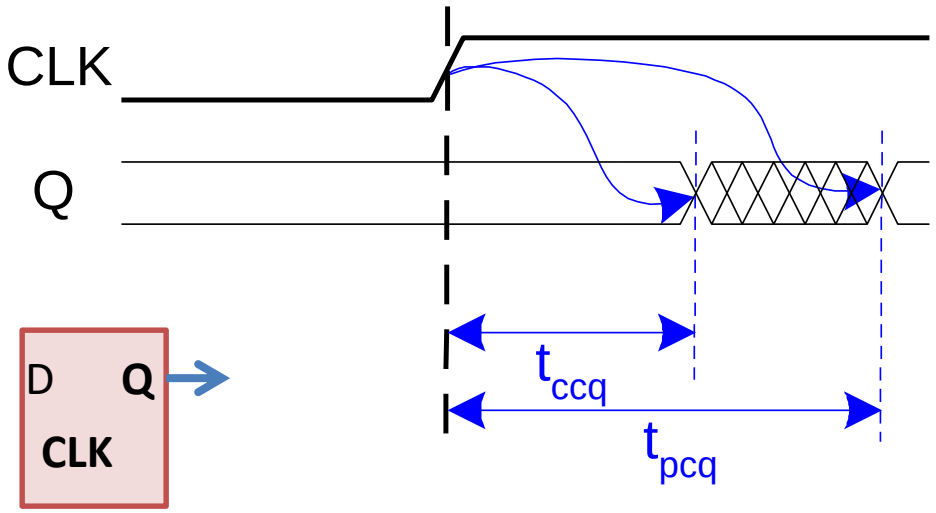
Input Timing

- **Setup time:** t_{setup} = time *before* clock edge data. It must be stable (i.e. not changing, guaranteed to be stable)
- **Hold time:** t_{hold} = time *after* clock edge data. It must be stable (guaranteed to be stable)
- Aperture time (Data required interval): t_a = time *around* clock edge data. It must be stable ($t_a = t_{setup} + t_{hold}$)



Output Timing

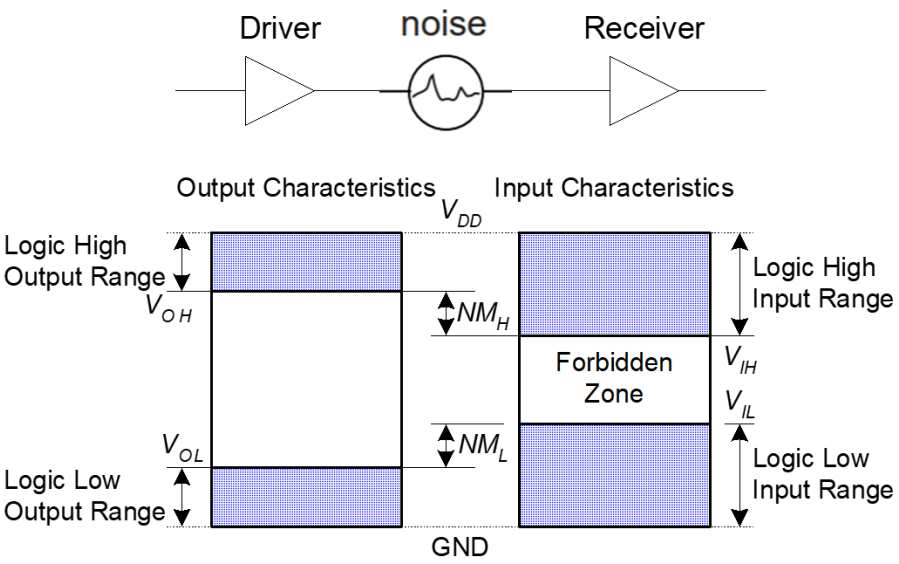
- **Propagation delay, clk to Q: t_{pcq}** = time after clock edge that the output *Q* is guaranteed to be stable (i.e., to stop changing, maximum t) ←→ t_{pd} in Comb. logics
- **Contamination delay, clk to Q: t_{ccq}** = time after clock edge that *Q* might be stable (or not) (i.e., start changing, minimum t) ←→ t_{cd} in Comb. logics



- Synchronous sequential circuit **inputs** must be stable during aperture (setup and hold) time around clock edge
- Specifically, **inputs** must be stable
  1. at least t_{setup} before the clock edge: setup time constraint
  2. at least until t_{hold} after the clock edge: hold time constraints
  3. 1 and 2 are considered with the clock skew concept

RECAP: cascading two components to analyze from “OUTPUT” to “INPUT”

A chain of two buffers

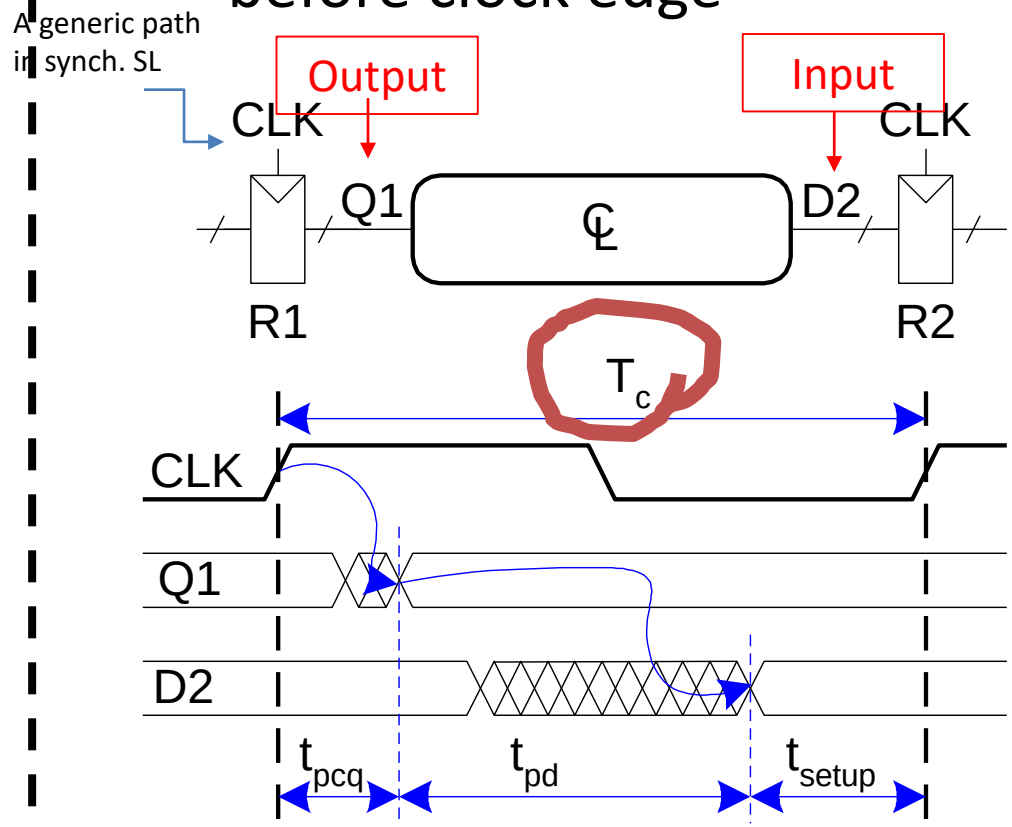


High Noise Margin: $NM_H = V_{OH} - V_{IH}$

Low Noise Margin: $NM_L = V_{IL} - V_{OL}$

Setup Time Constraint

- Depends on the **maximum** delay from register R1 through combinational logic to R2
- The **input** to register R2 must be stable at least t_{setup} before clock edge



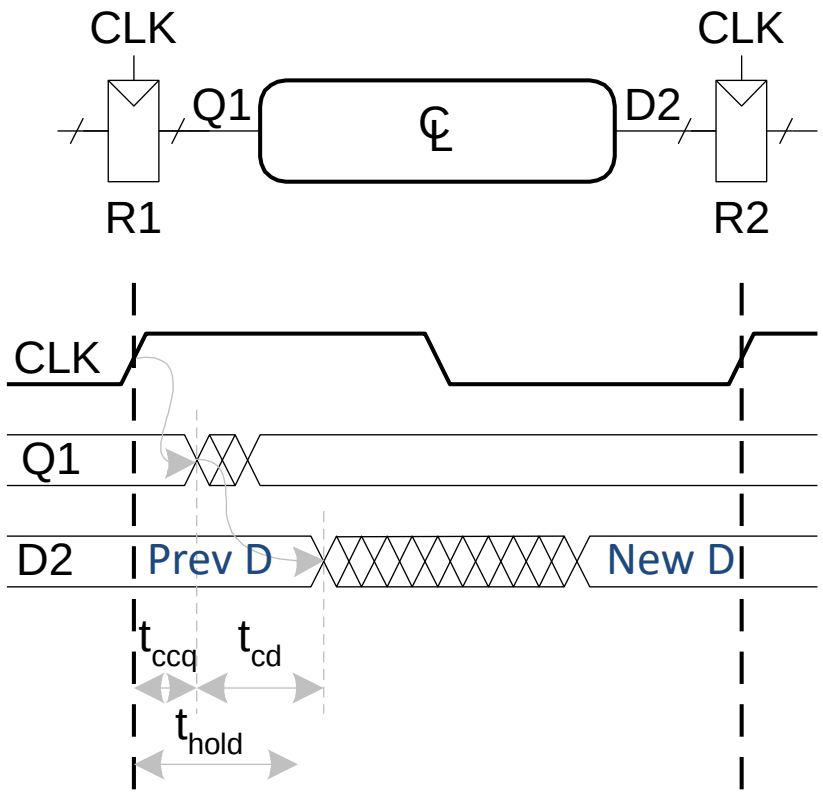
CLK period must be longer than this

$$T_c \;?\; t_{pcq} + t_{pd} + t_{setup}$$

$(t_{pcq} + t_{setup})$: *sequencing overhead*

Hold Time Constraint

- Depends on the **minimum** delay from register R1 through the combinational logic to R2
- After the rising edge of the clock, D2 must not change until t_{hold} and might change as soon as $t_{ccq}+t_{cd}$

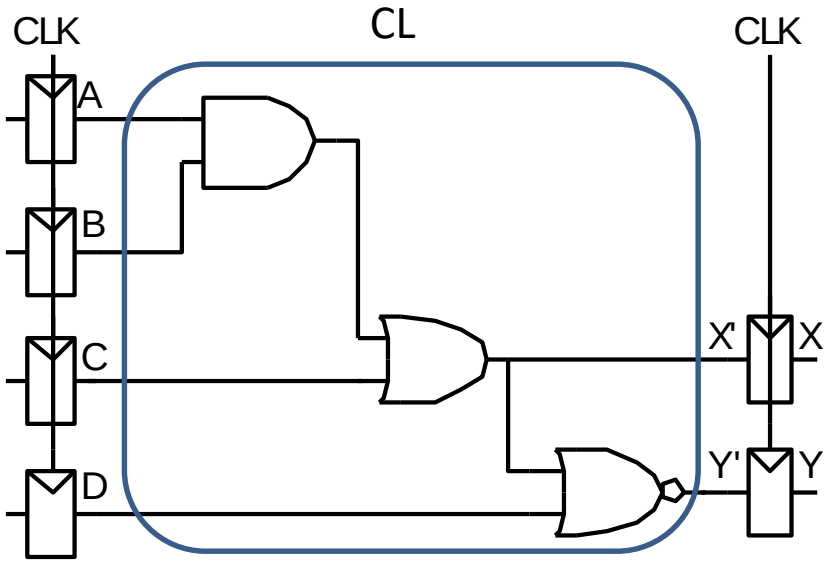


$$t_{hold} \stackrel{?}{} t_{ccq} + t_{cd}$$

If you hold previous input (D2) too long, you can't take next output from Q1

Examples: Timing Analysis, setup/hold time constraint

Q. Find the minimum clock period (in sec) to work with this circuit. And check if this circuit satisfy hold time constraint.



Timing Characteristics per gate

t_{ccq} = 30 ps
t_{pcq} = 50 ps
t_{setup} = 60 ps
t_{hold} = 70 ps

per gate:
t_{pd} = 35 ps
t_{cd} = 25 ps

Consider entire CL's:
t_{pd} = Critical path
t_{cd} = Shortest pat

Hold time constraint:

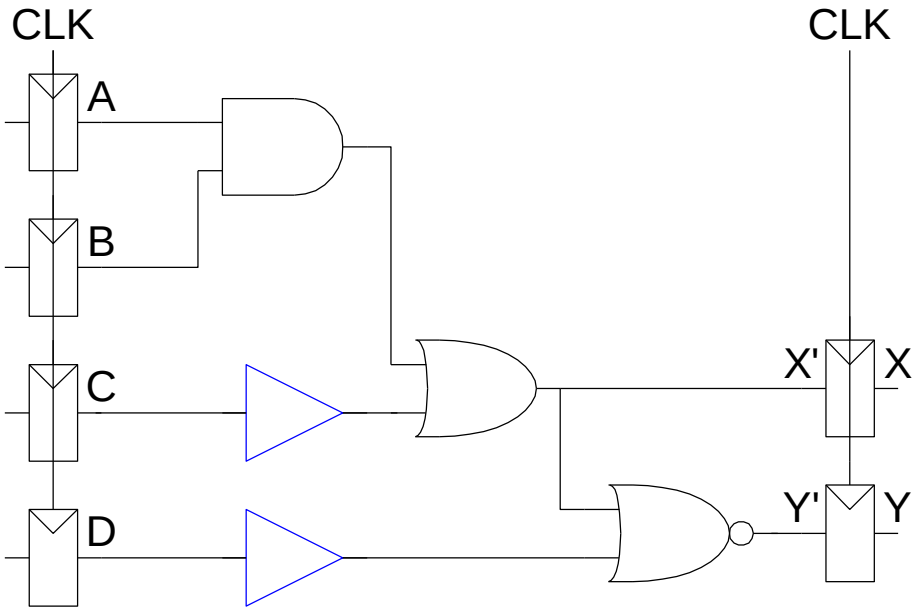
$t_{ccq} + t_{cd} > t_{hold}$?

Setup time constraint:

$T_c \geq$?

Maximum clock frequency to work with this circuit!

Let's add buffers to the short paths:



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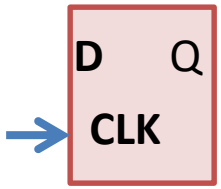
Setup time constraint:

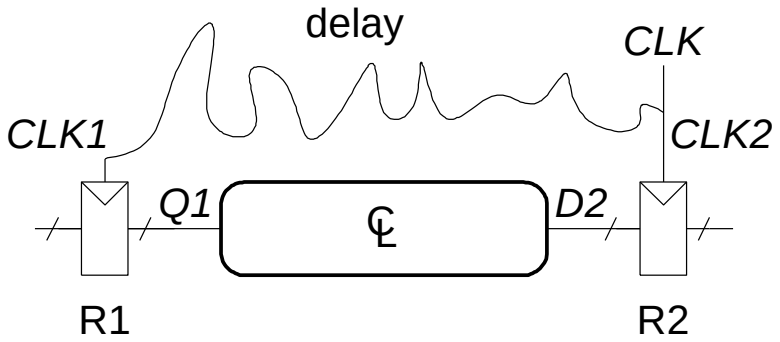
$T_c \geq$?

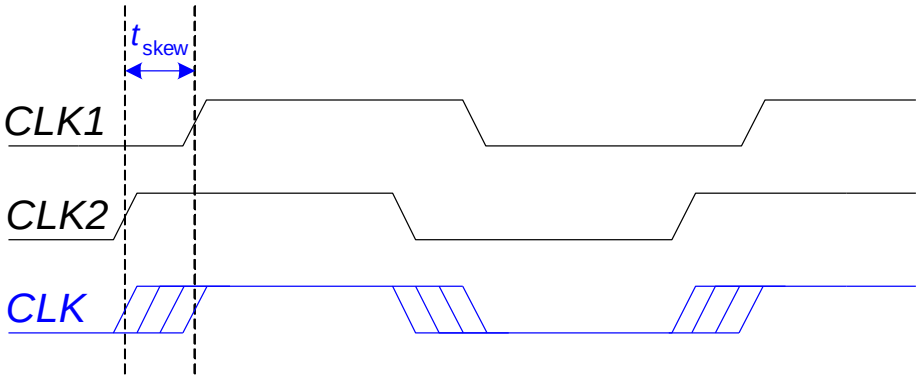
Changed or not?


D
Q
CLK

Setup/hold time constraints (+) Clock Skew

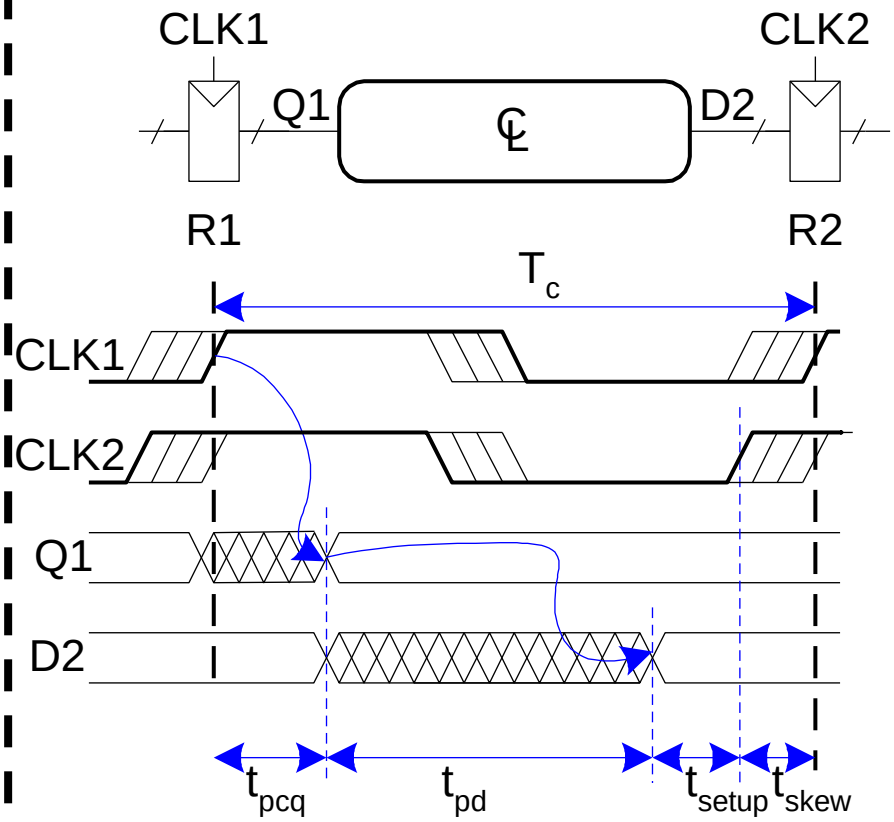
- **The clock doesn't arrive at all registers at same time**
- **Skew:** difference between two clock edges
- Perform **worst case analysis** to guarantee dynamic discipline is not violated for any register – many registers in a system!





Setup Time Constraint with Skew

- In the worst case, CLK2 is earlier than CLK1

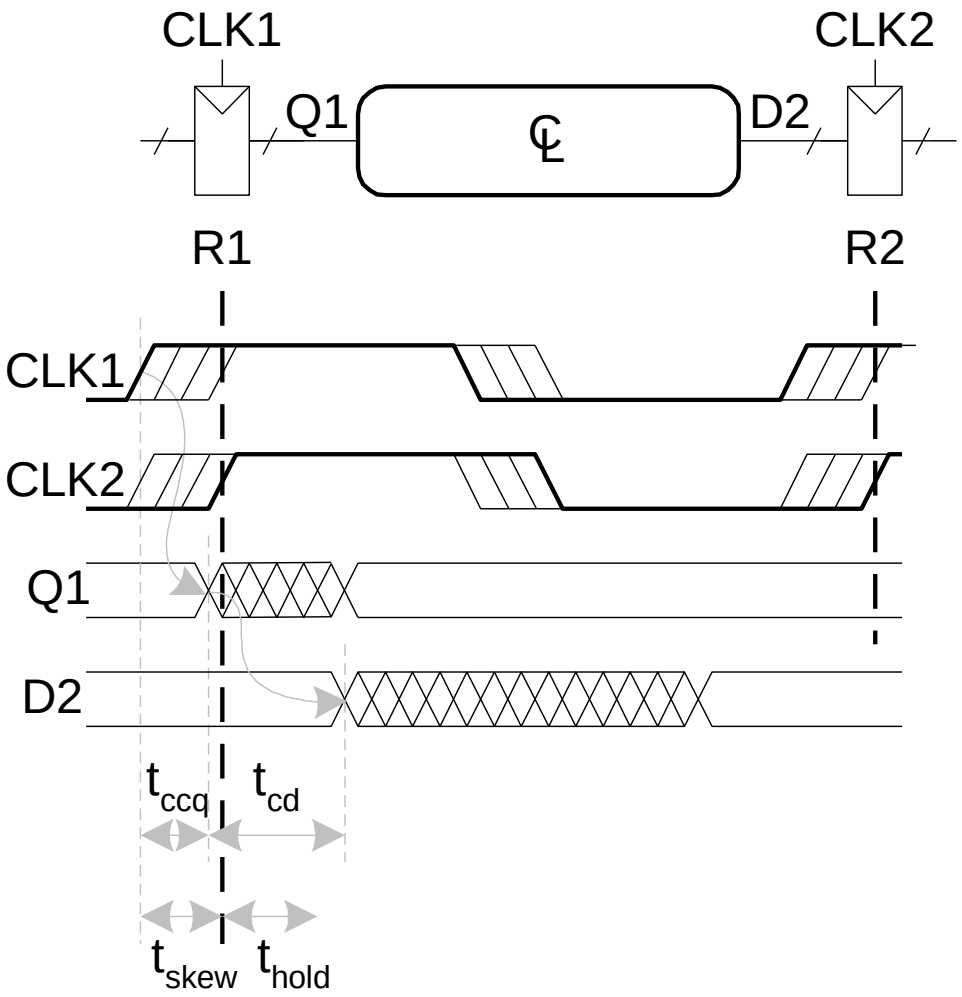


$T_c \geq ?$

T_c should be larger than input/output's undesired effects

Hold Time Constraint with Skew

- In the worst case, CLK2 is later than CLK1



$$t_{hold} < t_{ccq} + t_{cd}$$

Which hand-side is for t_{skew}?
→clock is a kind of inputs

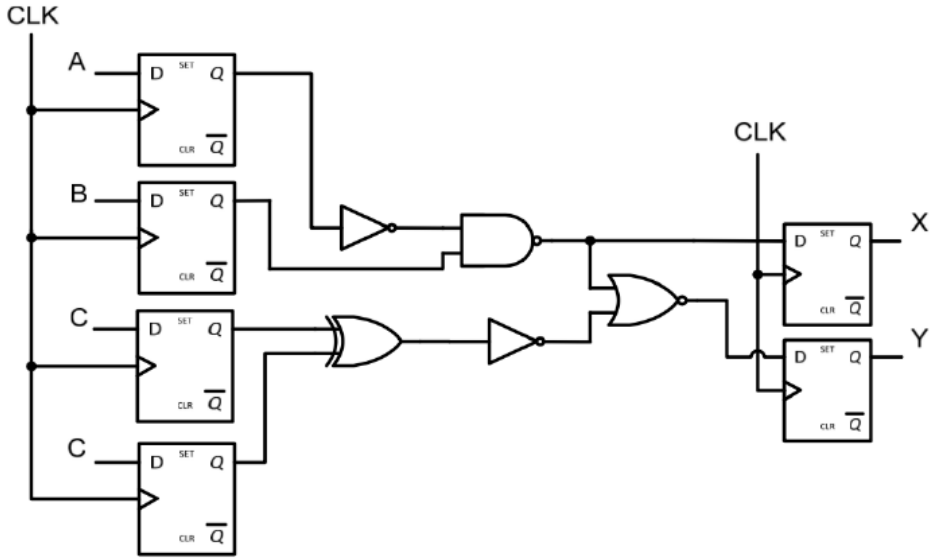
An example

- A sequential circuit design is shown with its delay parameters:

D-FF clk-to-q propagation delay $t_{pcq} = 18$ ps
D-FF clk-to-q contamination delay $t_{ccq} = 12$ ps
D-FF data setup time $t_s = 14$ ps
D-FF data hold time $t_h = 7$ ps

Table 1: Propagation delay for certain gates

Gate	T_{pd} (ps)	T_{cd} (ps)
2-input NAND	17	11
2-input NOR	27	16
2-input XOR	36	26
NOT	11	6



a. Calculate the maximum clock frequency for reliable operation assuming there is no clock skew
b. How much clock skew can the circuit tolerate before it experiences a hold time violation?

We discussed several equations, which one should we apply for each question?

Summary of sequential timing eqs.

1. Hold Time Constraint:

$$t_{\text{hold}} < t_{ccq} + t_{cd}$$

2. Hold Time Constraint with Skew:

$$t_{\text{hold}} + t_{\text{skew}} < t_{ccq} + t_{cd}$$

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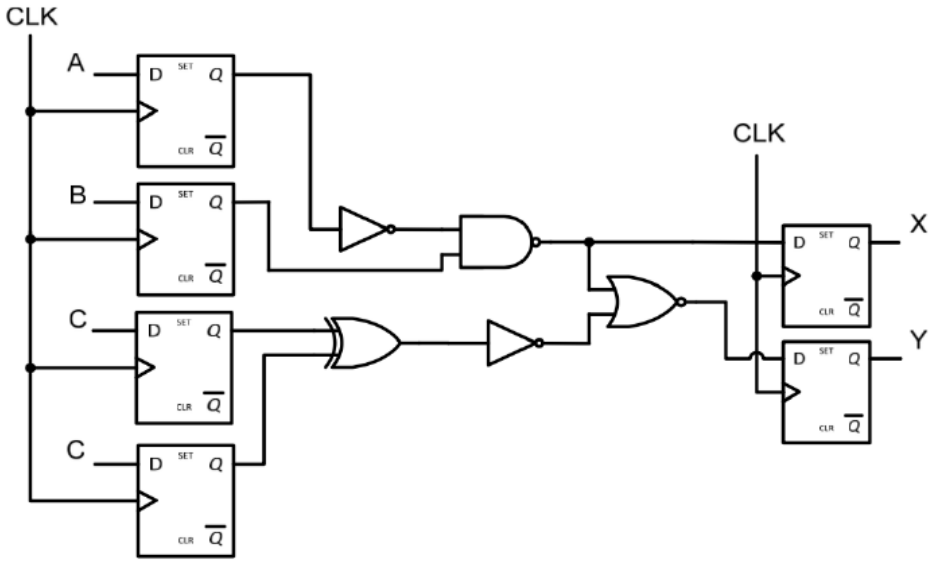

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