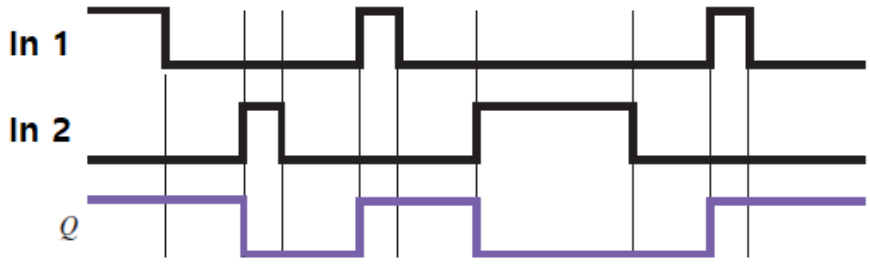
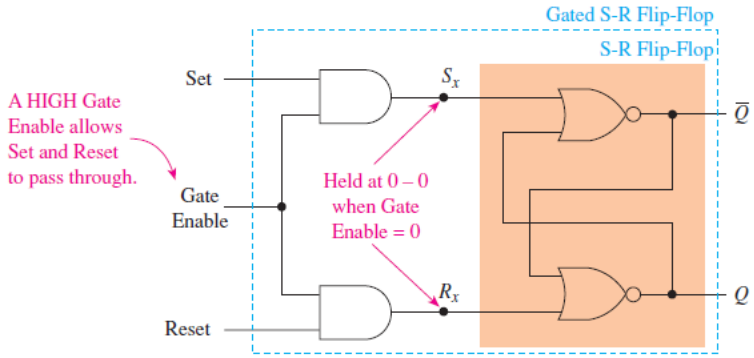
Questions

1. Given the Q output waveform shown in the figure below, determine the name of latch.



S-R latch

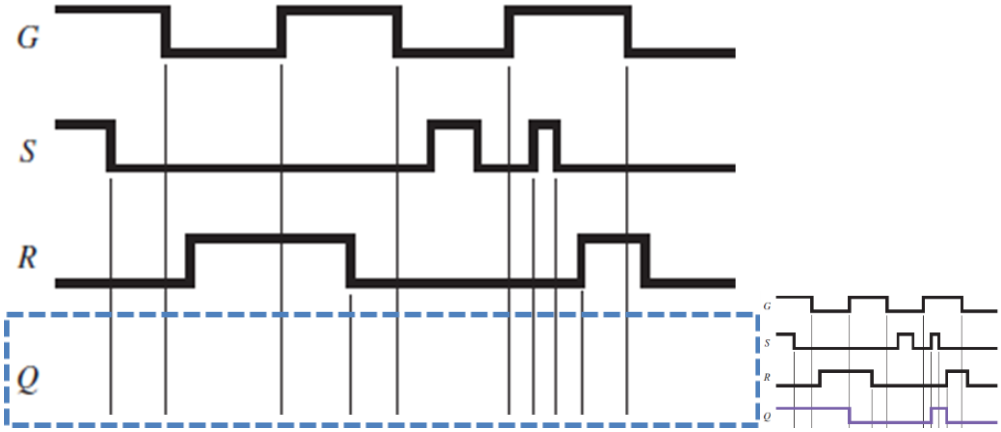
2. The following figure shows a Gated S-R flip-flop.



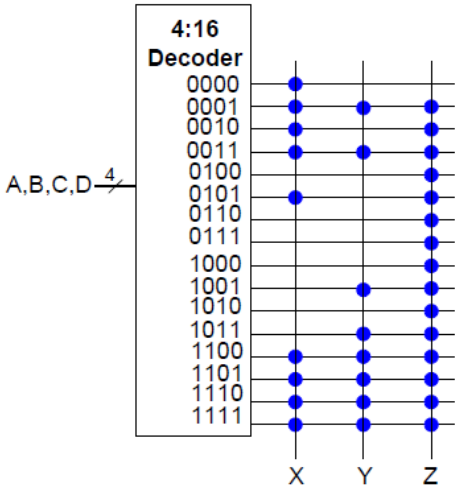
a. Find its truth table (Inputs are S, G,R and output is Q)

G	S	R	Q
0	0	0	Q
0	0	1	Q
0	1	0	Q
0	1	1	Q
1	0	0	Q
1	0	1	0
1	1	0	1
1	1	1	0

b. Feed the G, S, and R inputs in the gated S-R flip-flop, sketch the output wave at Q, and list the flip-flop functions



3. The following figure shows X, Y, Z functions' implementation using a single 16 X 3 ROM. Dot notations are used to indicate the ROM contents.



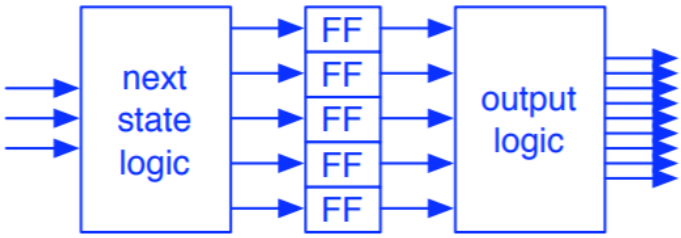
For example, X is a function which can be represented via following Boolean equation:

$$X = AB + B\bar{C}D + \bar{A}\bar{B}.$$

Determine functions Y and Z accordingly. Provide simplified Boolean equations.

Y=AB+B'D
Z=A+B+C+D

4. The following figure shows a Moore machine which has five flip-flops, three inputs, and nine outputs. Assume a state encoding that makes efficient use of the flip-flops.



Answer the following questions:

a. What are the minimum and maximum numbers of states in the state diagram?

The minimum number of states in the diagram is $2^{5-1} + 1 = 17$ and the maximum is $2^5 = 32$.

b. A fully defined machine needs to know what action to take for all possible inputs. What are the minimum and maximum numbers of transition arrows starting at a particular state (originating from each state)?

At a minimum each node will have 2^3 (8) transitions originating from it. Similarly, it is not possible to have more than one transition on a particular input. Thus, the maximum number of outgoing transitions is also 2^3 (8)
Min=Max=8

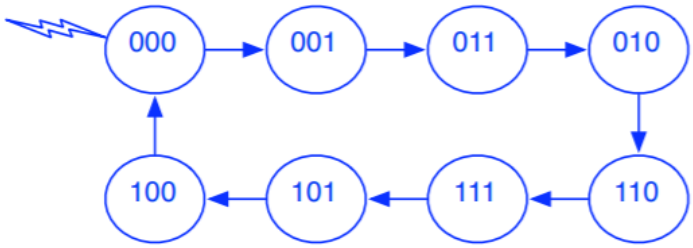
c. What are the minimum and maximum numbers of different binary patterns that can be displayed on the outputs? For the maximum case, a hint is this is a Moore machine. For the minimum case, assume that any output logic that is a function of the 5 state bits is valid.

Because this is a Moore machine, the output is a function of only the 5 state bits. At most, the machine can display as many outputs as there are states, or 2^5 (32). The minimum number of output values depends on certain assumptions about the output logic. However, assuming, logic that assigns a constant value to the output no matter the state would produce the minimal number of output values (1).
Max=32, Min=1

5. Gray codes have a useful property in that consecutive numbers differ in only a single bit position. The following table lists a 3-bit Gray code representing the numbers 0 to 7.

Number	Gray code
0	0 0 0
1	0 0 1
2	0 1 1
3	0 1 0
4	1 1 0
5	1 1 1
6	1 0 1
7	1 0 0

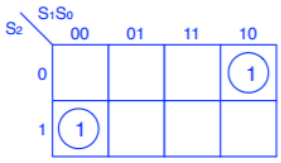
Design a 3-bit modulo 8 Gray code UP counter FSM with no inputs and three outputs. The designed counter counts from 0, 1, 2, 3, 4, 5, 6 and 7, then repeats in Gray code pattern. When reset, the output should be 000. **On each clock edge, the output should advance to the next Gray code (meaning that T_n is simply S_n).** After reaching 100, it should repeat with 000. Draw a schematic for this counter using T flip-flops. A transition diagram with encoding is shown as a starter of your design.



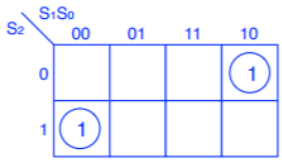
a. State Transition Table with encoding (T_n are inputs of each T flip-flop, S_n are states, + indicates next state logic)

S_2	S_1	S_0	S_2'	S_1'	S_0'	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	0	1	0	0	0	1
0	1	0	1	1	0	1	0	0
1	1	0	1	1	1	0	0	1
1	1	1	1	0	1	0	1	0
1	0	1	1	0	0	0	0	1
1	0	0	0	0	0	1	0	0

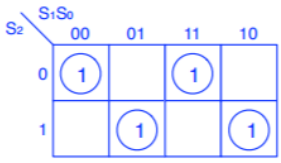
b. Simplify T_n equations using K-map or Boolean simplification.



$T_2 = S_2\overline{S_1}\overline{S_0} + \overline{S_2}S_1\overline{S_0}$



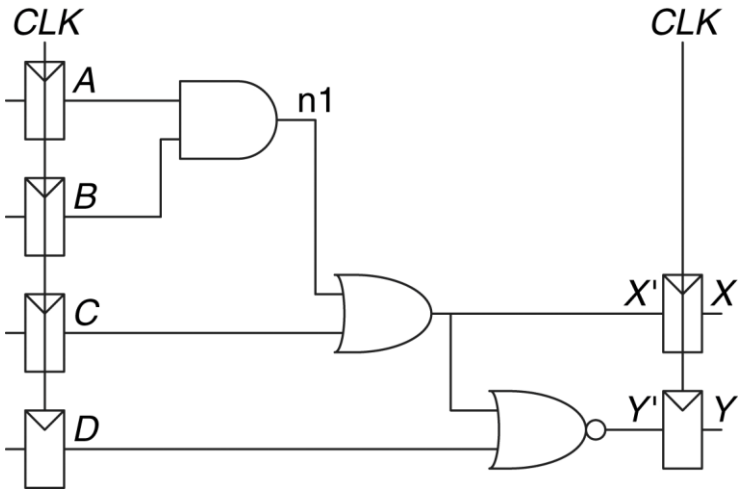
$T_1 = \overline{S_2}\overline{S_1}S_0 + S_2S_1S_0$



$T_0 = \overline{S_2}\overline{S_1}\overline{S_0} + \overline{S_2}S_1S_0 + S_2\overline{S_1}S_0 + S_2S_1\overline{S_0}$

6. Check the following circuit whether it violates hold time constraint. Also determine the maximum clock frequency. Timing Characteristics of each gate and flip-flop are given as follows:

t_{ccq} = 30 ps
t_{pcq} = 80 ps
t_{setup} = 50 ps
t_{hold} = 60 ps
t_{pd} = 40 ps
t_{cd} = 25 ps



$t_{ccq} + t_{cd} > t_{hold}$
30+25=55 > 60 (!)
Violates!
Tc>=tpcq +3*tpd+tsetup=80+3*40+50=250ps
F=1/Tc=4GHz

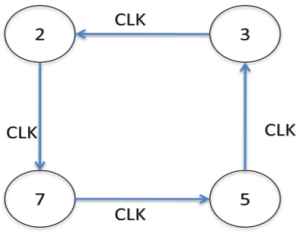
7. Design a 3-bit down counter (synchronous) that counts prime numbers (i.e., 2, 3, 5, 7). An initial 3-bit prime number is 010_2. Use three D-FFs for your answer.

   a. Write the next state's state transition

Previous state			Next state		
P2	P1	P0 (LSB)	N2	N1	N0 (LSB)
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

   b. Draw the transition diagram.

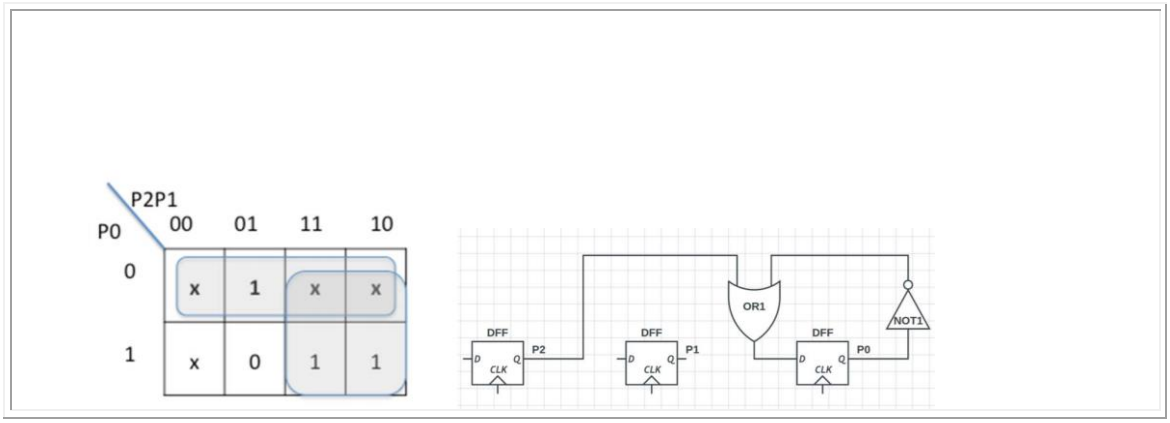
previous state			next state		
P2	P1	P0	N2	N1	N0
0	0	0	x	x	x
0	0	1	x	x	x
0	1	0	1	1	1
0	1	1	0	1	0
1	0	0	x	x	x
1	0	1	0	1	1
1	1	0	x	x	x
1	1	1	1	0	1



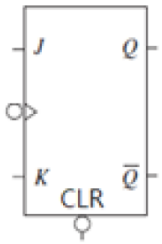
   c. Boolean equations for the next state using K-maps (all three bits).

N2=P2Pa+P0'
N1=P2'+P1'
N0=P2+P0'

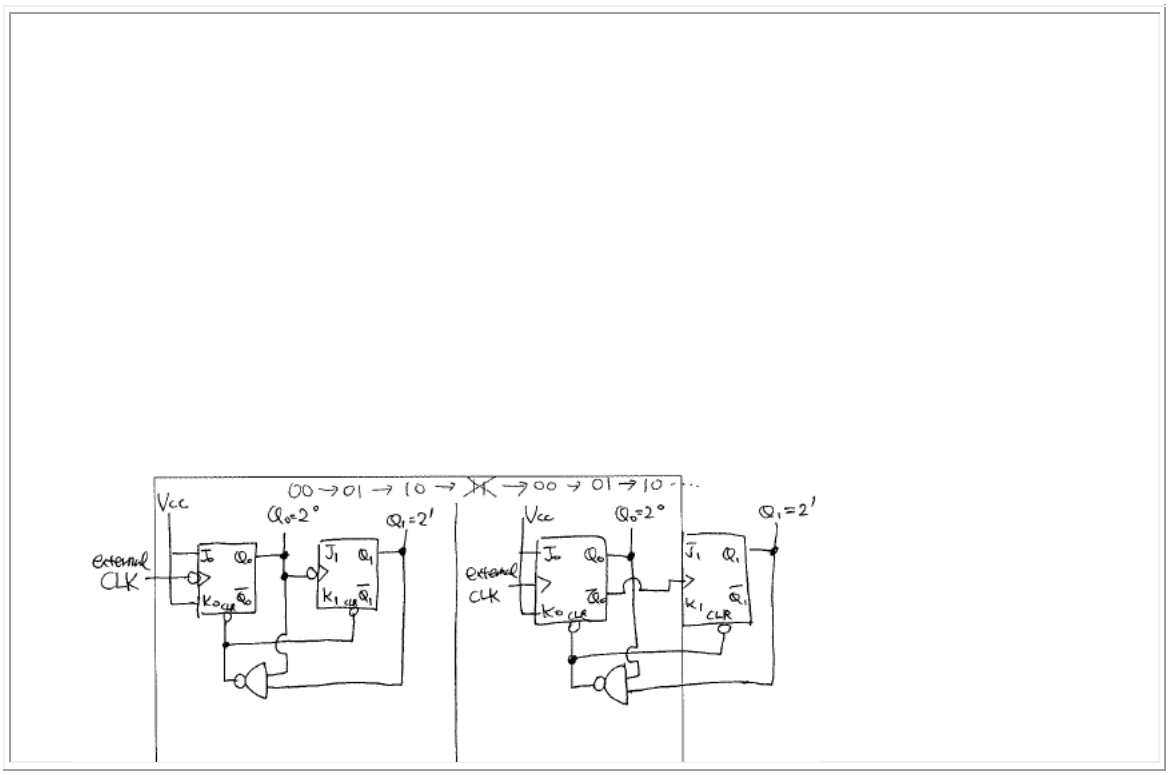
d. Design the circuit for the N0 - LSB of the next state



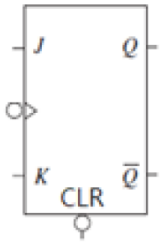
8. Design an asynchronous MOD3 up counter using JK FFs.



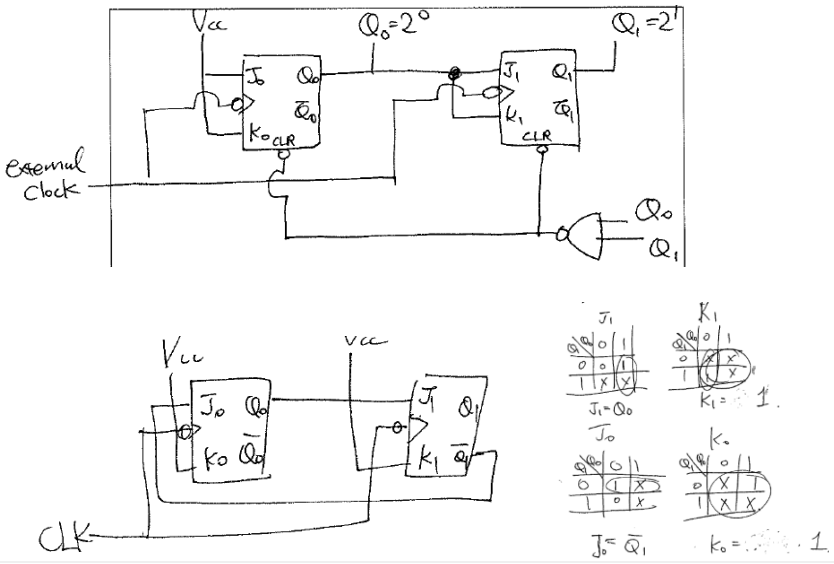
* A symbol of JK FF is given above. Use an additional logic gates when you need.
* Put a special consideration on CLR (clear). Due to “the bubble" placed on the CLR pin.
* Clearly label each JK FFs bit position (make LSB inputs as J0, K0 and LSB outputs: Q0 and Q0)
* Clarify wiring connection V_{cc} (or 1), GND (or 0), and an external clock if it needs.
* To check your counter working, assume that you connect LEDs on Q (not on Q’).



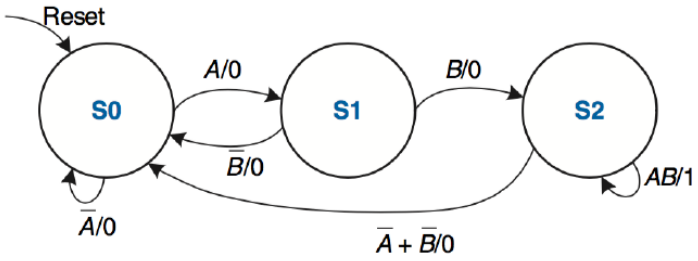
9. Design a synchronous MOD3 up counter using JK FFs.



* A symbol of JK FF is given above. Use an additional logic gates when you need.
* Put a special consideration on CLR (clear). Due to “the bubble" placed on the CLR pin.
* Clearly label each JK FFs bit position (make LSB inputs as J0, K0 and LSB outputs: Q0 and Q0)
* Clarify wiring connection V_{cc} (or 1), GND (or 0), and an external clock if it needs.
* To check your counter working, assume that you connect LEDs on Q (not on Q’).



10. Find a state transition table and output table for the FSM bleow. Write Boolean equations for the next state and output.



S_1	S_0	A	B	S_1^+	S_0^+	Q
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	1	0	0
0	1	1	0	0	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	1	0	1
1	1	0	0	X	X	X
1	1	0	1	X	X	X
1	1	1	0	X	X	X
1	1	1	1	X	X	X

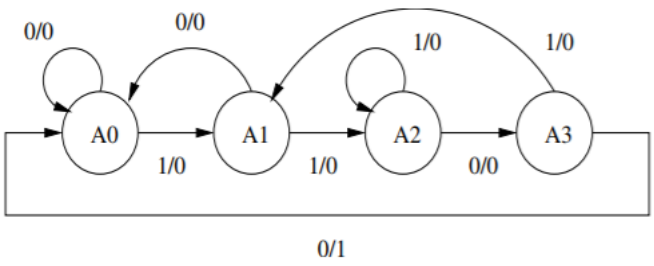
$S_1^+ = S_0 \cdot B + S_1 \cdot A \cdot B$
$S_0^+ = \bar{S_1} \cdot \bar{S_0} \cdot A$
$Q = S_1 \cdot A \cdot B$

11. A sequence detector has a serial input X and an output Z. Whenever the circuit receives a sequence of 1100 on input X during four consecutive clock cycles, it produces an output Z = 1 at the same time as the fourth input. At all other times, the output Z = 0. To further clarify the problem, an example of input/output sequence is shown below:

    X: 00110111000011110001100111...

    Z: 00000000010000000100001000...

    a. Obtain a state transition diagram for this problem. Use Mealy FSM. Label the starting state as A0 and other states as A1, A2, etc.



    b. Derive the state transition table.

S_1	S_0	X	S_1^+	S_0^+	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	0	1	0

Pres State	Next State , Z	
	$X = 0$	$X = 1$
A_0	$A_0, 0$	$A_1, 0$
A_1	$A_0, 0$	$A_2, 0$
A_2	$A_3, 0$	$A_2, 0$
A_3	$A_0, 1$	$A_1, 0$

12. This circuit uses negative edge-triggered JK flip-flops. Complete Input and output waveforms. Note that the clock input from the second FF comes from Q0.