Examples for Day 8

Dr. Noori Kim

The Karnaugh Map

Practice $\overline{A}\,\overline{B}C + \overline{A}B\overline{C} + AB\overline{C} + ABC$

C \ AB	0	1
00		**1**
01	**1**	
11	**1**	**1**
10		

Practice

$$\overline{A} + A\overline{B} + AB\overline{C}$$

	C	
AB	0	1
00	**1**	**1**
01	**1**	**1**
11	**1**	
10	**1**	**1**

Grouping the 1s

Grouping the 1s

CD AB	00	01	11	10
00	1	1		
01	1	1	1	1
11				
10		1	1	

CD AB	00	01	11	10
00	1			1
01	1	1		1
11	1	1		1
10	1		1	1

Determining the Minimum SOP Expression from the Map
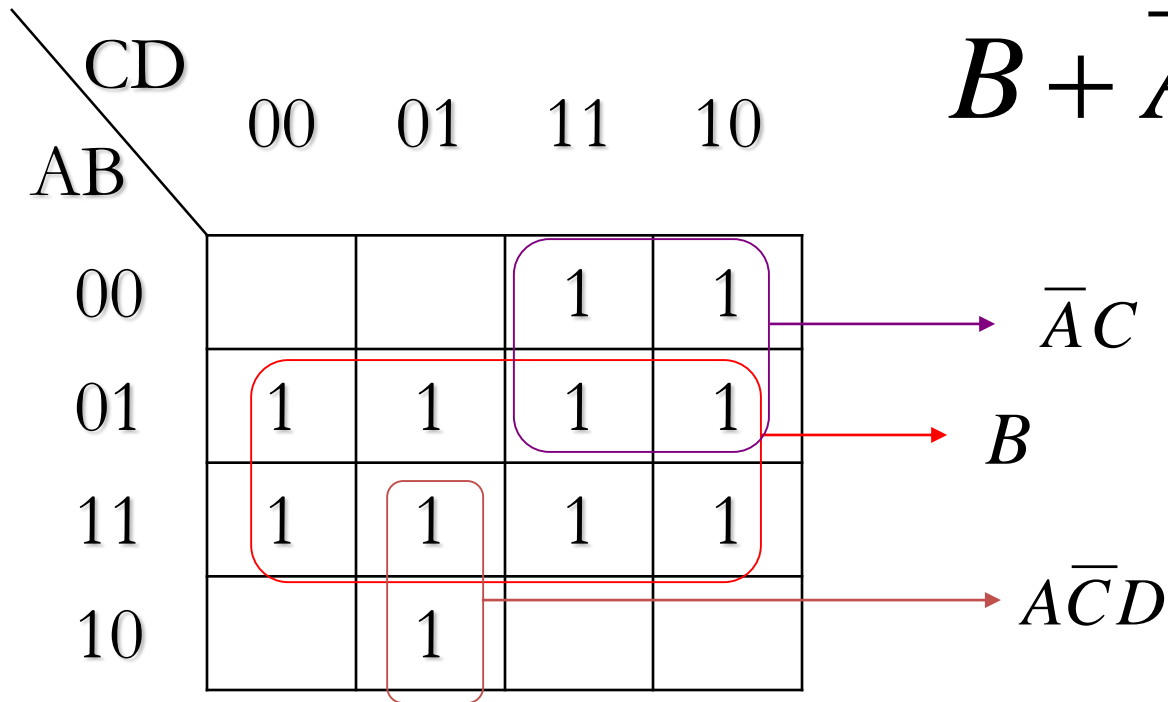
$$B + \overline{A}\,C + A\overline{C}D$$

Determining the Minimum SOP Expression

$$AB + BC + \overline{A}\,\overline{B}\,\overline{C}$$

$$\overline{B} + \overline{A}\,\overline{C} + AC$$

8

Determining the Minimum SOP Expression

CD AB	00	01	11	10
00	1	1		
01	1	1	1	1
11				
10		1	1	

$$\overline{A}B + \overline{A}\overline{C} + A\overline{B}D$$

CD AB	00	01	11	10
00	1			1
01	1	1		1
11	1	1		1
10	1		1	1

$$\overline{D} + A\overline{B}C + B\overline{C}$$

9

Mapping Directly from a Truth Table

$$\overline{A}\,\overline{B}\,\overline{C} + A\overline{B}\,\overline{C} + AB\overline{C} + ABC$$

I/P			O/P
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

C

AB	0	1
00	**1**	
01		
11	**1**	**1**
10	**1**	

AB+B'C'

"Don't Care" Conditions

- Sometimes a situation arises in which some input variable combinations are not allowed:
  - i.e., six invalid combinations: 1010, 1011, 1100, 1101, 1110, and 1111.
- Since these unallowed states will never occur in an application → they can be treated as "don't care" terms with respect to their effect on the output.
- The "don't care" terms can be used to advantage on the K-map (how? see the next).

"Don't Care" Conditions

(i.e., six invalid combinations: 1010, 1011, 1100, 1101, 1110, and 1111)

INPUTS				O/P
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	x
1	0	1	1	x
1	1	0	0	x
1	1	0	1	x
1	1	1	0	x
1	1	1	1	x

CD

AB	00	01	11	10
00				
01			1	
11	X	X	X	X
10	1	1	X	X

Without "don't care"

$$Y = A\overline{B}\,\overline{C} + \overline{A}BCD$$

With "don't care"

$$Y = A + BCD$$

12

Mapping a Standard POS

The expression:

$(A + B + C)(A + \overline{B} + C)(\overline{A} + \overline{B} + C)(\overline{A} + B + \overline{C})$

000   010   110   101

AB \ C	0	1
00	**0**	
01	**0**	
11	**0**	
10		**0**
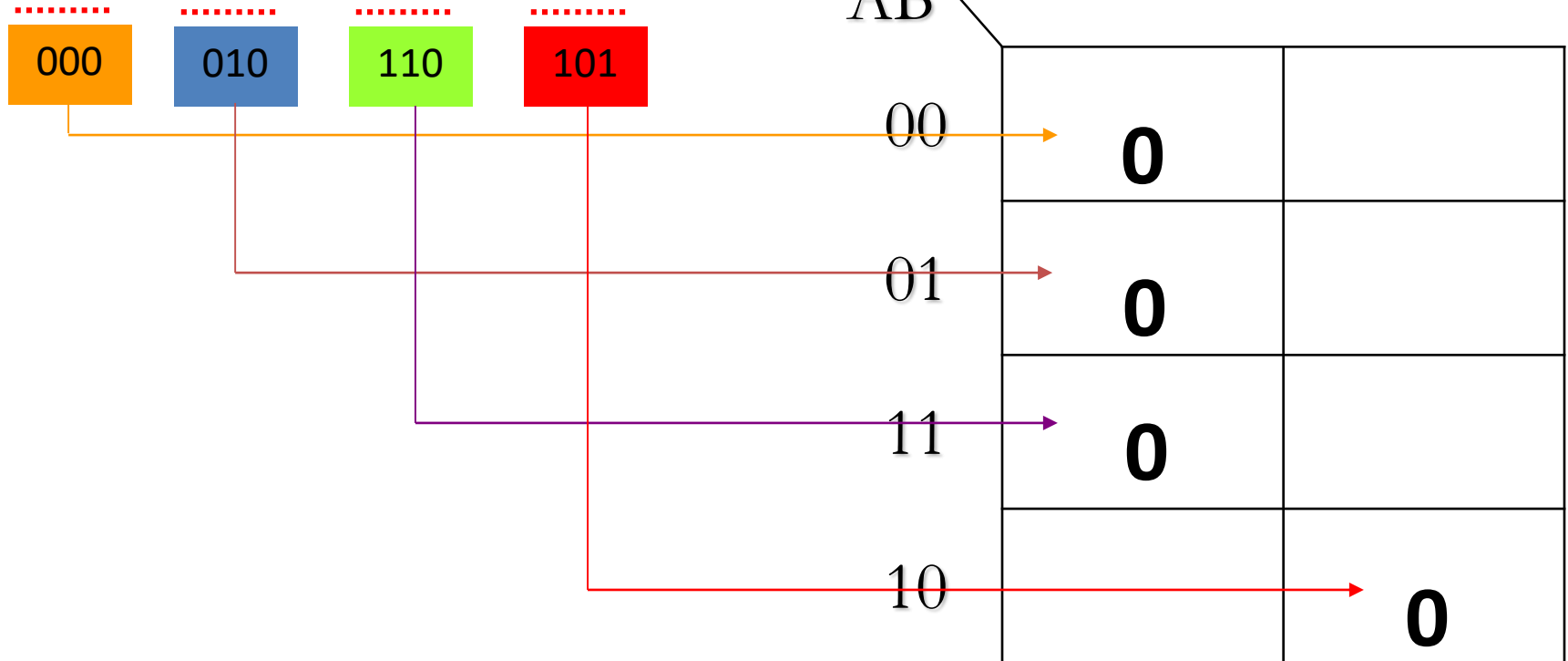
Mapping a Standard POS/SOP

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

$$(A+B+C)(A+B+\overline{C})(A+\overline{B}+C)(A+\overline{B}+\overline{C})(\overline{A}+\overline{B}+C)$$

POS: 000,001,010,011,110 → missing 100,111,101 : SOP

C

AB   0   1

A

$\overline{B}+C$

	0	**1**
00	**0**	**0**
01	**0**	**0**
11	**0**	**1**	AC
10	**1**	**1**	$A\overline{B}$
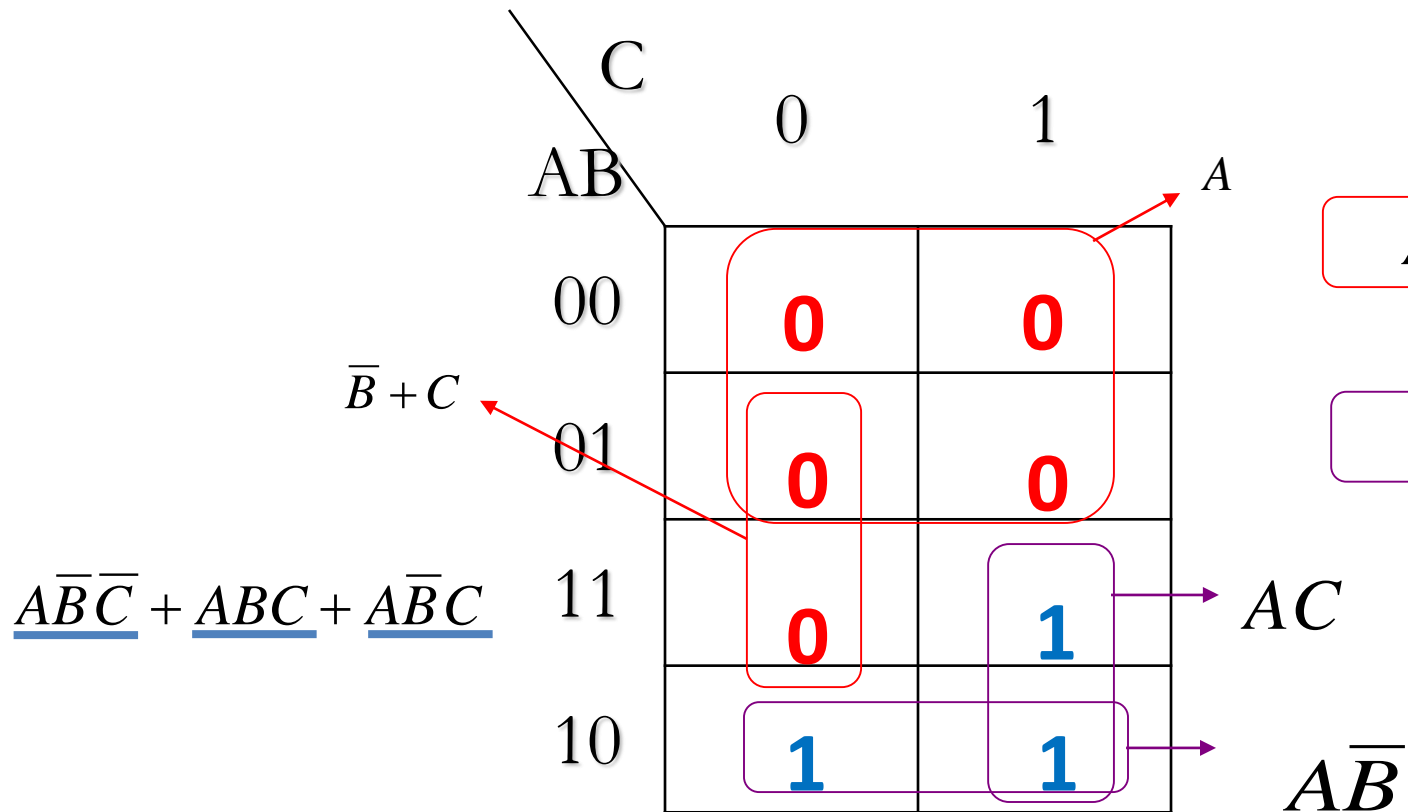
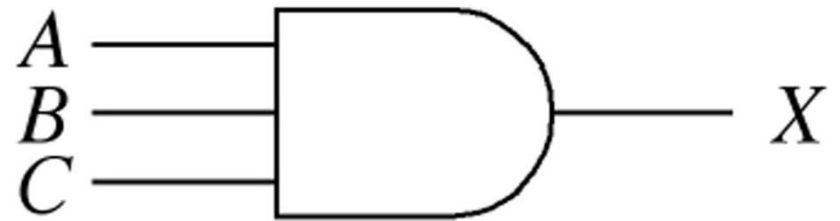$A\overline{B}\,\overline{C} + ABC + A\overline{B}C$

$A(\overline{B}+C)$

$A\overline{B} + AC$

Timing Analysis

- Determine the gate output for the input waveforms below.
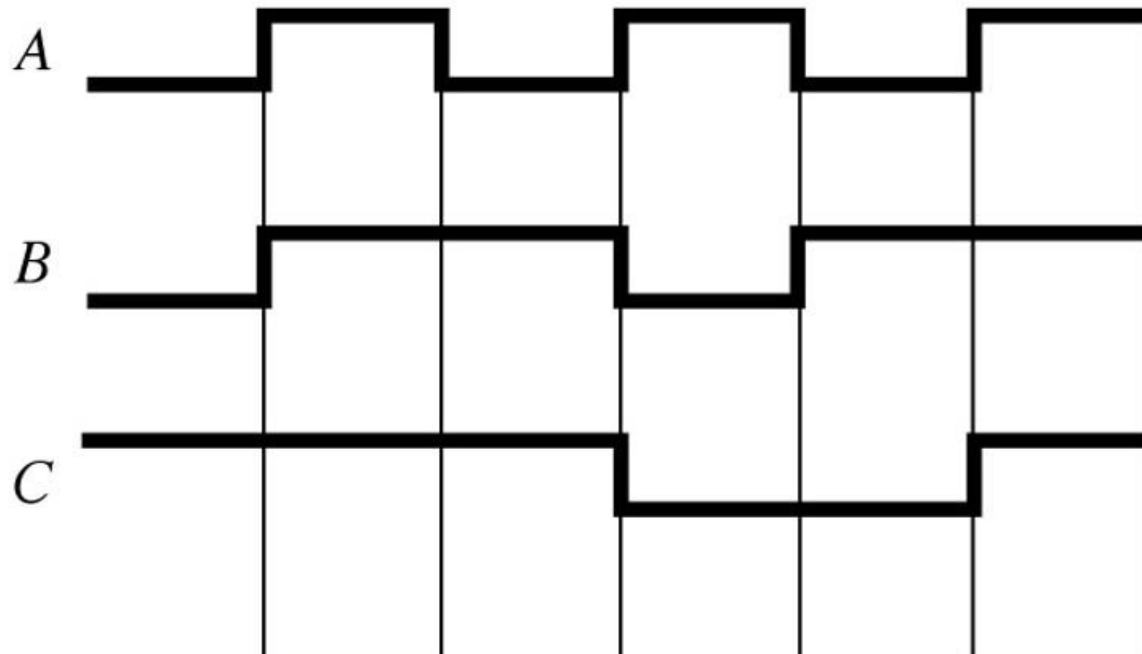
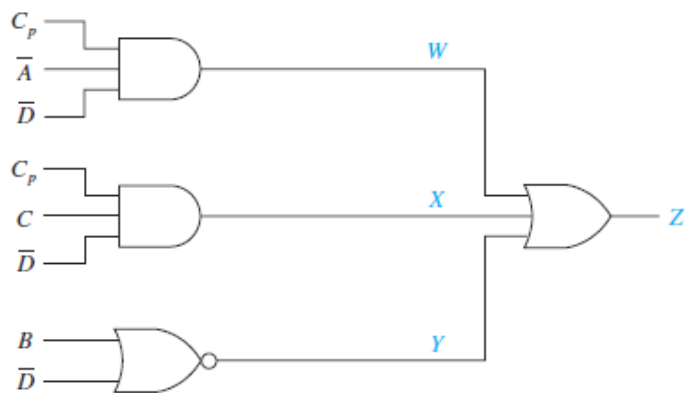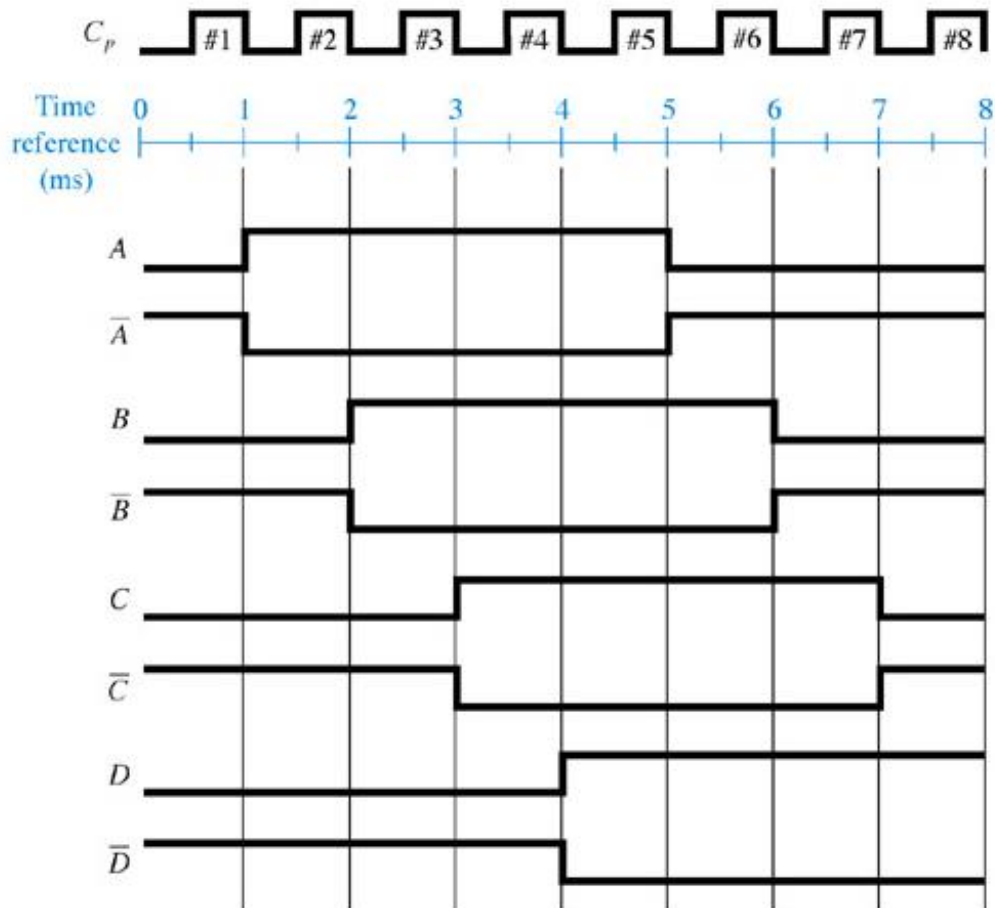Sketch the output waveforms for the circuit shown in Figure 3–58.

Figure 3–58

Simplification Using Boolean Algebra

1. $AB' + AB + BC$ $\quad = A(B'+B) + BC = A + BC$
2. $AB'D + AB'D'$ $\quad = AB'(D+D') = AB'$
3. $(A'+B)(A+B)$ $\quad = A'A + AB + A'B + BB = 0 + B(A+A') = B$
4. $ACD+A'BCD$ $\quad = CD(A+A'B) = CD(A+B)=ACD + BCD$
5. $AC'+ABC'$ $\quad = AC'(1+B) = AC'$
6. $A'B'CD' + A'B'C'D' = A'B'D'(C+C') = A'B'D'$
7. $A'D + ABD$ $\quad = D(A' + AB) = D(A'+B)$
8. $((A'+C)(B+D'))'$ $\quad = AC' + B'D$

> A note for K-map.
> 3. $(A'+B)(A+B)$: POS: F=B;
> 1. $AB' + AB + BC$: SOP: F= A+BC