Counters

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For your demo, wire color convention

Red → Power +

Black →Ground

Do not use Red and Black color of wires for other purpose. If this happens, demo mark will be deducted (-1 per each wrong color wire).

Introduction

Counters are used in many digital circuit applications. Such as Write memory address and Read memory address in FIFO. JK flip-flops can easily form the basis of a counter circuit. It should be easy to see that a JK flip-flop can easily form the basis of a counter circuit. In this lab, two counters will be implemented from JK flip-flops, one is synchronous counter and another is asynchronous counter.

Pre-lab

You will understand and implement synchronous and asynchronous counters using JK flip-flops. To complete this lab, your work must be checked by TAs during lab session and upload your report on the moddle. Failure to complete your demo will result in a reduction of the grade by 15% for the current lab.

1) J-K flip-flop is provided by 74109 logic gate IC. Figure 1 shows the internal architecture of 74109. **Study 74109 by yourself (explain the chip's functionality)**.

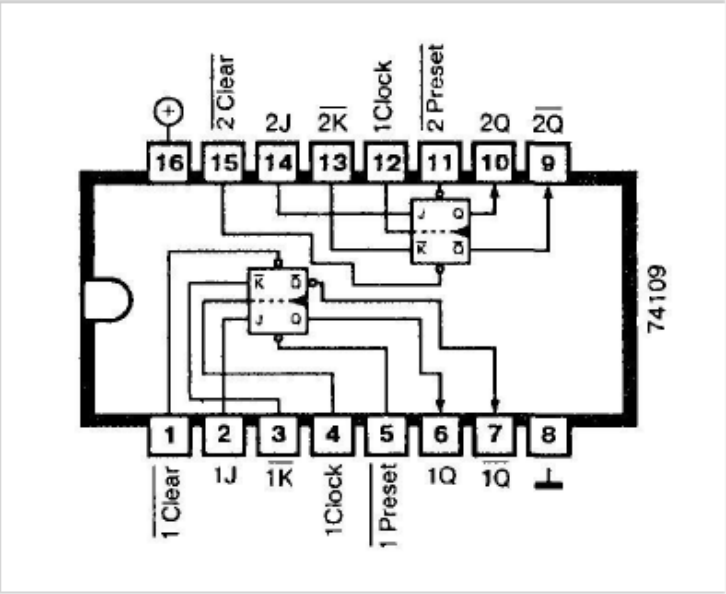
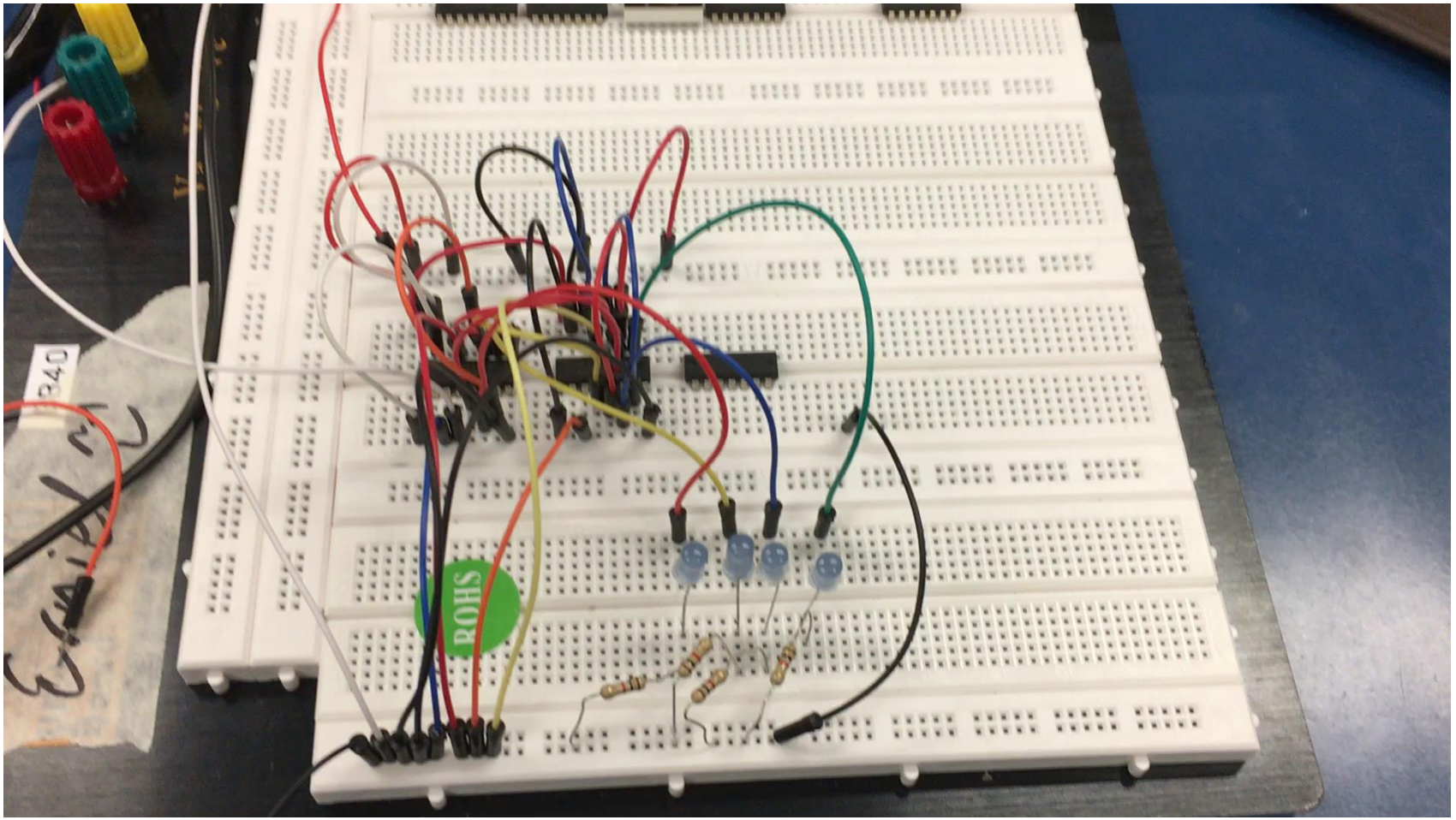
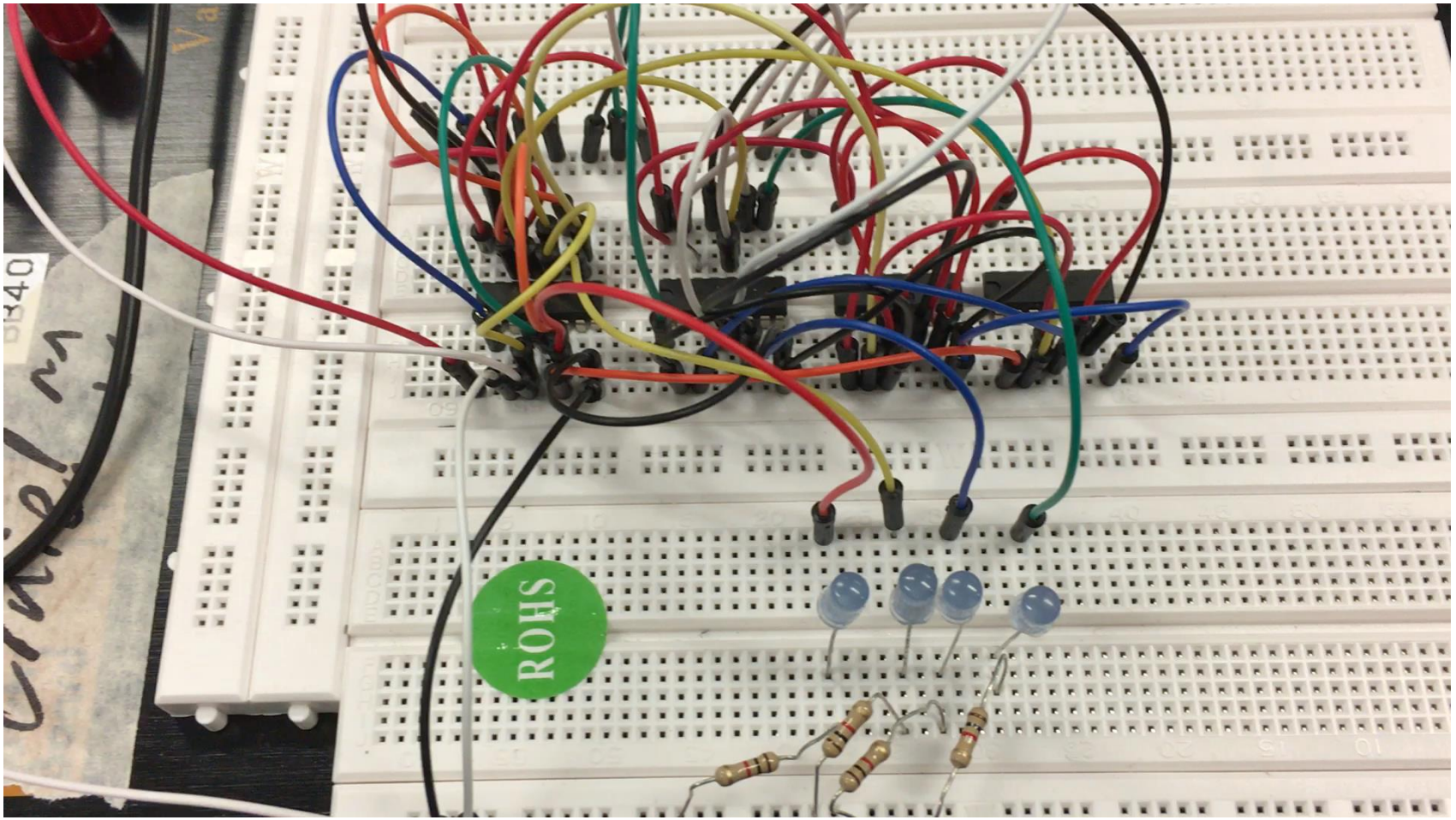


Figure 1: 74109 Internal Block Diagram

An asynchronous counter implementation



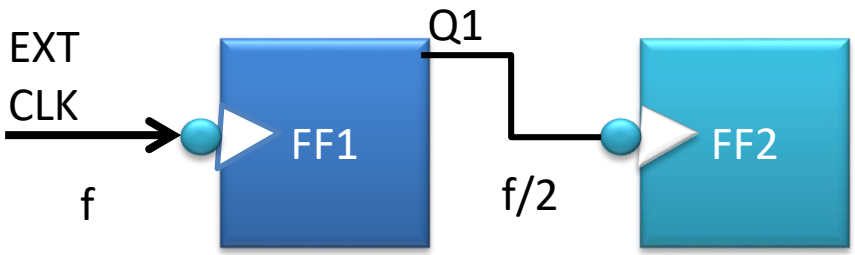
A synchronous counter implementation



Types of counter

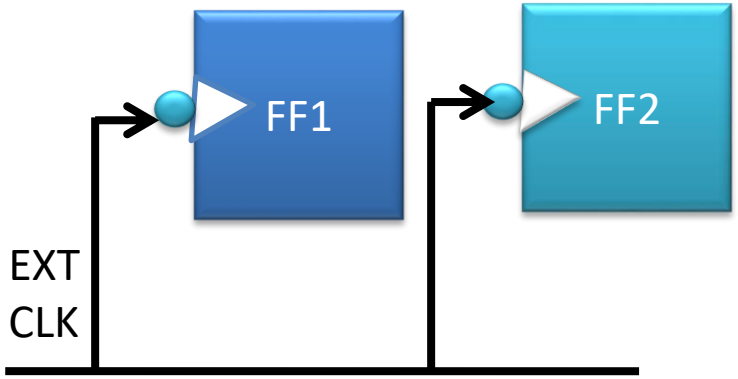
Asynchronous (Ripple)

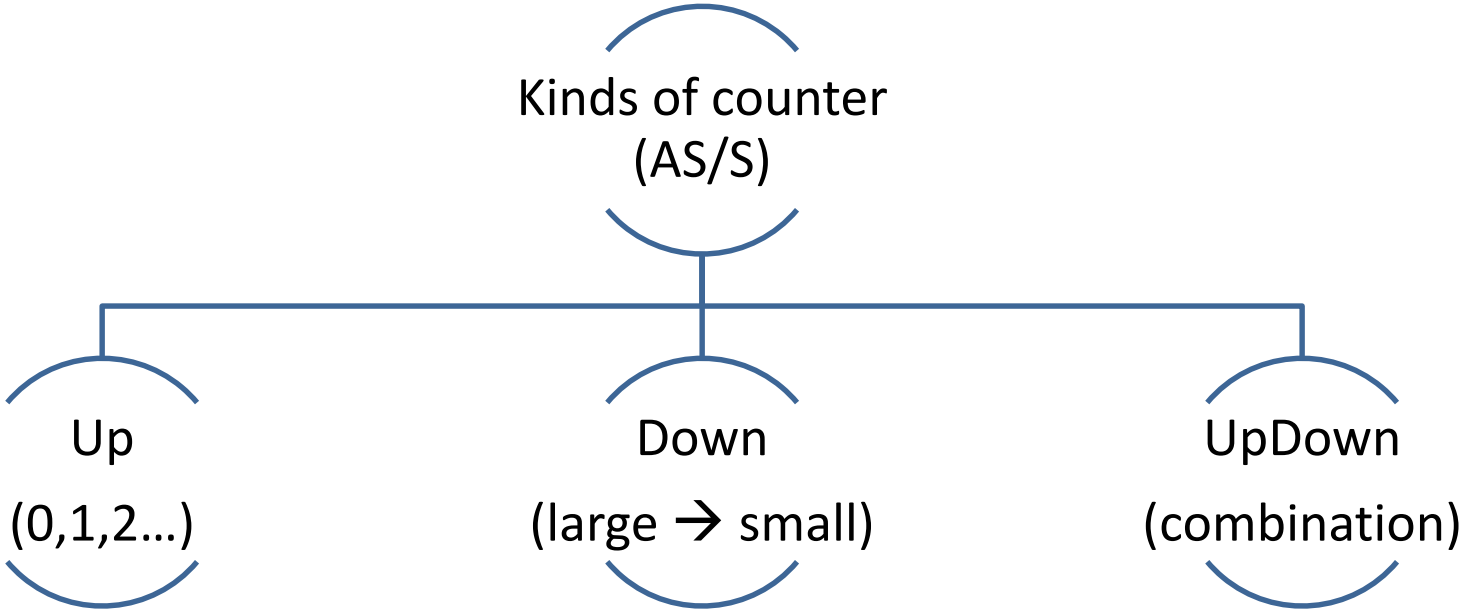
- An external CLK is applied to the first FF only
- Output of preceding FF is connected to the next FF's clk
- FFs are not clocked simultaneously
- Simple circuits
- Slow speed due to propagation delay
- A Freq divided by 2 circuit configuration



Synchronous

- All FFs are receiving external CLK simultaneously
- Complicate circuits
- Fast speed





In lab 7, we will implement

Up-counters both Asynchronous and Synchronous types

Asynchronous counter implementations

Steps

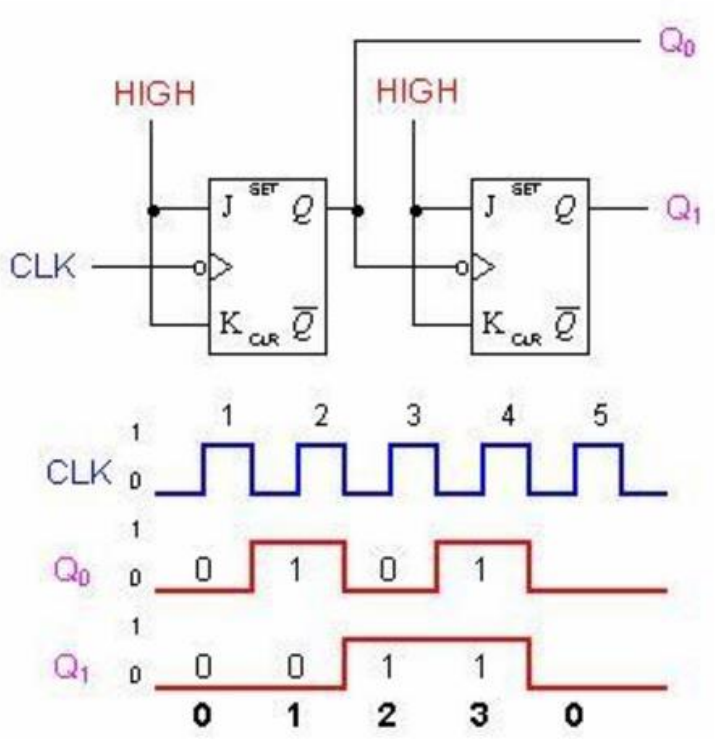
I. Decide the number of FFs (based on the counting limit) and a kind of FF
   - #: 4 bit=16 mod --> 4 FFs
   - Type: JK FF

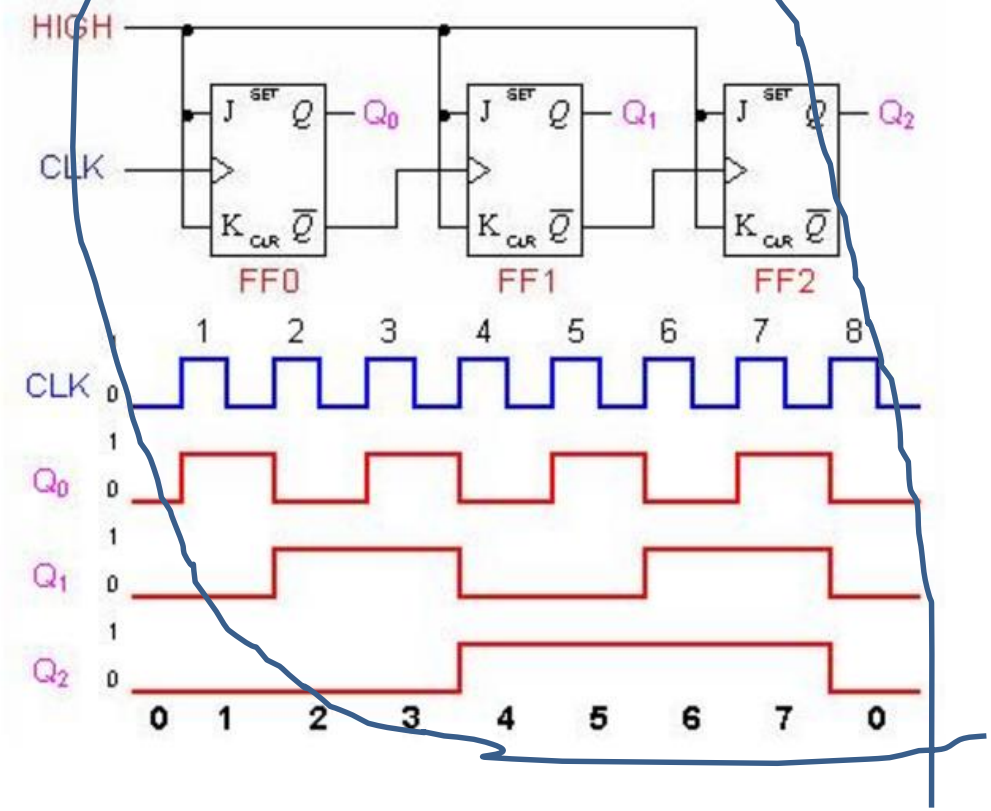
II. Draw the circuit: Very simple
   - Just feed preceding FFs output to the next FF clk
   - Use the frequency “divided by 2” property of FF

An asynchronous “up” counter → falling edge trigger: several ways to implement

Negative-edge triggered flip-flops, connecting the clock inputs to the Q outputs of the preceding flip-flops.

Positive-edge triggered flip-flops
Connecting the clock inputs of positive-edge triggered J-K flip-flops to the Q’ outputs of the preceding flip-flops.





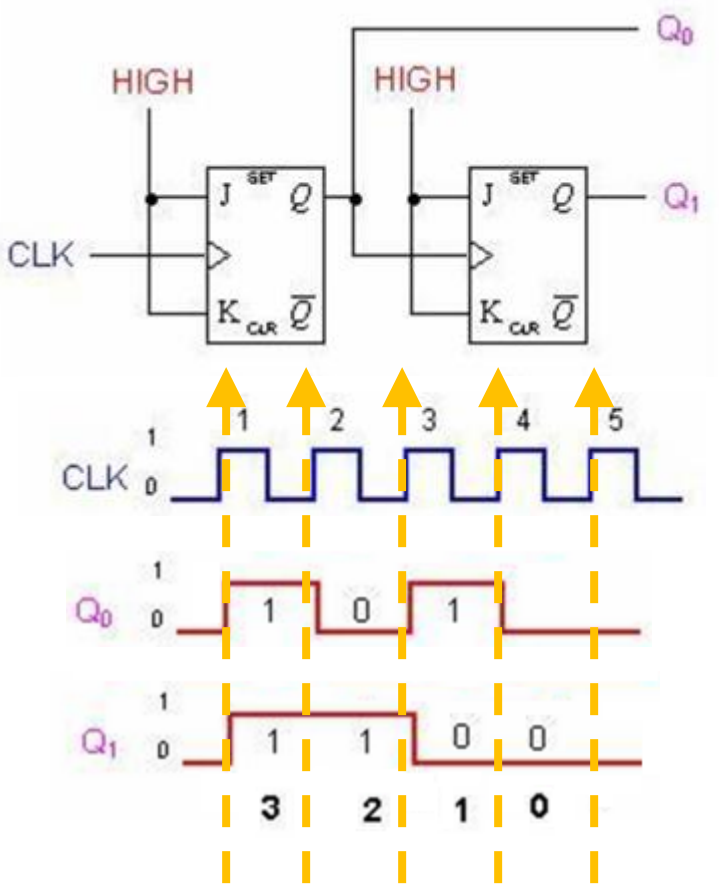
A two-bit asynchronous counter

A three-bit asynchronous binary counter

https://www.ee.usyd.edu.au/tutorials/digital_tutorial/part2/counter02.html

A side bar: Asynchronous DOWN counters?

- Positive edge triggering



Synchronous counter

Steps

I. Decide the number of FFs (based on the states) and a kind of FF
   - i.e., 3 bits, JK FF

II. Excitation table of FF (relates Q_t and Q_{t+1})
   - Next slide

III. State diagram and circuit excitation table

IV. Obtain simplified equations using K map

V. Draw the logic diagram

JK flip-flops

TT

Inputs		Output
J	K	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	$\sim Q_t$

Excitation table of JK FF

Status		J	K
Present Q_t	Next Q_{t+1}		
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

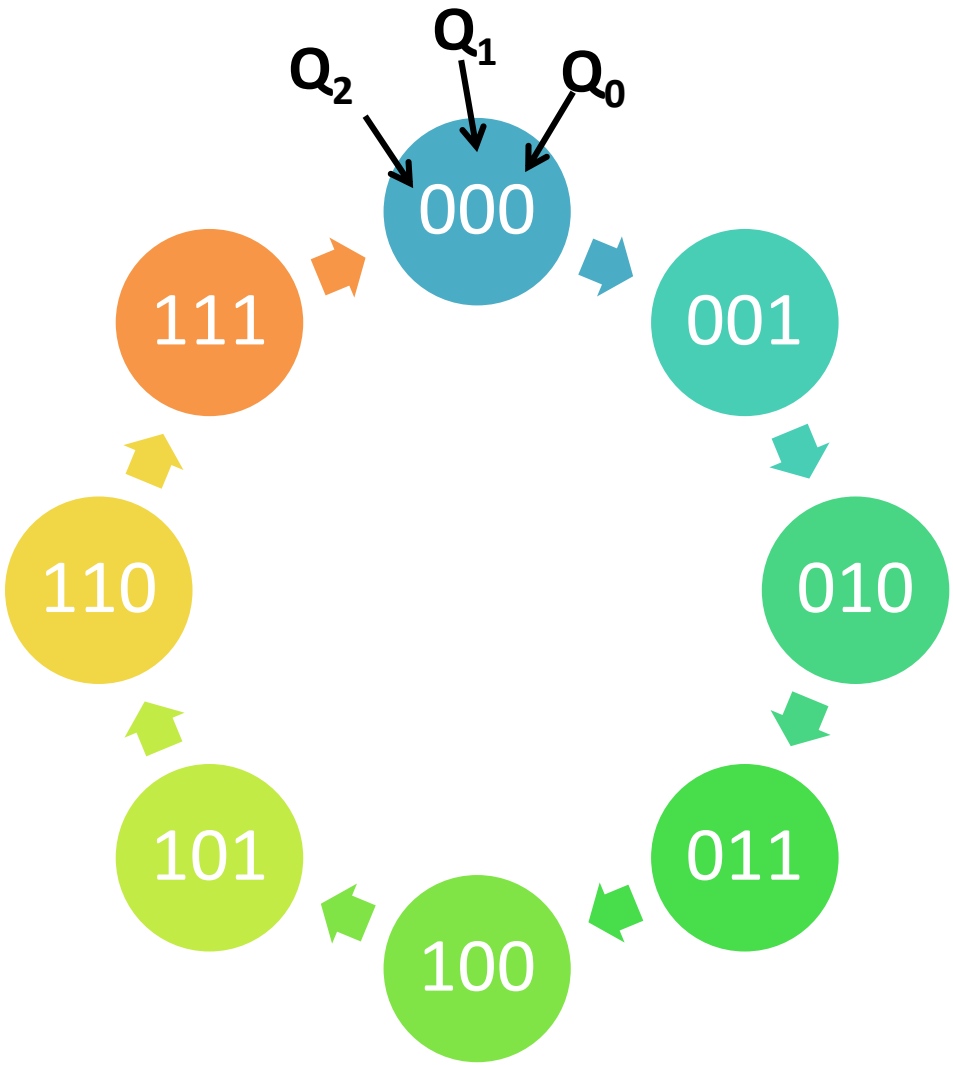
Excitation table of T FF

Status		T
Present Q_t	Next Q_{t+1}	
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of D FF

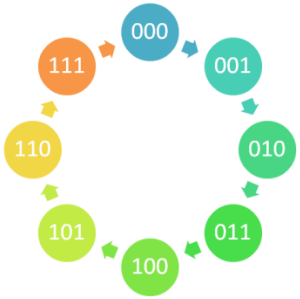
Status		D
Present Q_t	Next Q_{t+1}	
0	0	0
0	1	1
1	0	0
1	1	1

III-1. State diagram (3 bits)



III-2. circuit excitation table

Status		J	K
Present Q_t	Next Q_{t+1}		
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0



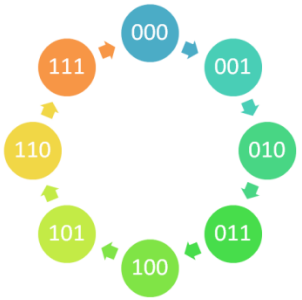
Present → Next

Q_2	Q_1	Q_0	Q_2^*	Q_1^*	Q_0^*
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

J_2	K_2
0	X
0	X
0	X
1	X
X	0
X	0
X	0
X	1

III-2. circuit excitation table

Status		J	K
Present Q_t	Next Q_{t+1}		
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0



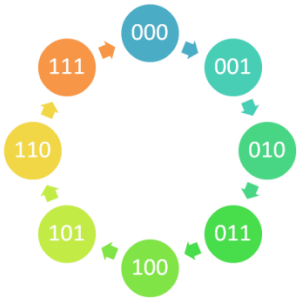
Present → Next

Q_2	Q_1	Q_0	Q_2^*	Q_1^*	Q_0^*
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

J_1	K_1
0	X
1	X
X	0
X	1
0	X
1	X
X	0
X	1

III-2. circuit excitation table

Status		J	K
Present Q_t	Next Q_{t+1}		
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0



Present → Next

Q_2	Q_1	Q_0	Q_2^*	Q_1^*	Q_0^*
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

J_0	K_0
1	X
X	1
1	X
X	1
1	X
X	1
1	X
X	1

IV. Simplified equations using K map

Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	X	0	X	1	X
0	0	1	0	X	1	X	X	1
0	1	0	0	X	X	0	1	X
0	1	1	1	X	X	1	X	1
1	0	0	X	0	0	X	1	X
1	0	1	X	0	1	X	X	1
1	1	0	X	0	X	0	1	X
1	1	1	X	1	X	1	X	1

For J_2

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_2=Q_1Q_0$

For K_2

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	X	X
1	0	0	1	0

$K_2=Q_1Q_0$

IV. Simplified equations using K map

Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	X	0	X	1	X
0	0	1	0	X	1	X	X	1
0	1	0	0	X	X	0	1	X
0	1	1	1	X	X	1	X	1
1	0	0	X	0	0	X	1	X
1	0	1	X	0	1	X	X	1
1	1	0	X	0	X	0	1	X
1	1	1	X	1	X	1	X	1

For J_1

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	X	X
1	0	1	X	X

For K_1

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	1	0
1	X	X	1	0

$J_1=Q_0$

$K_1=Q_0$

IV. Simplified equations using K map

Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	X	0	X	1	X
0	0	1	0	X	1	X	X	1
0	1	0	0	X	X	0	1	X
0	1	1	1	X	X	1	X	1
1	0	0	X	0	0	X	1	X
1	0	1	X	0	1	X	X	1
1	1	0	X	0	X	0	1	X
1	1	1	X	1	X	1	X	1

For J_0

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$J_0=1$

For K_0

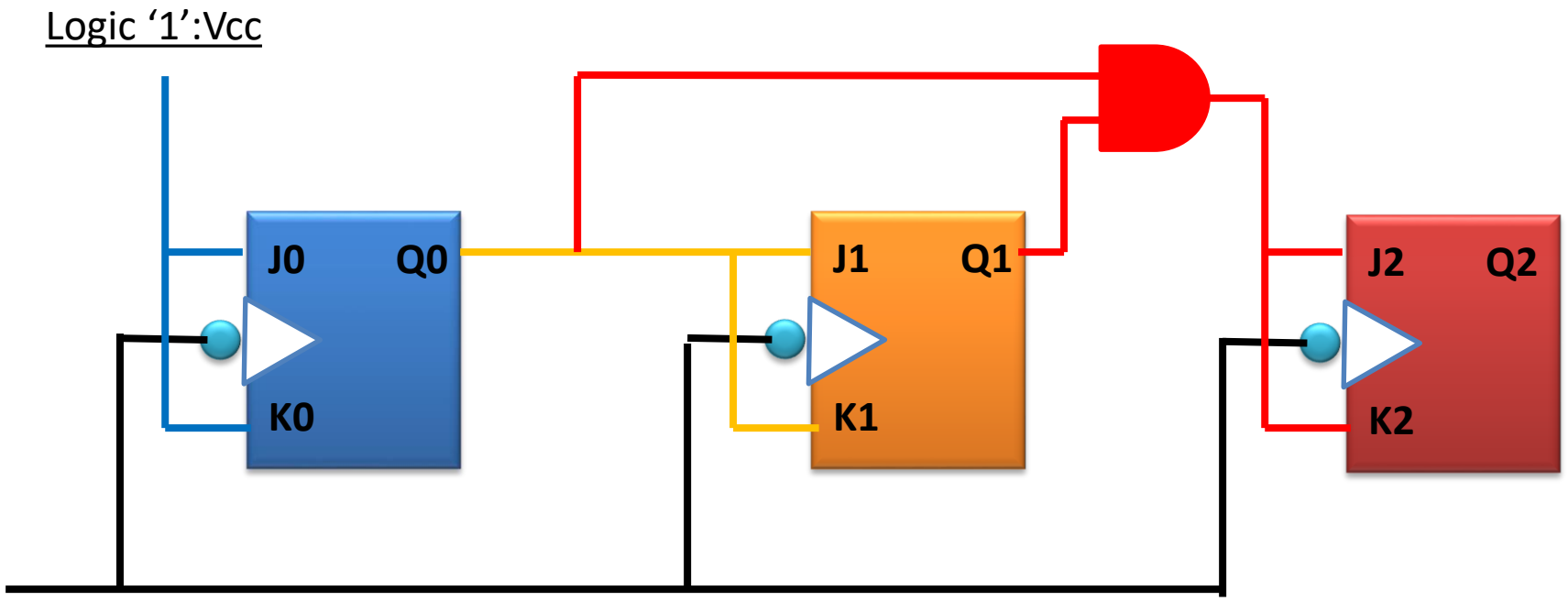
Q_2 \ Q_1Q_0	00	01	11	10
0	X	1	1	X
1	X	1	1	X

$K_0=1$

V. Draw a diagram

$J_2=Q_1Q_0$
$J_1=Q_0$
$J_0=1$

$K_2=Q_1Q_0$
$K_1=Q_0$
$K_0=1$



The synchronous mod 8 up counter