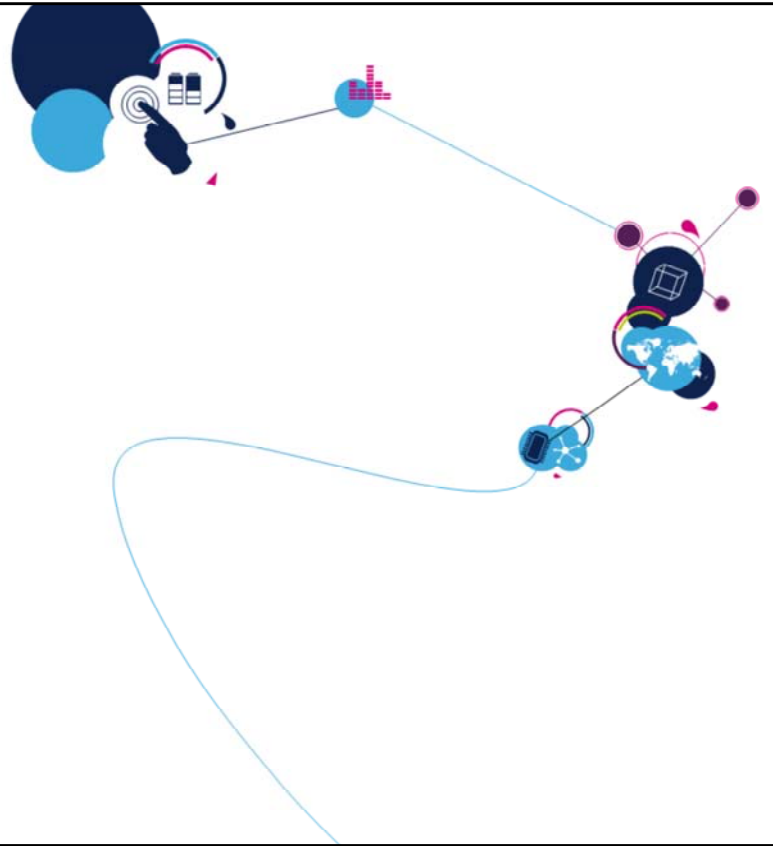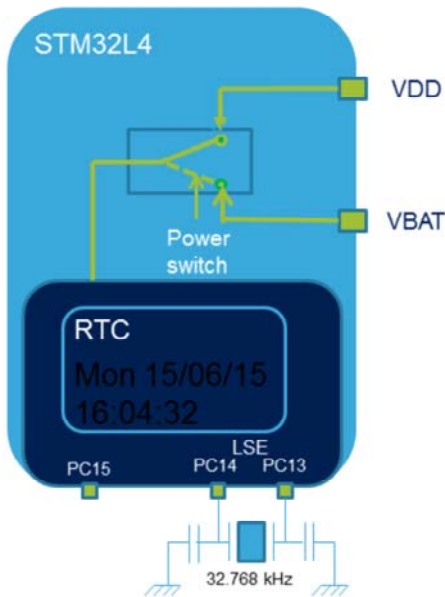# STM32L4 – RTC

Real-time clock

Revision 2.1

Hello, and welcome to this presentation of the STM32 Real-Time Clock. It covers the main features of this peripheral, which is used to provide a very accurate time base.

- The RTC provides an ultra-low-power hardware calendar with alarms, in all low-power modes
- Belongs to the Battery Backup Domain, so it is kept functional when the main supply is off
- 128 bytes of backup registers, erased on tamper detection

Application benefits

- Ultra-low power: 300 nA at 1.8 V
- Hardware BCD calendar to reduce software load
- Ultra-low-power tamper detection with filtering

The RTC peripheral features an ultra-low power calendar with alarms, which run in all low-power modes.
Additionally, when it is clocked by the low-speed external oscillator (LSE) at 32.768 kHz, the RTC is functional even when the main supply is off and when the VBAT domain is supplied by a backup battery.
The RTC embeds 128 bytes of backup registers, used to preserve data when the main supply is off. These backup registers can be used to store secure data, as they are erased when a tamper event is detected on the tamper pins.
The RTC consumes only 300 nA at 1.8 V , including the LSE power consumption. The hardware calendar is provided in binary-coded decimal (BCD) format to reduce software load, particularly when the date and time must be displayed. The anti-tamper circuitry includes ultra-low-power digital filtering, avoiding false tamper detections.

- Sub-seconds, seconds, minutes, hours, week day, date, month, year in BCD format
- "On the fly" programmable daylight savings compensation
- Two programmable alarms with wakeup interrupt function
- A periodic flag with programmable resolution, triggering wakeup interrupt
- A reference clock source (50 or 60 Hz) can be used to update the calendar
- Digital calibration circuit to achieve 0.95 ppm accuracy
- Time-stamp function for event saving with sub-second precision (1 event)
- 128 bytes of backup registers, which are reset upon tamper detection
- 3 tamper pins with filtering, functional in VBAT mode

The key features of the RTC are:
Seconds, minutes, hours, week day, date, month, and year, provided in binary-coded decimal format. Sub-seconds are provided in binary format.
Add or remove one hour on the fly to the calendar, in order to manage daylight savings.
Two programmable alarms, which can wake up the microprocessor from all low-power modes.
An embedded auto-reload timer, which can be used to generate a periodic flag or interrupt with wakeup capability. The resolution of this timer is programmable.
The calendar can be calibrated thanks to a reference clock source which is the mains at 50 or 60 Hz.
A digital calibration circuit allowing compensation of the crystal accuracy, with 0.95 ppm resolution.
A timestamp function to save calendar contents in timestamp registers, depending on an external event.
128 bytes of backup registers, split into thirty-two 32-bit

backup registers. These registers are preserved in all low-power modes and in VBAT mode, and are erased when a tamper detection event occurs on any one of the three tamper pins. The 3 tamper pins are available in VBAT mode.

Block diagram
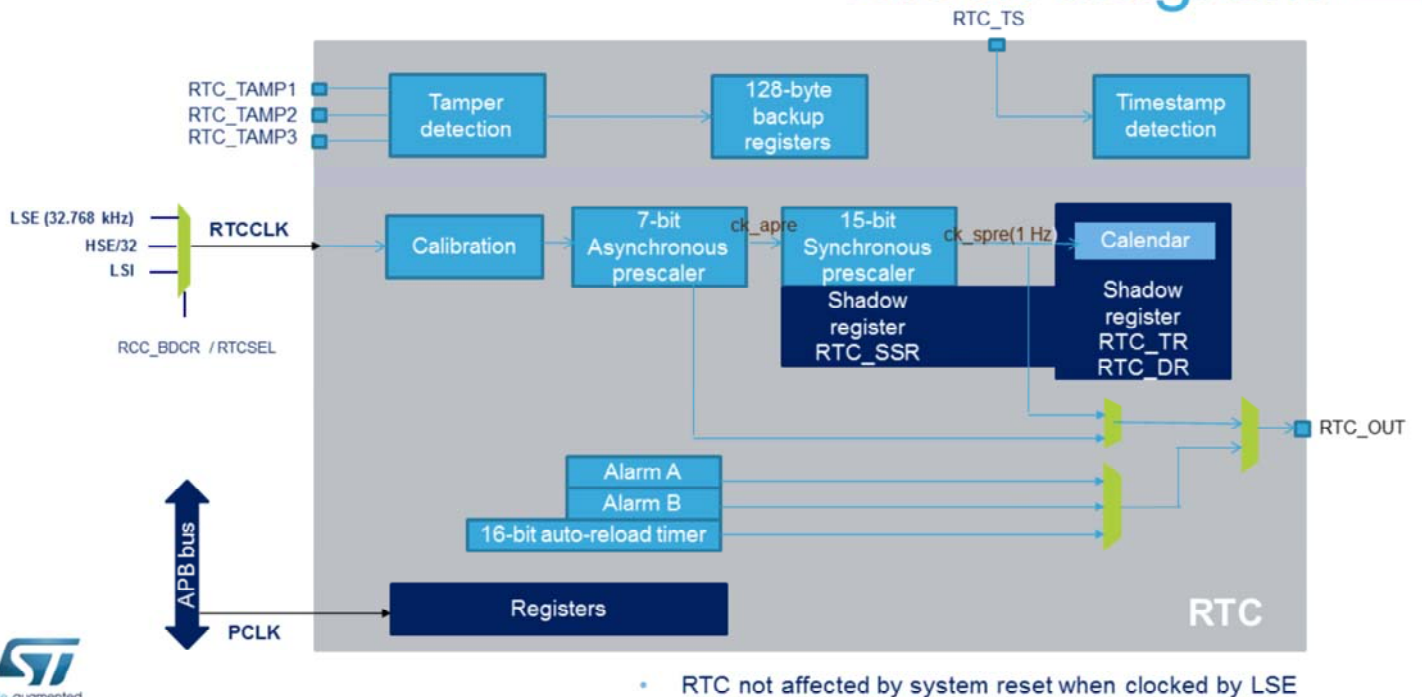
Here is the RTC block diagram. The RTC has two clock sources: the RTC clock (RTCCLK) is used for the RTC timer counter, and the APB clock is used for RTC register read and write accesses. The RTC clock can use either the high-speed external oscillator (HSE), divided by 32, the low-speed external oscillator (LSE), or the low-speed internal oscillator (LSI). To be functional in Stop0, Stop 1, Stop 2, or Standby mode, the RTC clock must use the LSE or LSI. To be functional in Shutdown or VBAT mode, the RTC clock must use the LSE.

The RTC clock is first divided by a 7-bit programmable asynchronous prescaler, which provides the ck_apre clock. Most of the RTC is clocked at the ck_apre frequency, so, in order to reduce power consumption, it is recommended to set a high asynchronous division value. The default value is 128.

Then, a 15-bit programmable synchronous prescaler

provides the ck_spre clock. Ck_spre must be 1 Hz in order to update the time and date BCD registers in 1 second increments. The sub-second register resolution is defined by the ck_apre frequency. By default, it is 256 Hz. The SSR register resolution is increased by reducing the asynchronous prescaler value. The asynchronous prescaler can also be bypassed; in this case the sub-second register resolution is defined by the RTC clock frequency.

RTC register write protection

Secure RTC initialization

- The RTC registers are write-protected to avoid possible parasitic write accesses
  - Disable Backup Domain (DBP) bit must be set in the Power Controller control register (PWR_CR) to enable RTC write access
  - A Key must be written in RTC write protection register (RTC_WPR) register

- Specific software sequence to enter RTC initialization mode
 - Used for calendar registers and prescaler initialization

The RTC is initialized using a secure method.
The RTC registers are write protected to avoid any possible parasitic write accesses. First, the Disable Backup Domain Protection bit must be set in the Power Controller control register in order to enable RTC write accesses. Then, a specific sequence must be written in the RTC write protection register.
Initialization mode must be entered in order to change the clock prescalers values or the calendar value.

Active in all low-power modes, VBAT and reset

- Initialization done through shadow registers: Time and Date registers

Actual registers

Date				Time			
Day	Month	Date	Year	HH	MM	SS	SSR

| DR | TR | SSR |
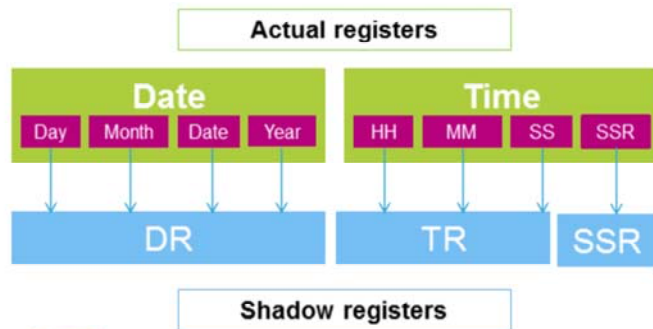
Shadow registers

- Reading the calendar:
  - BYPSHAD = 0: Read shadow registers
    - Delay up to 2 RTCCLK cycles to update shadow registers when exiting Stop/Standby/Shutdown modes.
    - DR update is frozen after reading TR, and unfrozen when DR is read.
    - TR and DR update is frozen after reading SSR, and unfrozen when DR is read.
  - BYPSHAD = 1: Bypass shadow registers
    - Calendar read directly accesses the calendar counters
    - Software must read all calendar registers twice and compare the results to ensure that the data are coherent and correct.

The RTC calendar keeps running in all low-power modes, in VBAT mode, and during reset.

Initialization of the Time and Date registers is performed through their shadow registers, which are in the APB clock domain. The Sub-second register cannot be initialized.

The calendar Sub-second, Time, and Date registers content can be read in two different modes.

When the Bypass Shadow Registers control bit is cleared, the shadow registers are read. The advantage of this mode is that it guarantees that all three registers are consistent: when the Time register is read, the Date register is frozen until it is read. When the Sub second register is read, the Time and Date registers are frozen until the Date register is read. The disadvantage of this mode is that when exiting Stop, Standby or Shutdown mode, the software must wait for a synchronization delay to ensure that the shadow registers are updated with the last calendar register values. This synchronization delay can be up to two RTC clock periods.

When the Bypass Shadow Registers control bit is set, the actual calendar registers are read directly. The advantage of this mode is that there is no need to wait for the synchronization delay. The disadvantage is that the read values can be false or not consistent due to synchronization issues, so they must be read twice and compared with previous read values to ensure they are correct and coherent.

RTC calendar features

- "Daylight savings" is managed by automatic addition or subtraction of 1 hour

- Calendar synchronization up to 1 s by adding/subtracting an offset with the sub-second resolution => Allows synchronization with remote clock

- Reference clock detection: A more precise second-source clock (50 or 60 Hz mains) can be used to enhance the long-term precision of the calendar:
  - The reference clock is automatically detected and used to update the calendar
  - The LSE clock is automatically used to update the calendar whenever the reference clock becomes unavailable

- Timestamp
  - Calendar value is saved in timestamp registers on external I/O event
  - Internal timestamp detection when a switch to VBAT occurs.

This slide presents the main calendar features.
Daylight savings can be managed by software, with automatic 1 hour addition or subtraction.
It is possible to synchronize the RTC clock to a remote clock by adding or subtracting an offset to the Sub-second register on the fly, with ck_apre clock resolution. This feature is commonly used in RF applications.
A reference clock, mains at 50 or 60 Hz, can be used to enhance long-term calendar precision. The reference clock is automatically detected and used to update the calendar when it is present. When the reference clock is not available, the LSE clock is automatically used to update the calendar. This feature is not available in Standby, Shutdown, and VBAT modes.
A timestamp function is available: the calendar values, Sub-second, Time, and Date registers are saved in timestamp registers when an event occurs on the timestamp I/O. A timestamp event can also occur when a switch to VBAT

occurs.

Smooth digital calibration

Crystal inaccuracy compensation

- Consists in masking/adding N (configurable) 32 kHz clock pulses, fairly well distributed in a configurable window

- Calibration value can be changed on the fly

- A 1 Hz output is provided to measure the crystal frequency and the calibration result

Calibration window	Accuracy	Total range
8 s	± 1.91 ppm	[0 ± 480 ppm]
16 s	± 0.95 ppm	[0 ± 480 ppm]
32 s	± 0.48 ppm	[0 ± 480 ppm]

The digital calibration is used to compensate crystal inaccuracy and accuracy variation with temperature and aging.
It consists in masking or adding a programmable number of RTC clock cycles, fairly well distributed in a configurable window. The calibration value can be changed on the fly, depending on detected temperature changes for instance. A 1 Hz calibration output signal is provided to measure the crystal frequency before and after applying the calibration value.
The accuracy shown here is the resolution of the digital calibration. The calibration window size is configurable, between 8, 16, and 32 seconds. For a 32 s calibration window, the accuracy is plus or minus 0.48 ppm. The total correction range is from -480 to 480 ppm. The accuracy resolution scales with the calibration window size. Final accuracy in the application will depend on the crystal parameter precision, temperature detection precision, how often the software calibration procedure is launched, etc.
In order to reach the precision of the calibration window, the measurement window must be a multiple of the calibration window.

RTC programmable alarm

2 flexible alarms based on calendar value

- The Alarm flags are set if the calendar sub-seconds, seconds, minutes, hours or date match the value programmed in the alarm registers

- 2 alarms, which exit the device from all low-power modes

- Alarm event can also be routed to the specific output pin RTC_OUT, with configurable polarity

- Calendar sub-second, seconds, minutes, hours or date fields can be independently selected (masked or not masked)
  - Masks allow configuration of periodic alarm interrupts

The RTC embeds two flexible alarms, based on comparison with the calendar value. The alarm flags are set if the calendar sub-seconds, seconds, minutes, hours or date match the value programmed in the alarm registers.
The alarms events can wake up the device from all low-power modes.
The alarms event can also be routed to the specific output pin RTC_OUT, with configurable polarity.
The calendar alarm sub-second, seconds, minutes, hours or date fields can be independently masked or not masked for the comparison. When the masks are used, periodic alarms are generated.

Periodic auto-wakeup

Flexible periodic wakeup interrupt

- The periodic wakeup flag is generated by a 16-bit programmable binary auto-reload down counter (can be extended to 17 bits)

- Able to exit the device from Stop/Standby/Shutdown modes

Wakeup timer (WUT) clock	Wakeup period	Resolution
RTCCLK divided by 2, 4, 8, 16	From 122 µs to 32 s when RTCCLK = 32.768 kHz	Down to 61 µs
ck_spre	From 1 s to 36 hours when ck_spre = 1 Hz	1s

In addition to the calendar and alarms, another 16-bit auto-reload counter can generate periodic events with wakeup from low-power modes capability. This counter cannot be read.

Depending on the software configuration, the wakeup timer clock can be the RTC clock divided by 2, 4, 8 or 16, or the output of the synchronous prescaler. With the divided RTC clock, the wakeup period can be from 122 microseconds to 32 seconds when RTC clock frequency is 32.768 kHz. The resolution is down to 61 microseconds in this case. With the ck_spre clock, the wakeup period can be from 1 second to 36 hours when the ck_spre clock is at 1 Hz.

Tamper detection

Ultra-low power anti-tamper circuitry
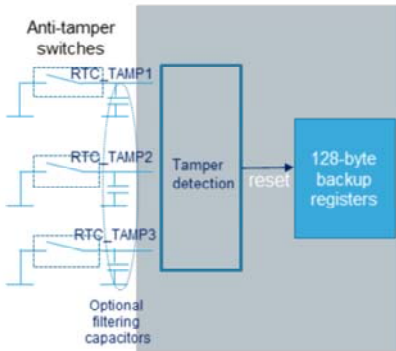
- 3 tamper pins and events, available in VBAT mode

- Configurable active edge or level for each event

- Reset of backup registers when a tamper event is detected

- Tamper can generate a timestamp event

The RTC embeds ultra-low-power tamper detection circuitry. The purpose is to detect physical tampering in a secure application, and to automatically erase sensitive data in case of intrusion.

3 tamper pins and events are supported, and are functional in all low-power modes and in VBAT mode.

The detection can be edge- or level-triggered, and the active edge or level is configurable for each event.

Backup register contents are erased when a tamper event is detected.

A tamper event can generate a timestamp event.

Tamper detection

Safe and ultra-low-power tamper detection with filtering

- Configurable use of I/O pull-up resistor to detect anti-tamper switch open state

- Configurable pre-charging pulse to support different capacitance values
  - 1, 2, 4 or 8 cycles

- Configurable filter
  - Sampling rate: 128, 64, 32, 16, 8, 4, 2, or 1 Hz
  - Number of consecutive identical events before issuing an interrupt to wake up the MCU: 1, 2, 4, or 8

The tamper detection circuit includes an ultra-low power digital filter. The internal I/O pull-up can be used to detect the anti-tamper switch state.
The I/O pull-up is applied only during the pre-charging pulse in order to avoid any consumption if the tamper pin is at a low level. The pre-charging pulse duration is configurable to support different capacitance values, and can be 1, 2, 4 or 8 RTC clock cycles. The pin level is sampled at the end of the pre-charging pulse.
A filter can be applied to the tamper pins. It consists of detecting a given number of consecutive identical events before issuing an interrupt to wake up the device. This number is configurable and can be 1, 2, 4 or 8 events, at a programmable sampling rate from 1 Hz to 128 Hz.

Tamper detection - signals
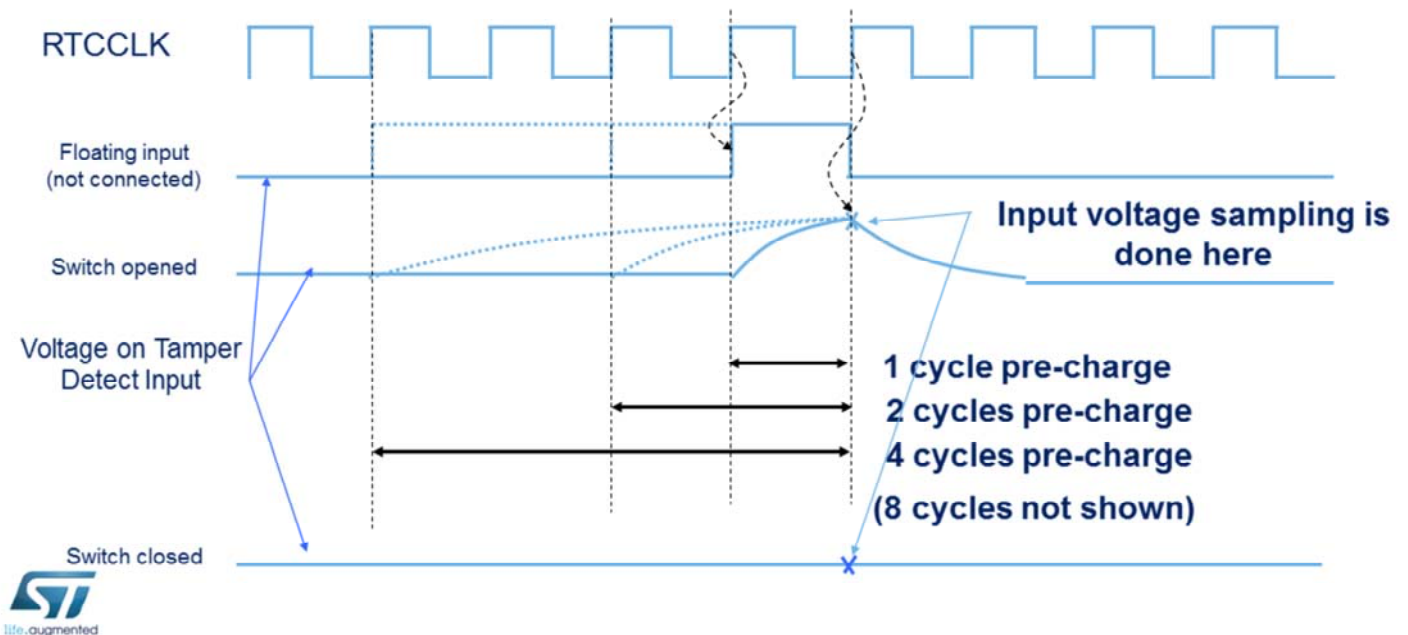
This figure illustrates tamper detection using the internal pull-up. The internal pull-up can be applied for 1, 2, 4 or 8 cycles.
If the switch is opened, the level is pulled-up by the resistor.
If the switch is closed, the level remains low.
The input voltage is sampled at the end of the pre-charge pulse.

Tamper detection

- Tamper detection can generate interrupts or trigger events, and can benefit from digital filtering
    - Interrupts can be enabled/disabled for each event
    - Backup registers erase is configurable for each event
    - Hardware trigger to the low-power timers is configurable for each event

The tamper detection circuitry can also be used to generate interrupts or trigger events. Each tamper interrupt can be individually enabled or disabled. Each tamper event can be individually configured to erase the backup registers or not. Each tamper event can be individually configured to generate a hardware trigger to low-power timers. This takes advantage of the digital filtering present on these I/Os for interrupt or trigger generation.

Interrupt event	Description
Alarm A	Set when the calendar value matches the Alarm A value
Alarm B	Set when the calendar value matches the Alarm B value
Wake-up timer	Set when the wakeup auto-reload timer reaches 0
Timestamp	Set when a timestamp event occurs
Tamper 1	Set when a tamper event is detected on RTC_TAMP1
Tamper 2	Set when a tamper event is detected on RTC_TAMP2
Tamper 3	Set when a tamper event is detected on RTC_TAMP3

Several RTC events can generate an interrupt. All interrupts can wake the microprocessor up from all low-power modes.
The Alarm A interrupt is set when the calendar value matches the Alarm A value.
Similarly, the Alarm B interrupt is set when the calendar value matches the Alarm B value.
The wakeup timer interrupt is set when the wakeup auto reload timer reaches zero.
The timestamp interrupt is set when a timestamp event occurs.
The tamper 1, 2 and 3 interrupts are set when a tamper event is detected respectively on the RTC_TAMP1, RTC_TAMP2 or RTC_TAMP3 pin.

Low-power modes

Mode	Description
Run	Active.
Sleep	Active. RTC interrupts cause the device to exit Sleep mode.
Low-power run	Active.
Low-power sleep	Active. RTC interrupts cause the device to exit Low-power sleep mode.
Stop 0/Stop 1	Active when clocked by LSE or LSI. RTC interrupts cause the device to exit Stop 0/Stop 1 mode.
Stop 2	Active when clocked by LSE or LSI. RTC interrupts cause the device to exit Stop 2 mode.
Standby	Active when clocked by LSE or LSI. RTC interrupts cause the device to exit Standby mode.
Shutdown	Active when clocked by LSE. RTC interrupts cause the device to exit Shutdown mode.

The RTC peripheral is active in all low-power modes and the RTC interrupts cause the device to exit the low-power mode. In Stop 0, Stop 1, Stop 2 and Standby modes, only the LSE or LSI clocks can be used to clock the RTC. Only the LSE is functional in Shutdown mode.

Power Optimization

- RTCAPBEN bit: RTC APB clock can be stopped when not needed for register access (except on STM32L47x/48x devices)

A bit is available in the Reset and Clock Control module, in order to stop the RTC APB clock when there is no need to access RTC registers.
This feature is not available on STM32L47x/48x devices

Debug information

- DBG_RTC_STOP bit: RTC counter stopped when core is halted

A bit is available in the MCU Debug interface, in order to
stop the RTC counter when the core is halted for debugging.

Related peripherals

- Refer to these peripheral trainings linked to the RTC
    - Reset and clock control (RCC)
    - Power control (PWR)
    - Extended interrupt controller (EXTI)

This is a list of peripherals related to the real-time clock.
Please refer to these peripheral trainings for more information if needed.
- Reset and clock control
- Power control
- Extended interrupt controller

Thank you.