

Partitioning	(P)
Chip Planning	(P)
Placement	(P)
Clock Tree Synthesis	(P)
Signal Routing	(P)
Timing Closure	(P)
Boolean Functions	(L)
Binary Decision Diagrams (BDDs)	(L)
Multi Level Synthesis	(L)
Technology Mapping	(L)
Two-level Logic Optimization	(L)
Sequential Optimization	(L)
Verification	(L)
Notes	