USB PD multi-fast charging protocol power receiving chip CH224

Manual 1

Version: 2.1

https://wch.cn

1. Overview

CH224Q/CH224A supports USB. The USB PD fast charging protocol power receiving chip supports up to PD3.2. EPR 140W power It supports single-resistor configuration, I/O level configuration, and I2C configuration. The I2C interface allows reading the protocol handshake status and the current rated current of the current PD level. The chip integrates a high-voltage LDO, featuring low static power consumption, high integration, and a simplified peripheral circuit. It integrates output voltage detection and overvoltage protection, making it widely applicable in various electronic devices for expanding high-power input, such as wireless chargers, small appliances, and lithium-ion battery power tools.

CH224K/CH224D/CH221K are USB PD fast charging protocol power receiving chips that support USB PD3.0, with a maximum power of 100W, and support single resistor configuration and I/O level configuration.

2. Features

- Supports input voltage from 4V to 30V.
- Supports PD3.2 EPR, AVS, PPS, SPR protocols and BC1.2 and other boost fast charging protocols; supports
- eMarker simulation and automatically detects VCONN.
- Supports dynamic adjustment of requested voltage in multiple ways
- Supports 400kHz I2C communication; the chip integrates a high-
- voltage LDO and has low static power consumption.
- High single-chip integration, simplified peripherals, and low cost
- Built-in overvoltage protection module OVP

3. Pin arrangement

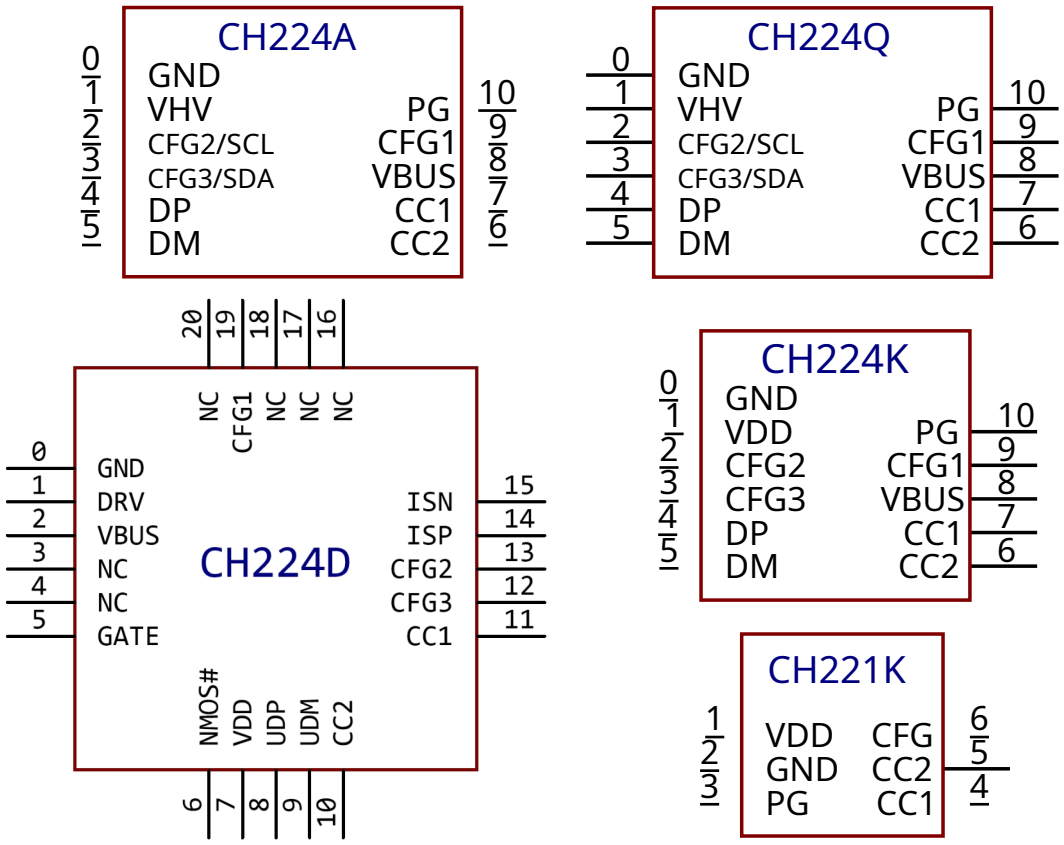


Table 3-1 Packaging Description

Packaging	Plastic body size	Pin pitch		Packaging Description	Order Model
DFN10	2*2mm	0.4mm	15.7mil	10-pin dual-sided leadless connector	CH224Q
ESSOP10	3.9mm	1.00mm	39.4mil	Narrow-pitch 10-pin patch with base plate	CH224A
ESSOP10	3.9mm	1.00mm	39.4mil	Narrow-pitch 10-pin patch with base plate	CH224K
QFN20	3*3mm	0.40mm	15.7mil	20 pins with no leads on all four sides	CH224D
SOT23-6	1.6mm	0.95mm	37mil	Small 6-pin patch	CH221K

Note: 1. Pin 0# refers to the baseboard of ESSOP10, DFN10, and QFN20 packages.

2. For new projects, it is recommended to use the small-sized and multifunctional CH224Q, while the CH224A focuses on PCB compatibility with the CH224K.

4. Pin Definitions

Table 4-1 Pin Definitions of CH224Q and CH224A

pin number		pin name	pin type(1)	Function Description
CH224Q	CH224A			
0	0	GND	P	Common grounding terminal, heat dissipation base plate.
1	1	VHV	P	For the operating power input, connect an external 1uF capacitor to ground (note the voltage rating).
4	4	DP	I/O	USB bus.
5	5	DM		
7	7	CC1	I/O	Type-C CC signal cable.
6	6	CC2		
9	9	CFG1	I	Power level configuration input pin 1.
2	2	CFG2/SCL	I,PU	Power level configuration input pin 2 or I2C clock input pin. Power level
3	3	CFG3/SDA	I/O, PU	configuration input pin 3 or I2C bidirectional data input pin. Voltage
8	8	VBUS	I	sensing input, needs to be shorted to VHV.
10	10	PG	OD	The default indicator is Power Good, active low, but customizable functions are available.

Table 4-2 CH224K Pin Definitions

pin number	pin name	pin type(1)	Function Description
CH224K			
0	GND	P	Common grounding terminal, heat dissipation base plate.
1	VDD	P	The operating power input is connected to an external 1uF capacitor to ground, and a series resistor to VBUS.
4	DP	I/O	USB bus.
5	DM		
7	CC1	I/O	Type-C CC signal cable.
6	CC2		
9	CFG1	I	Power level configuration input pins.
2	CFG2	I	
3	CFG3	I	
8	VBUS	I	Voltage sensing input requires a series resistor to the external input VBUS. The
10	PG	OD	default indicator is Power Good, active low; customizable functions are available.

Table 4-3 CH224D Pin Definitions

pin number	pin name	pin type(1)	Function Description
CH224D			
0	GND	P	Common grounding terminal, heat dissipation base plate.
2	VBUS	P	For the operating power input, it is recommended to connect an external 0.1uF or 1uF capacitor to ground.
7	VDD	P	For the internal regulator output, connect an external 1uF capacitor to ground.
8	DP	I/O	USB bus.
9	DM		
11	CC1	I/O	Type-C CC signal cable.
10	CC2		
19	CFG1	I	Power level configuration input pins.
13	CFG2	I	
12	CFG3	I	
1	DRV	O	Weak drive output, used to drive the configuration resistor.
14	ISP	I	Differential input for detecting operating current, customizable functions.
15	ISN		

5	GATE	O,HV	Customized features for driving high-side power path NMOS.
6	NMOS#	I	To enable the NMOS drive, which is active low, GND should be shorted.

Table 4-4 CH221K Pin Definitions

pin number CH221K	pin name	pin type(1)	Function Description
1	VDD	P	Operating power input, external 1uF capacitor to ground, series resistor to VBUS. Common
2	GND	P	ground terminal.
4	CC1	I/O	Type-C CC signal cable.
5	CC2		
3	PG	I,OD	The default Power Good indicator is active low; customizable functions are available.
6	CFG	OD	Power level configuration input pin.

Note 1: Explanation of pin type abbreviations:

I = Signal input;

O = Signal output;

P = power supply or ground;

OD = Open Drain Output;

HV = High voltage pin;

PD = Built-in pull-down resistor;

PU = Built-in pull-up resistor.

5. Functional Description

5.1 Overview

The CH224Q/CH224A is a protocol power receiver chip that supports PD3.2 EPR, AVS, PPS, SPR handshake protocols and BC1.2 boost fast charging protocol input. It supports voltage requests within the range of 5-30V and can dynamically configure the requested voltage level through single resistor configuration, I/O level configuration, and I2C configuration. The CH224Q, in particular, has a smaller size and is suitable for scenarios with higher integration requirements.

The CH224A is pin-compatible with the CH224K and can be replaced in most cases by changing peripheral components without altering the PCB. Please refer to Chapter 7 for details.

5.2 CH224Q/CH224A Voltage Range Configuration

5.2.1 Single Resistor Configuration

This is suitable for applications where different requested voltages can be achieved by modifying the resistor values on the same PCB.

Connect a resistor to GND on CFG1; different resistance values correspond to different voltage request levels. When using the single resistor configuration, the CFG2 and CFG3 pins can be left floating. The resistor-to-request voltage mapping table is as follows:

Table 5-1 Resistor and Requested Voltage Comparison

Configure resistor value	Requested voltage
6.8KΩ	9V
24KΩ	12V
56KΩ	15V
120KΩ	20V
210KΩ	28V

5.2.2 I/O Level Configuration

Suitable for applications where the requested voltage of the MCU is dynamically adjusted or the requested voltage of the PCB circuit is fixed.

Table 5-2 I/O Level and Requested Voltage Comparison

CFG1	CFG2	CFG3	Requested voltage
0	0	0	9V
0	0	1	12V
0	1	1	20V
0	1	0	28V
1	X	X	5V

In the table, "X" indicates that you are not interested.

In the table, "0" represents a low level, and the external circuit should be shorted to GND.

In the table, "1" indicates a high level. CFG2 and CFG3 have built-in pull-up resistors and support 3.3V or 5V input levels. They can be driven externally using push-pull or open-drain outputs. To set CFG1 to a high level, depending on the application scenario, there are three methods:

(1) Pull up to the VHV pin through a 100KΩ resistor (when CH224 does not need to be controlled);

(2) Connect a 2KΩ resistor in series to the GPIO of the MCU and output a high level using push-pull mode (when using 5V level to control CH224);

(3) Connect directly to the GPIO of the MCU and output a high level using push-pull mode (when using 3.3V level to control CH224).

5.2.3 I2C Configuration

When the chip is configured with a single resistor, the I2C configuration function is automatically enabled. At this time, voltage requests or related information can be controlled through I2C communication.

The CH224Q/CH224A has a 7-bit I2C address of 0x22 or 0x23 (excluding read/write bits).

Table 5-3 Chip Function Register Table

address	name	Function
0x09	I2C Status Register	Get the current protocol status
0x0A	Voltage control register	Switch request voltage
0x50	Current data register	Get the maximum available current for the current gear.
0x51	AVS Voltage Configuration Register (High 8 Bits)	Configure AVS to request voltage high eight bits
0x52	AVS Voltage Configuration Register (lower 8 bits)	Configure AVS to request the lower eight bits of voltage.
0x53	PPS Voltage Configuration Register	Configure PPS request voltage
0x60~0x8F	PD power data register	Get complete power information from the adapter

0x09: I2C Status Register

Bit	7	6	5	4	3	2	1	0
name	reserve	reserve	reserve	EPR activation	PD activation	QC3 activation	QC2 activation	BC activation
default value	0	0	0	0	0	0	0	0
Reading and writing	Read-only							

When BIT0, 1, 2, 3, or 4 is 1, it indicates that the corresponding protocol handshake was successful.

0x0A: Voltage Control Register

Bit	7	6	5	4	3	2	1	0
name	Please request the voltage value and refer to the detailed explanation.							
default value	0x00							
Reading and writing	Write only							

Request voltage details:

0:5V 1:9V 2:12V 3:15V 4:20V 5:28V

6: PPS Mode 7: AVS Mode

0x50: Current Data Register

Bit	7	6	5	4	3	2	1	0
name	Maximum current reference value (unit: 50mA)							
default value	0xXX							
Reading and writing	Read-only							

This register indicates the maximum available current value under the current PD setting. This register is only valid during the handshake PD protocol.

0x51, 0x52: High eight bits of AVS voltage configuration register, low eight bits of AVS voltage configuration register

Bit	15	14	13	12	11	10	9	8	7	6	5	Enable					4	3	2	1	0
name									AVS Request Voltage Value (Unit: 100mV)												
default value	0x0000																				
Reading and writing	Write only																				

The voltage configuration register consists of bits 0-7 (lower 8 bits) for the requested voltage, bits 8-14 (higher 7 bits) for the requested voltage, and the highest bit (enable bit). During configuration, the lower 8 bits are written first, followed by the higher 7 bits and the enable bit (set to 1). When initially requesting AVS, the voltage is configured first, then the voltage control register is configured to AVS mode. Subsequent voltage adjustments can be made simply by modifying the AVS voltage configuration register.

0x53: PPS Voltage Configuration Register

Bit	7	6	5	4	3	2	1	0
name	PPS setting voltage (unit: 100mV)							
default value	0x00							
Reading and writing	Write only							

When applying for PPS for the first time, first configure the voltage, then configure the voltage control register to PPS mode. Subsequent voltage adjustments will be made by directly modifying the PPS register.

Simply press the configuration register.

0x60~0x8F: PD Power Data Register

default value	0x00
Reading and writing	Read-only

When the adapter's power supply capacity is less than 100W, reading this area will yield complete power SRCCAP data. When the chip is in EPR mode (28V), reading this area will yield complete EPR_SRCCAP data.

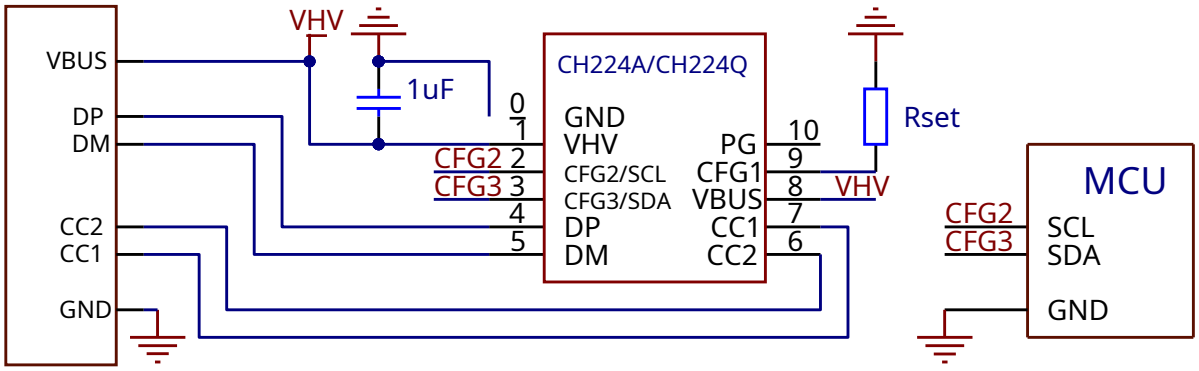
5.3 Simulating eMarker Functionality

If you want to use the analog eMarker function and request an output greater than 20V or greater than 60W, you must use a Type-C male connector and connect a 1KΩ resistor to GND on the CC2 pin (please contact our technical support).

6. Reference Schematic Diagram

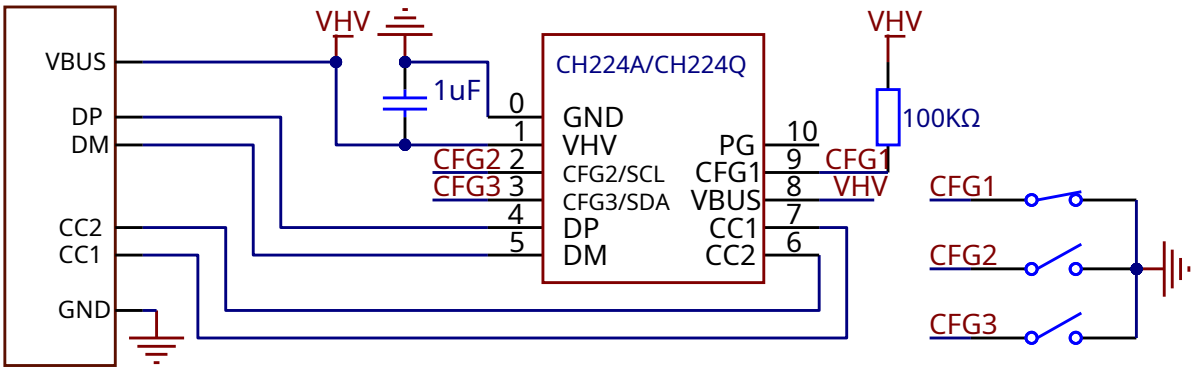
6.1 CH224Q/CH224A Reference Schematic

6.1.1 Single Resistor Configuration and I2C Configuration Reference Schematic (Rset resistance value corresponds to the requested voltage reference Table 5-1) Single-resistor configuration is achieved by connecting a specific value of configuration resistor to GND via the CFG1 pin. In this case, CFG2 and CFG3 can be used for I2C configuration. If I2C configuration is not used, CFG2 and CFG3 can be left floating.

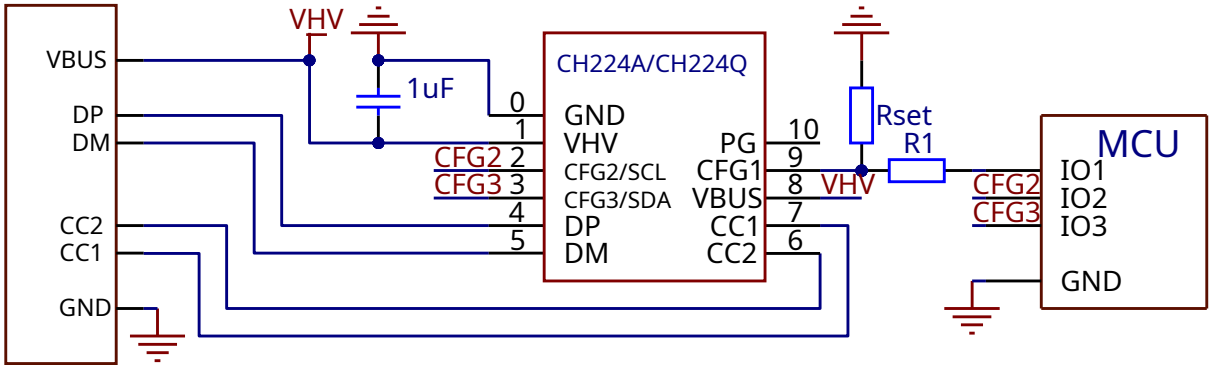


6.1.2 I/O Level Configuration Reference Schematic (I/O Level Corresponding Request Voltage Reference Table 5-2)

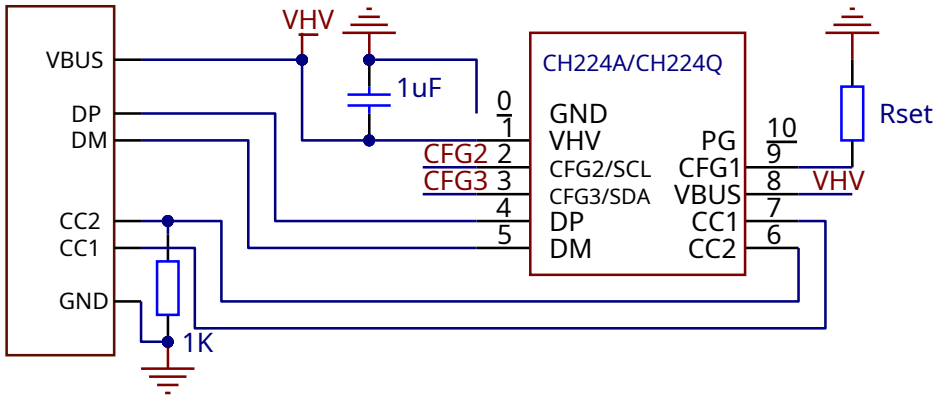
When the power system does not need to interact with or control the CH224, the CFG1 can provide a high level by connecting a 100KΩ resistor in series to the VHV pin (the figure below shows the I/O level configuration of 20V).



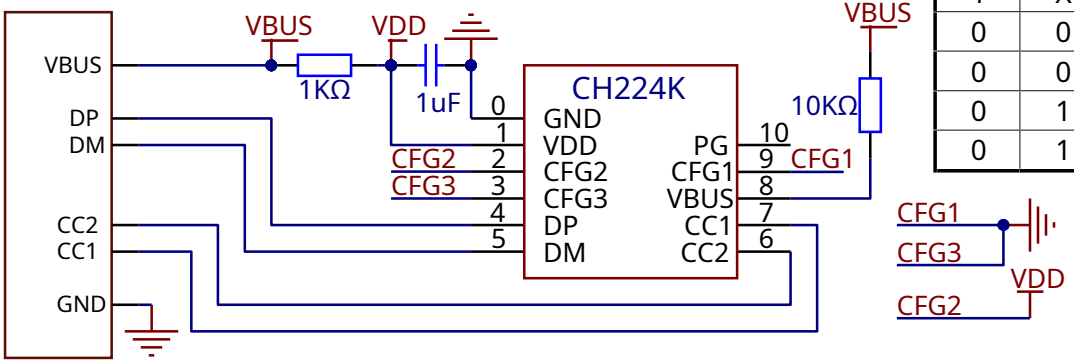
When the power supply system has a 3.3V or 5V power supply and CH224 needs to be controlled, CFG1 can be connected to the GPIO of the MCU in the system (as shown in the figure below). If the system high level is 3.3V, R1 should be 0Ω; if the system high level is 5V, R1 should be 2KΩ.



6.1.3 Using Type-C male port eMarker to simulate functionality



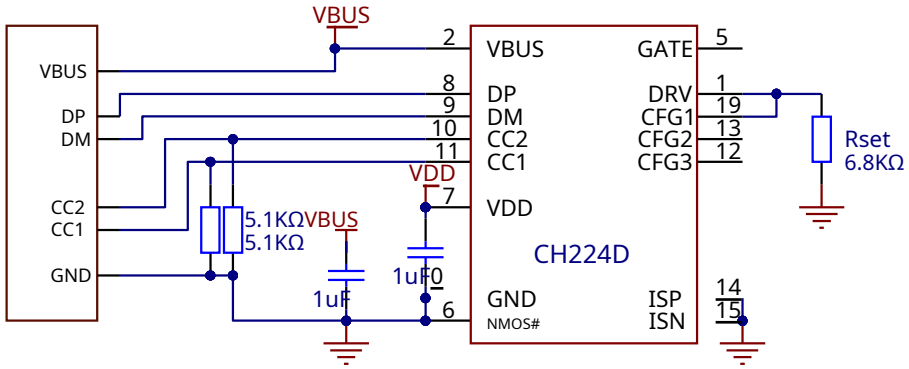
6.2 CH224K Reference Schematic (The diagram shows I/O level configuration of 20V)



CFG1	CFG2	CFG3	ask Voltage
1	X	X	5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

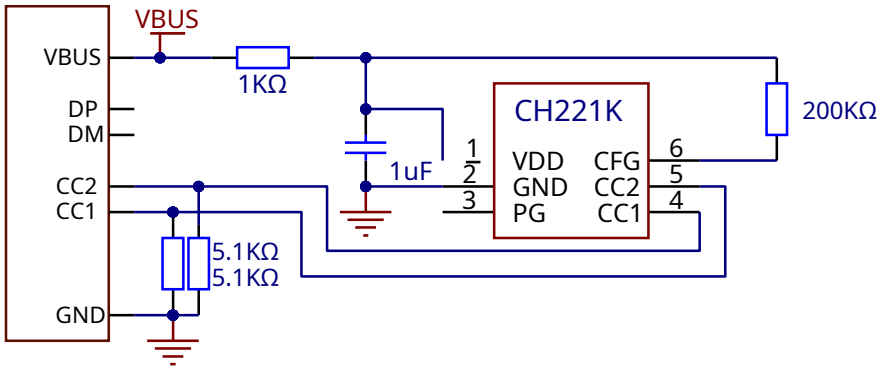
Note: It is recommended to upgrade to the CH224A chip, see section 7.2.

6.3 CH224D Reference Schematic (The diagram shows a single resistor configuration at 9V)



Rset resistance value	Requested voltage
6.8KΩ	9V
24KΩ	12V
56KΩ	15V
NC	20V

6.4 CH221K Reference Schematic (The diagram shows a single resistor configured for 20V)



Rset resistance value	Requested voltage
10KΩ	5V
20KΩ	9V
47KΩ	12V
100KΩ	15V
200KΩ	20V

7. CH224A Replacement Guide for CH224K

The CH224A is pin-compatible with the CH224K and can be replaced in most cases by changing peripheral components without changing the PCB. The following are the differences between the chips and common replacement examples.

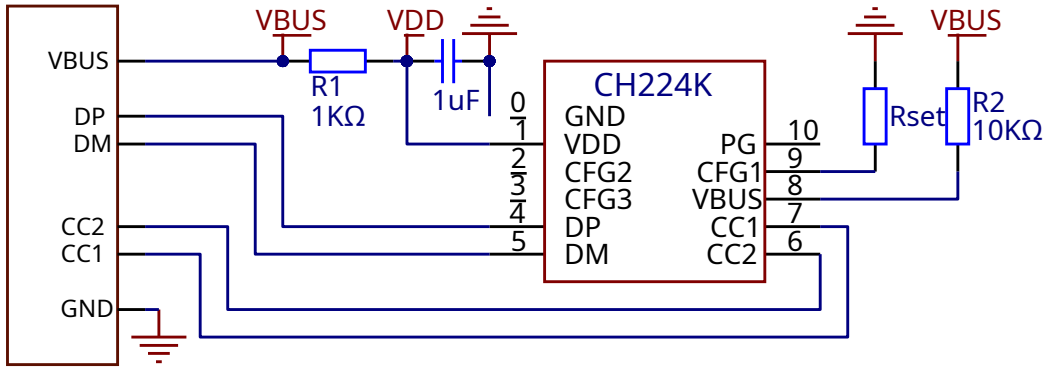
7.1 Differences between CH224A and CH224K

- Pin 1 of CH224A is VHV, with a withstand voltage of 32V; pin 1 of CH224K is VDD, with a withstand voltage of 3.6V.
- CH224A's CFG2 and CFG3 have internal pull-up resistors, while CH224K's CFG2 and CFG3 do not. CH224A's CFG1 has a
- withstand voltage of 3.8V, while CH224K's CFG1 has a withstand voltage of 8V.
- CH224A has a VBUS withstand voltage of 32V, while CH224K has a VBUS withstand voltage of 13.5V.

7.2 Common Replacement Examples

7.2.1 The original CH224K was configured in single-resistor mode (with a reserved Rset resistor, and CFG2 and CFG3 bits left floating or shorted to GND).

Figure 7-1 Schematic diagram of the original CH224K single resistor configuration

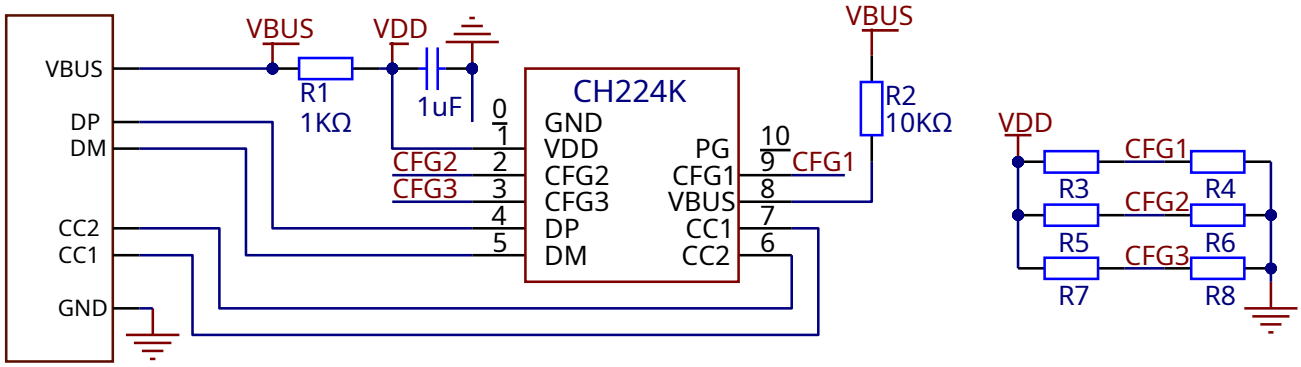


The following changes are required:

1. Short-circuit R1 or replace it with 0Ω;
2. Short-circuit R2 or replace it with 0Ω;
3. Change Rset to the configuration resistor of CH224A.

7.2.2 The original CH224K was in I/O level configuration mode (CFG1, CFG2, CFG3 reserved configuration pads or resistors).

Figure 7-2 Schematic diagram of the original CH224 I/O level configuration



Note: R3/R4, R5/R6, and R7/R8 in the diagram above are reserved resistors or pads. The following changes are required:

1. Short-circuit R1 or replace it with 0Ω;
2. Short-circuit R2 or replace it with 0Ω;

3. Replace R3 with 100KΩ, and do not solder R5 and R7 (CH224A's CFG2 and CFG3 have built-in pull-up resistors).

4. Select and short R4, R6, and R8 according to the I/O level configuration mode of CH224A.

7.3 Other Precautions

-The resistor values or corresponding I/O level voltages used in the single-resistor configuration and I/O level configuration of CH224A and CH224K are not exactly the same.

8. Parameters

8.1 Absolute Maximum Value

8.1.1 CH224Q/A Absolute Maximum Value (Critical or exceeding the absolute maximum value may cause the chip to malfunction or even be damaged)

name	Parameter Description	Minimum value	Maximum value	unit
TA	Ambient temperature during operation	- 40	105	℃
TS	Ambient temperature during storage	- 55	125	℃
VHV	Operating power supply voltage	- 0.5	32.0	V
VIOHV	Voltage on pins that support high voltage (PG, VBUS)	- 0.5	32.0	V
VIOCC	Voltage on pins CC1 and CC2	- 0.5	32.0	V
VIOUX	Voltages on pins DP, DM, and CFG1;	- 0.5	3.8	V
VIOFT	Voltages on pins CFG2 and CFG3	- 0.5	6.5	V
PD	Maximum power consumption of the entire chip (VHV voltage * current)		300	mW

8.1.2 CH221K Absolute Maximum Value (Critical or exceeding the absolute maximum value may cause the chip to malfunction or even be damaged)

name	Parameter Description	Minimum value	Maximum value	unit
TA	Ambient temperature during operation	- 40	105	℃
TS	Ambient temperature during storage	- 55	125	℃
VDD	Operating power supply voltage (VDD pin connected to power supply, GND pin grounded)	- 0.5	5.8	V
VODHV	Voltage on the high-voltage open-drain output pin PG	- 0.5	13.5	V
VIOCC	Voltage on pins CC1 and CC2	- 0.5	8	V
VIOUX	Voltage on CFG pin	- 0.5	VDD+0.5	V
PD	Maximum power consumption of the entire chip (VDD voltage * current)		250	mW

8.1.3 CH224K Absolute Maximum Value (Critical or exceeding the absolute maximum value may cause the chip to malfunction or even be damaged)

name	Parameter Description	Minimum value	Maximum value	unit
TA	Ambient temperature during operation	- 40	90	℃
TS	Ambient temperature during storage	- 55	125	℃
VDD	Operating power supply voltage (VDD pin connected to power supply, GND pin	3.0	3.6	V
VODHV	grounded) Voltage on VBUS pin	- 0.5	13.5	V
VIOCC	Voltages on pins CC1, CC2, and CFG1; Voltages on pins DP,	- 0.5	8	V
VIOUX	DM, CFG2, and CFG3; Maximum power consumption of the	- 0.5	VDD+0.5	V
PD	entire chip (VDD voltage * current).		400	mW

8.1.4 CH224D Absolute Maximum Value (Critical or exceeding the absolute maximum value may cause the chip to malfunction or even be damaged)

name	Parameter Description	Minimum value	Maximum value	unit
TA	Ambient temperature during operation	- 40	100	℃
TS	Ambient temperature during storage	- 55	125	℃
VDD	Operating power supply voltage (VDD pin connected to power supply, GND pin	- 0.5	6	V
VODHV	grounded) Voltage on VBUS pin	- 0.5	twenty four	V
VIOCC	Voltage on pins CC1 and CC2	- 0.5	20	V
VIOUX	Voltages on the DP, DM, CFG1, CFG2, CFG3, DRV, NMOS#, ISP, and ISN pins	- 0.5	VDD+0.5	V
VIOHX	Voltage on the GATE pin	- 0.5	VIOHV+6.5	V
PD	Maximum power consumption of the entire chip (VDD voltage * current)		300	mW

8.2 Electrical Parameters

8.2.1 CH224Q/A Electrical Parameters (Test Conditions: TA = 25℃)

name	Parameter Description	Minimum value	Typical value	Maximum value	unit
VHV	High voltage power supply voltage VHV	3.3	5.0	30	V
ICC	Power supply current during operation		1.8	12	mA
VILI2C	I2C low-level active voltage	0		0.8	V
VIHI2C	I2C high-level active voltage	1.5		3.3	V
RPUFB	Pull-up resistors for CFG2 and CFG3 pins	7	10	15	KΩ
VVHVX	VHV power supply overvoltage reset OVR protection voltage	32	33	34	V
VR	Power-on reset voltage threshold	2.2	2.4	2.65	V

8.2.2 Electrical parameters of CH221K (Test conditions: TA = 25℃)

name	Parameter Description	Minimum value	Typical value	Maximum value	unit
VLDOK	Internal power regulator VDD parallel voltage regulator	3.0	3.3	3.6	V
ILDO	Internal power regulator VDD parallel current absorption capability	0		30	mA
VR	Power-on reset voltage threshold	2.2	2.4	2.6	V

8.2.3 Electrical parameters of CH224K (Test conditions: TA = 25℃)

name	Parameter Description	Minimum value	Typical value	Maximum value	unit
VLDOK	Internal power regulator VDD parallel voltage regulator	3.24	3.3	3.36	V
ILDO	Internal power regulator VDD parallel current absorption capability	0		30	mA
TOTA	Over-temperature protection module OTA reference threshold temperature	90	105	120	℃
VR	Power-on reset voltage threshold	2.2	2.4	2.6	V

8.2.4 Electrical parameters of CH224D (Test conditions: TA = 25℃)

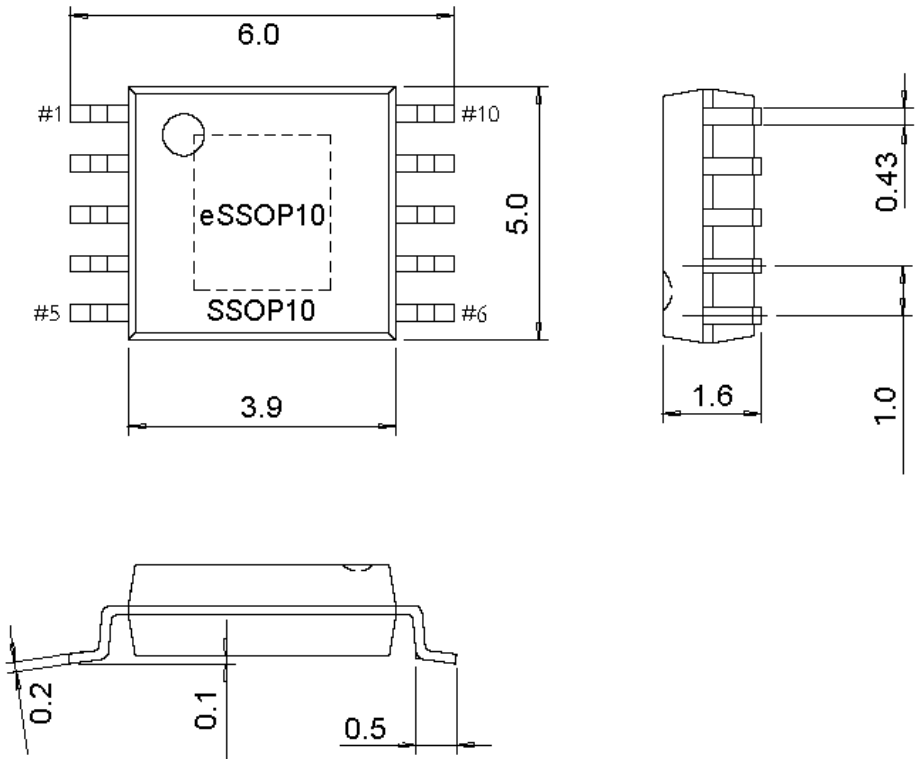
name	Parameter Description	Minimum value	Typical value	Maximum value	unit
VLDOK	Internal power regulator VDD output voltage	4.6	4.7	4.8	V
ILDO	Internal power regulator VDD external load capacity			10	mA
VR	Power-on reset voltage threshold	2.2	2.4	2.6	V

9. Encapsulation Information

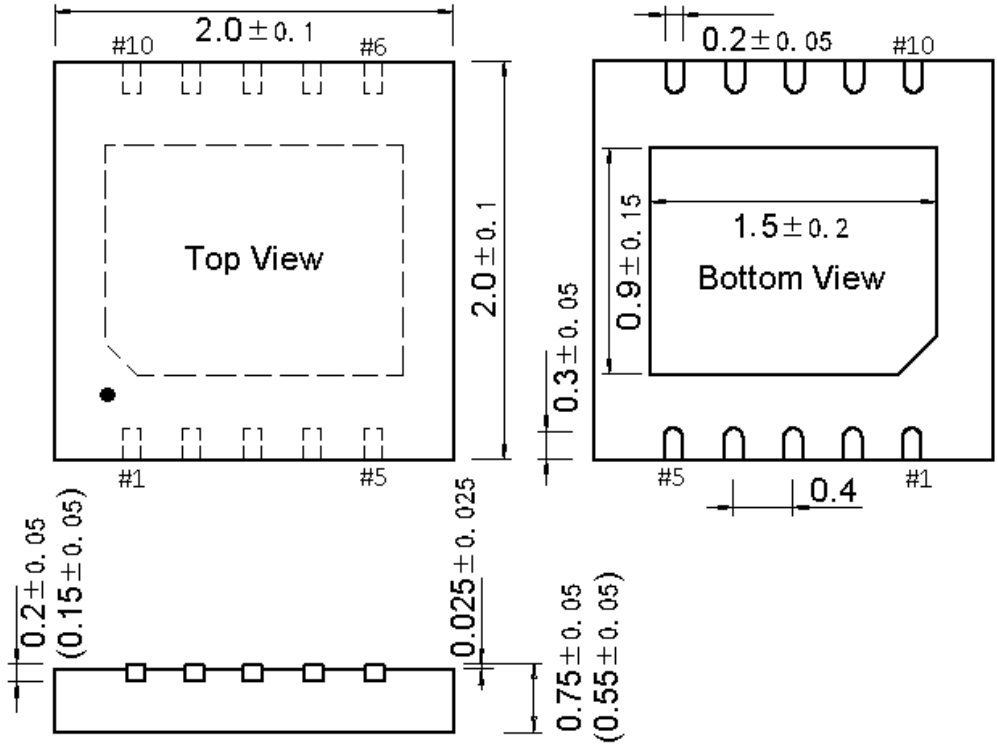
Note: The unit of dimensioning is mm (millimeters).

The pin center-to-center spacing is the nominal value with no error, and other dimensional errors are no greater than ±0.2mm.

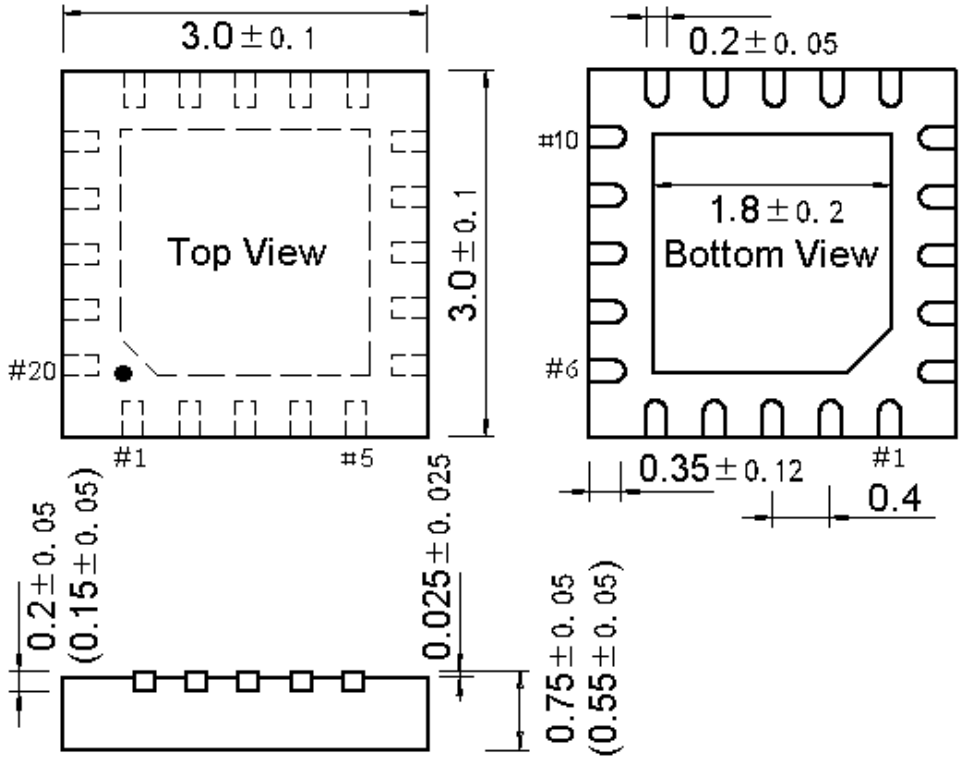
9.1 ESSOP10



9.2 DFN10



9.3 QFN20



9.4 SOT23-6