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Due: January 19 (midnight) HW 1

Instructions: Complete the problems below **in your own handwriting**. Show any work. Circle your answers where necessary. If the work or answer is not readable, you will not receive credit.

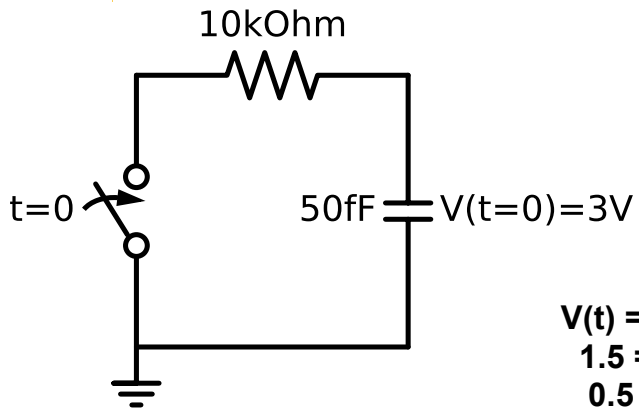
1 Fill in the Blank [30 points]

Fill in the blank with the most correct answer.

- a) Statistical Timing Analysis checks if setup and hold times are satisfied.
- b) Placement determines the location of standard cells.
- c) Routing creates the wires that connect standard cells.
- d) Floorplanning determines the location of standard cell rows and macro blocks.
- e) Dopants can be added most quickly by ion implementation.
- f) A shape on the mcon layer creates a connection between LI and the metal layer.
- g) PMOS transistors are created in an n-type well.
- h) After some processing steps, a wafer is made more flat using chemical mechanical planarization.
- i) Dielectric materials electrically insulates interconnect layers.
- j) When exposed to UV light, photoresist develops with the pattern of the mask.
- k) The source and drain of an NMOS transistor is n-type type silicon.
- l) The four terminals of a transistor are the gate, source, drain and body.
- m) Metal interconnect is commonly made with copper (a material).
- n) Modern MOS transistor gates are made with polysilicon (a material).
- o) Etching can be isotropic or anisotropic.

2 Review: Time Constants [8 points]

What is the time in **nanoseconds** to discharge this capacitor to 50% of the initial value? **Show your work!**

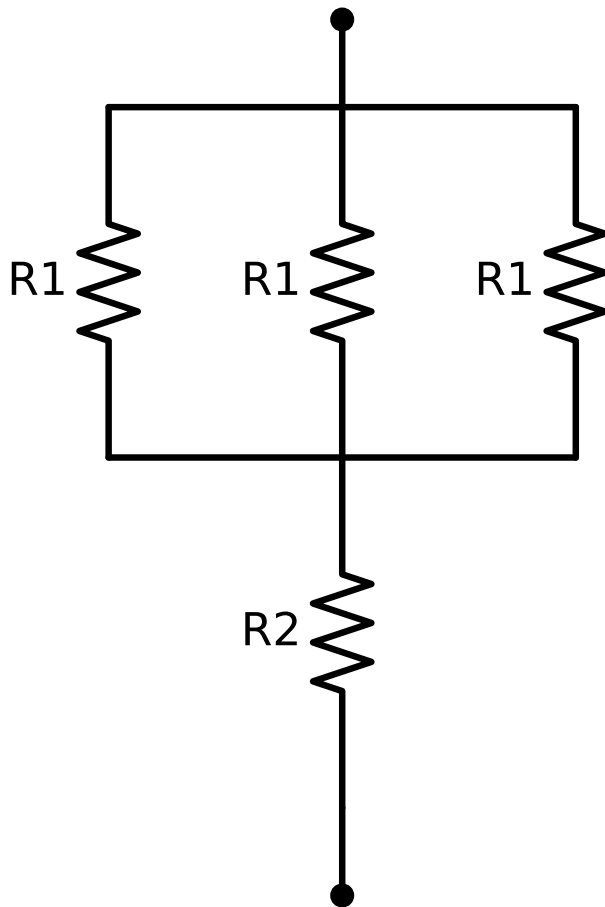


$$\begin{aligned} V(t) &= V_0 \cdot e^{-t/rc} \\ 1.5 &= 3 \cdot e^{-t/rc} \\ 0.5 &= e^{-t/rc} \\ \ln(0.5) &= -t/(10^4 \cdot 50 \cdot 10^{-15}) \\ t &= -\ln(0.5) \cdot (5 \cdot 10^{-9}) \end{aligned}$$

$$t = 0.3466 \text{ ns}$$

3 Review: Series/Parallel Resistors [5 points]

Assuming $R_1=10\text{k}\Omega$ and $R_2=20\text{k}\Omega$, what is the equivalent resistance in $\text{k}\Omega$ of the circuit below?
Show your work!



$$\frac{1}{((1/10)*3)} + 20 =$$
$$\frac{10}{3} + 20 =$$

23.33kOhm

4 Processing Steps [7 points]

For each mask layer, specify the correct processing step or step(s) in the CMOS fabrication process: implantation, diffusion, oxidation, etch, deposition.

a) nwell: Implantation, diffusion

b) psdm: Implantation, diffusion

c) m1: Deposition, etching

d) licon: Deposition, etching

e) poly: Deposition, etching

f) diff: Diffusion

g) mcon: Implantation, diffusion