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Due: February 2 (midnight) **HW 3**

Instructions: Complete the problems below **in your own handwriting**. Show any work. Circle your answers where necessary. If the work or answer is not readable, you will not receive credit.

Also, submit the following required spice netlists as described in the problems to your github repository:

- hw3/drcX.gds (where X is your cell)
- hw3/lvsX.spice (where X is your cell)
- hw3/FO4_rise.sp
- hw3/delay_rise.sp
- hw3/sizing_rise.sp

In this project, you will gain basic skills with editing and verifying standard cell layouts. You will also gain experience running spice to simulation standard cells.

You should go through the KLayout tutorial at `https://vlsida.github.io/chip-tutorials/klayout.html` including the DRC, LVS, and Edit sub-pages. While we will not check that you did this, you need to learn the tools well enough to do this assignment.

Several of these problems use Ngspice and circuit simulation. You will also need to review the Spice and Ngpice tutorials at:

- `https://vlsida.github.io/chip-tutorials/spice.html`
- `https://vlsida.github.io/chip-tutorials/ngspice.html`

It is recommended that you start with the *example.sp* provided in those tutorials. Use include files (like the tutorial example) to include the logic gates and the technology models:

```
.lib "~/.volare/sky130A/libs.tech/ngspice/sky130.lib.spice" tt
.include "~/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_fd_sc_hd.spice"
```

Without these includes, our verification of your simulation will not work. For each of your spice files, make sure that they automatically run without interactivity by including the following lines before your .END statement:

```
.control
run
quit
.endc
```

Without this, your simulation will run in interactive mode and "break" our grading scripts.

Unless otherwise indicated, use $V_{dd} = 1.8V$, input slew rates are 5ps (0% to 100% or 100% to 0% of V_{dd}), and delays are 50% to 50% of V_{dd}.

1 DRC [20 points]

Depending on the first letter of your last name, select one of the following cells:

- A-G: drc1.gds
- H-M: drc2.gds
- N-S: drc3.gds
- T-Z: drc4.gds

Identify the DRC error(s) and adjust the layout so that it passes all DRC checks while still passing LVS. You should not increase the width or height of the standard cell. You can add, delete, or move shapes. You should not, however, change the functionality of the cell! The spice netlist of the above cell is available (drc.cdl) so you can run LVS and ensure it still passes.

In your CSE 122 Gitlab project directory, add a file in a subdirectory called `hw3/drcX.gds` with the corrected layout.

Done and pushed through command line.

2 LVS [20 points]

Depending on the first letter of your **CruzID** (NOT LAST NAME!), select one of the following cells:

- A-G: lvs1.gds, lvs1.sp
- H-M: lvs2.gds, lvs2.sp
- N-S: lvs3.gds, lvs3.sp
- T-Z: lvs4.gds, lvs4.sp

Assume that the layout is correct, but the spice is not. Usually, you won't know! Fix the spice netlist so that it passes LVS with the layout.

In your CSE 122 Gitlab project directory, add a file in a subdirectory called `hw3/lvsX.sp` with the corrected SPICE file.

Done and pushed through the command line.

3 Gate Delay [20 points]

Using Ngspice, what is the rising FO4 delay (in ns) of the **sky130_fd_sc_hd__inv_2** gate? In other words, this gate driving 4 copies of itself. Submit a self-contained netlist that demonstrates the delay with measurement "rise_delay" and name it “FO4_rise.sp“.

Delay: **0.0691844** ns

```
Initial Transient Solution
--------------------------

Node                    Voltage
----                    -------
z                         1.8
a                           0
vdd                       1.8
z1                    2.70603e-09
z2                    2.70603e-09
z3                    2.70603e-09
z4                    2.70603e-09
vsw#branch                  0
vdd#branch            -2.5007e-11

No. of Data Rows : 3026

 Measurements for Transient Analysis

rise_delay       =  6.918440e-11 targ=  1.576684e-09 trig=  1.507500e-09
rise_time        =  1.282382e-10 targ=  1.654259e-09 trig=  1.526021e-09

ngspice-44.2 done
```

4 Input Delays [20 points]

Using Ngspice, what is the rising FO4 delay (in ns) from input A1 to the output X of the **sky130_fd_sc_hd__a21oi** gate? In other words, this gate driving 4 copies of the **sky130_fd_sc_hd__inv_2** gate just like the previous problem. What inputs are needed to measure the delay? Submit a self-contained netlist that demonstrates the delay with measurement "rise_delay" and name it “delay_rise.sp“.

- Input V(A1) = **1 -> 0**
- Input V(A2) = **1**
- Input V(B1) = **0**

Delay: **0.1677247** ns

Why is the delay different from the previous **sky130_fd_sc_hd__inv_2** gate? (Short answer)

Delay is different because we are measuring a21oi_2 now with input change and not the inv_2.

```
Initial Transient Solution
--------------------------

Node                    Voltage
----                    -------
a2                        1.8
vdd                       1.8
a1                        0
x                         1.8
b1                        0
z1                      2.70682e-09
z2                      2.70682e-09
z3                      2.70682e-09
z4                      2.70682e-09
vb#branch                 0
va#branch                 0
vsw#branch                0
vdd#branch             -2.88577e-11

 Reference value :  0.00000e+00
No. of Data Rows : 3026

  Measurements for Transient Analysis

rise_delay        =  1.677247e-10 targ=  1.675225e-09 trig=  1.507500e-09

ngspice-44.2 done
```

5 Transistor Sizing [20 points]

Using Ngspice, what size (width only, in nm, to the nearest 0.1um) PMOS transistor would make the FO4 rise delay equal to the fall delay of the **sky130_fd_sc_hd__inv1_1** gate? You should *copy* the **sky130_fd_sc_hd__inv1_1** subckt and modify the PMOS width. You should also comment out the original library include line to not conflict with this name. In other words, this gate is driving 4 copies of itself. You should only change the PMOS width. Submit a self-contained netlist that demonstrates the delay with two measurements, "fall_delay" and "rise_delay" and name it "sizing_rise.sp". Approximately, what is the Beta ratio of the Sky130 technology?

Width: **2900** nm

Beta: **2900331/650000 = 4.462** nm

```
Initial Transient Solution
--------------------------

Node                    Voltage
----                    -------
a                         0
z                         1.8
vdd                       1.8
z1                      2.47599e-09
z2                      2.47599e-09
z3                      2.47599e-09
z4                      2.47599e-09
vsw#branch                    0
vdd#branch              -1.1604e-11

 Reference value :  0.00000e+00
No. of Data Rows : 3026

  Measurements for Transient Analysis

rise_delay       =  4.981472e-11 targ=  1.557315e-09 trig=  1.507500e-09
fall_delay       =  4.981472e-11 targ=  5.523147e-10 trig=  5.025000e-10

ngspice-44.2 done
```

```
.subckt sky130_fd_sc_hd__inv_1 A VGND VNB VPB VPWR Y
X0 VGND A Y VNB sky130_fd_pr__nfet_01v8 w=650000u l=150000u
X1 VPWR A Y VPB sky130_fd_pr__pfet_01v8_hvt w=2.900331e+6u l=150000u
.ends
```