SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. 4th Minor-I Examination (Even) 2018-19

Entry No: 17BEC033

Date:

Total Number of Pages: [01]

Total Number of Questions: [06]

Course Title: Digital System Design using VERILOG

Course Code: ECL 2073

Time Allowed: 1.5 Hours **Max Marks: [20]**

Instructions / NOTE

i. Attempt All Questions.
ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
iii. Assume an appropriate data / information, wherever necessary / missing.
iv. Use of IS Code (Mention Number) is permissible in examination.

	Section - A		
Q1.	(a) Verilog HDL is a programming Language (TRUE/ FALSE) (b) Verilog HDL is case-insensitive (TRUE/ FALSE) (c) Default data-type of port names is_____ (d) Object names must be started with_____ (e) An object of REG data-type can assigned a value in _____ (f) Name the two Verilog primitives which has more than one output.	[03]	CO1
Q2.	(a) Name the value sets used in Verilog HDL, and describe in one line how they are used in Verilog. (b) What values are assigned to left hand side object on its execution if B = 'b 0101_1101_1011 and C = 'h ABCD ? (i) A = ~& (B) ; (ii) A = & (~B) ; (iii) A =B & (~C) ;	[02] [03]	CO2 CO2
Q3.	Describe the capabilities of Verilog-HDL (write point-wise)	[03]	CO1
	Section – B		
Q4.	Design a Verilog-HDL module for 3:8 Decoder using data-flow modeling.	[03]	CO2
Q5.	Write a Verilog Test-Bench code to apply inputs to a 2-bit full adder circuit. **(module name is fa_2bit with ports in this sequence (sum, cout, a_in, b_in, c_in)**	[02]	CO4
Q6.	Design a Verilog module for **2:1 mux** using gate-level modeling. Then use that **2:1 mux** to design a module for **8:1 mux**. (**Must be supported with Block/circuit diagrams**)	[04]	CO3

Course Outcomes

CO 1: Describe Verilog hardware description languages (HDL).
CO 2: Design Digital Circuits and Write behavioral models of digital circuits.
CO 3: Write Register Transfer Level (RTL) models of digital circuits.
CO 4: Verify behavioral and RTL models.

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1	Q1, Q3	06	61
CO2	Q2, Q4	08	61
CO3	Q6	04	61
CO4	Q5	02	61

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