SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. 4th Minor-I Examination (Even) 2018-19

Entry No: 17BEC033

Date:

Total Number of Pages: [01]

Total Number of Questions: [06]

Course Title: Digital System Design using VERILOG

Course Code: ECL 2073

Time Allowed: 1.5 Hours **Max Marks: [20]**

Instructions / NOTE

i. Attempt All Questions.
ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
iii. Assume an appropriate data / information, wherever necessary / missing.
iv. Use of IS Code (Mention Number) is permissible in examination.

	Section - A		
Q1.	(a) Verilog HDL is a programming Language (TRUE/ FALSE) (b) Verilog HDL is case-insensitive (TRUE/ FALSE) (c) Default data-type of port names is_____ (d) Object names must be started with_____ (e) An object of REG data-type can assigned a value in _____ (f) Name the two Verilog primitives which has more than one output.	[03]	CO1
Q2.	(a) Name the value sets used in Verilog HDL, and describe in one line how they are used in Verilog. (b) What values are assigned to left hand side object on its execution if B = 'b 0101_1101_1011 and C = 'h ABCD ? (i) A = ~& (B) ; (ii) A = & (~B) ; (iii) A =B & (~C) ;	[02] [03]	CO2 CO2
Q3.	Describe the capabilities of Verilog-HDL (write point-wise)	[03]	CO1
	Section – B		
Q4.	Design a Verilog-HDL module for 3:8 Decoder using data-flow modeling.	[03]	CO2
Q5.	Write a Verilog Test-Bench code to apply inputs to a 2-bit full adder circuit. **(module name is fa_2bit with ports in this sequence (sum, cout, a_in, b_in, c_in)**	[02]	CO4
Q6.	Design a Verilog module for **2:1 mux** using gate-level modeling. Then use that **2:1 mux** to design a module for **8:1 mux**. (**Must be supported with Block/circuit diagrams**)	[04]	CO3

Course Outcomes

CO 1: Describe Verilog hardware description languages (HDL).
CO 2: Design Digital Circuits and Write behavioral models of digital circuits.
CO 3: Write Register Transfer Level (RTL) models of digital circuits.
CO 4: Verify behavioral and RTL models.

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1	Q1, Q3	06	61
CO2	Q2, Q4	08	61
CO3	Q6	04	61
CO4	Q5	02	61

NC of copies = (71) securely only

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. 4th Minor-II Examination (Even) 2018-19

Entry No: 17BEC033

Date:

Total Number of Pages: [01]

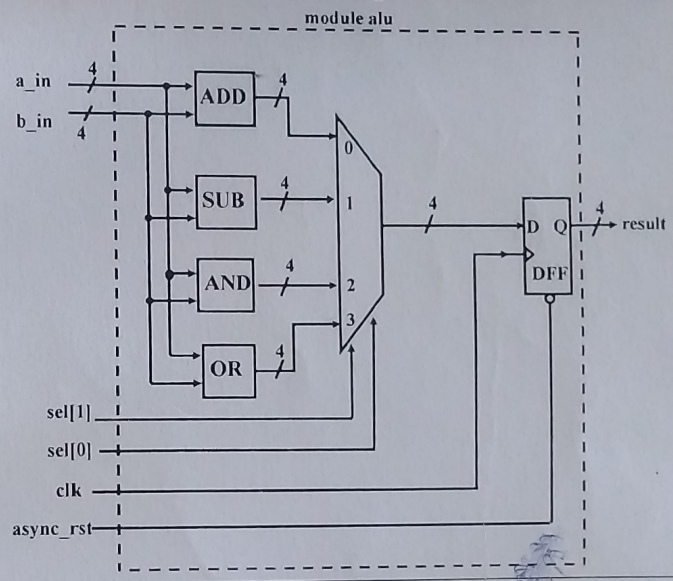
Total Number of Questions: [05]

Course Title: Digital System Design using VERILOG Course Code: ECL-2073

Time Allowed: 1.5 Hours **Max Marks: [20]**

Instructions / NOTE

i. Attempt All Questions.
ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
iii. Assume an appropriate data / information, wherever necessary / missing.

	Section - A		
Q1.	Explain different loop-statements with using short examples	[04]	CO1
Q2.	Write Verilog code for Figure shown below using case-statement and if-statement. 	[05]	CO2
	Section – B		
Q3.	Design a Verilog module for 8:3 priority encoder using case statement.	[03]	CO2
Q4.	Design a Verilog module design 5-bit synchronous (+ve edge Triggered) multiplier with asynchronous active HIGH RESET. When reset, the output should be equal to zero. (Draw External-view also)	[04]	CO3
Q5.	Design a Verilog module for negative edge triggered modulo-12 down- counter with asynchronous active low RESET and synchronous LOAD facility. (When Load = LOW, then output is will be loaded with Data_in, else works as normal down-counter). (Draw External-view also)	[04]	CO3

Course Outcomes

CO 1: Describe Verilog hardware description languages (HDL).
CO 2: Design Digital Circuits and Write behavioral models of digital circuits.
CO 3: Write Register Transfer Level (RTL) models of digital circuits.
CO 4: Verify behavioral and RTL models.

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1	Q1	04	61
CO2	Q2, Q3	08	61
CO3	Q4, Q5	08	61
CO4			

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. 4th Major Examination (Even) 2018-19 May-2019

Entry No: 17BEC033 Total Number of Pages: [02]

Date: Total Number of Questions: [10]

Course Title: Digital System Design using VERILOG Course Code: ECL-2073

Time Allowed: 1.5 Hours **Max Marks: [20]**

Instructions / NOTE

i. Attempt All Questions.
ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
iii. Assume an appropriate data / information, wherever necessary / missing.

Section - A

Q1 A digital circuit $f(A,B,C)$ gives a LOW output signal for a given input combination. However, when there occurs a change in the input signals (i.e., A,B,C) , the output signal switches from LOW to HIGH and then came back to LOW. What type of hazard the circuit does have? Comment and give remedy for this type of circuit by taking an example. — 2.5 — CO1

Q2 A digital designer has to design the following ROM like circuit for the table given below. — 2.5 — CO2

Inputs			Outputs			
A_2	A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	1	1	1	1
0	0	1	1	1	1	0
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	1	0	1	1
1	0	1	1	0	1	0
1	1	0	1	0	0	1
1	1	1	1	0	0	0

Write Verilog module for this circuit, so that ROM will infer from Verilog synthesis process.

Q3 (a) What is the difference between a Moore and Mealy Machine? — 02 — CO1

(b) What are similarities and differences between **forever-loop** and **repeat-loop?** — 02

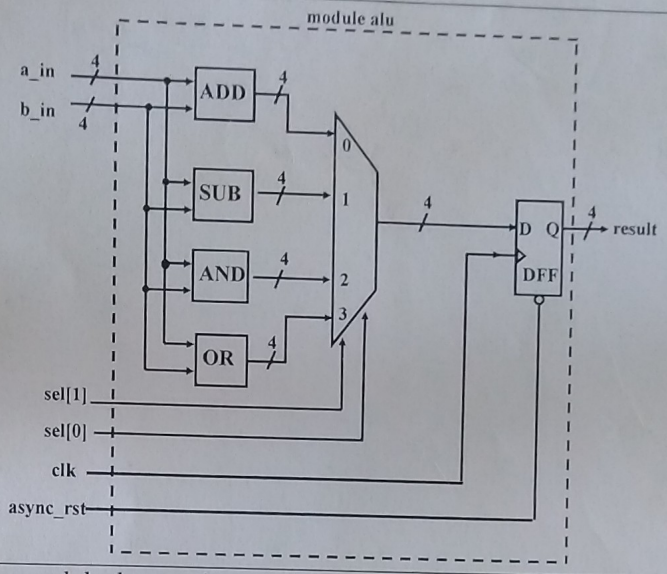
Q4 Write five main differences between a **function** and a **task**. — 04 — CO1

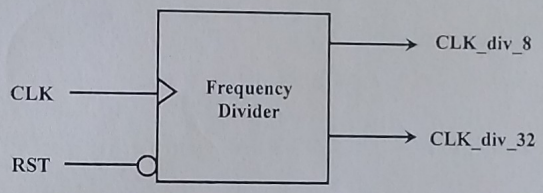
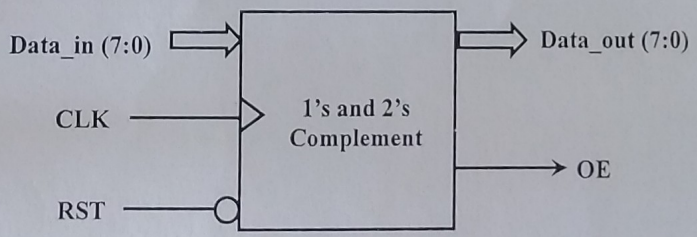
Q5 Design $\sum(A,B,C) = (0,1,5,7)$ using PAL circuit. — 03 — CO3

Q6 Draw the block diagram of an FPGA chip and explain the functionality of each block. — 04 — CO1

Section – B

Q7 Write Verilog code for Figure shown below using case-statement and if-statement and also write a test-bench for the same. — 07 — CO4



Q8	Write a Verilog module that receives a clock signal (**CLK**), and reset signal (**RST**) and generates two clock signals **CLK_div_8** (1/8 th of **CLK**) and **CLK_div_32** (1/32 th of **CLK**) 	07	CO3
Q9	A sequence detector is to detect "1100Q1" non-overlapped sequence and gives a LOW output signal when detected successfully. Design a state-machine and state-table for this sequence detector and write its verilog-code.	08	CO2
Q10	Write a verilog module using **FUNCTIONS** for the circuit given below.  The circuit gives 1's complement of **Data_in** at **Data_out** lines and OE = LOW when Data_in contains even number of ones. Similarly it gives 2's complement of **Data_in** at **Data_out** lines and **OE** = HIGH when **Data_in** contains odd number of ones. Note that the whole process is carried out at +ve edge of the **CLK**.	08	CO3

Course Outcomes

CO 1: Describe Verilog hardware description languages (HDL).
CO 2: Design Digital Circuits and Write behavioral models of digital circuits.
CO 3: Write Register Transfer Level (RTL) models of digital circuits.
CO 4: Verify behavioral and RTL models.

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1	Q1,Q3,Q4,Q6	14.5	61
CO2	Q2,Q9	10.5	61
CO3	Q5,Q8,Q10	18	61
CO4	Q7	07	61