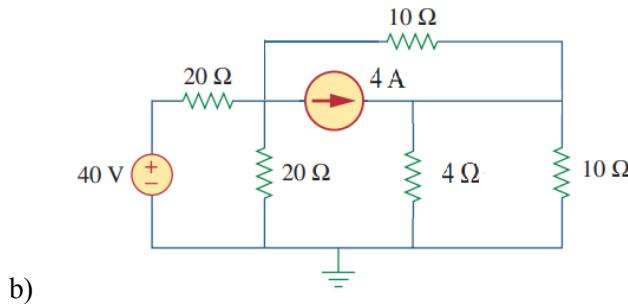
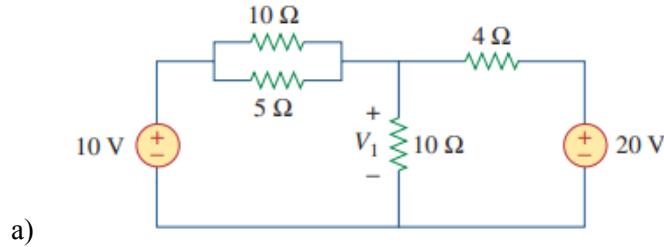


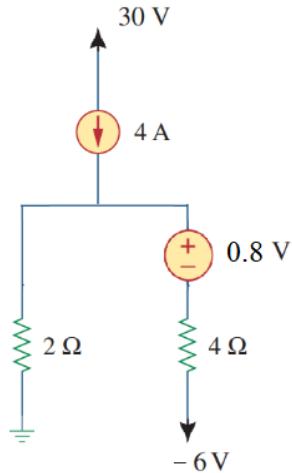
N.B: All the solutions to the problems have not been given

CSE250 [Review]

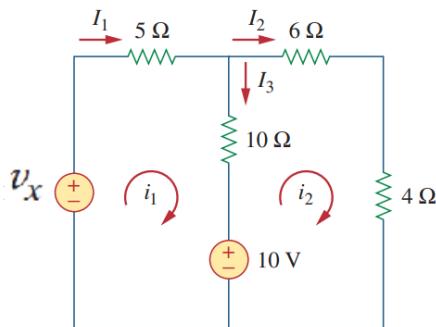
1. Draw the alternate representations of the following circuits [Note that the number of floating sources should be minimized].



2. Find the loop representation of the following circuit:



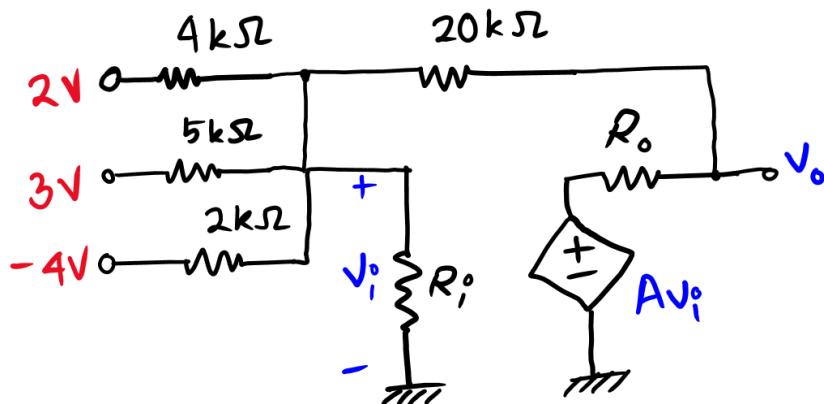
3. Here, $v_x = (10 + \text{last digit of your ID}) \text{ V}$



(i) Draw the alternate circuit representation of the circuit shown in the Figure above [Note that the number of floating sources should be minimized].

(ii) Apply KCL and KVL on the circuit drawn in (i) and calculate I_1 , I_2 , and I_3 .

4.



In the above circuit $A = 100$, $R_i = 100 \text{ k}\Omega$ and $R_o = 1 \text{ k}\Omega$. Answer the following questions

- Write the node equations for the nodes indicated by v_i and v_o .
- Solve the node equations to find the values of v_i and v_o .
- Can circuit theorems based on linearity principle (such as superposition principle) be applied to the above circuit? Explain in short why or why not.

Solution:

a) At node v_i :

$$\frac{2-v_i}{4} + \frac{3-v_i}{5} + \frac{-4-v_i}{2} = \frac{v_i - v_o}{20} + \frac{v_o}{100} \quad \dots \dots \text{(i)}$$

At node v_o :

$$\frac{v_i - v_o}{20} + \frac{Av_i - v_o}{1} = 0 \quad \dots \dots \text{(ii)}$$

b) Simplifying:

(i) becomes:

$$v_i \left(\frac{1}{4} + \frac{1}{5} + \frac{1}{2} + \frac{1}{20} + \frac{1}{100} \right) - v_o \left(\frac{1}{20} \right) = \frac{2}{4} + \frac{3}{5} - \frac{4}{2}$$

$$\therefore 1.01v_i - 0.05v_o = -0.9 \quad \dots \dots \text{(iii)}$$

(ii) becomes:

$$v_o \left(-\frac{1}{20} - \frac{100}{1} \right) + v_o \left(1 + \frac{1}{20} \right) = 0$$

$$-100.05v_i + 1.05v_o = 0 \quad \dots \dots \text{(iv)}$$

Solving (iii) & (iv) we get:

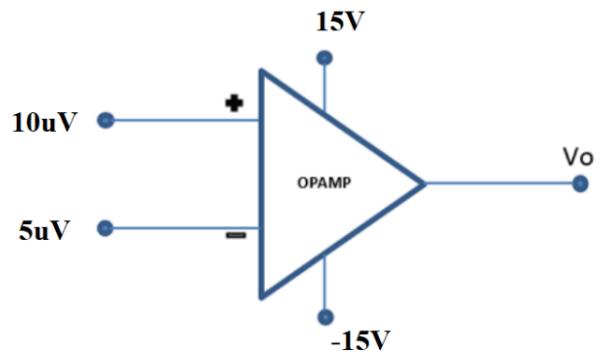
$$v_i = 0.24 \text{ V}$$

$$v_o = 22.842 \text{ V}$$

c) Yes! Because all the circuit elements are linear. (Even the voltage dependent voltage source, because the voltage dependence (Av_i) is linear.)

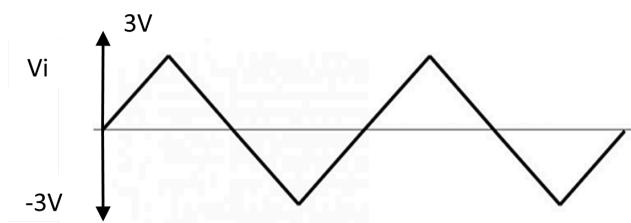
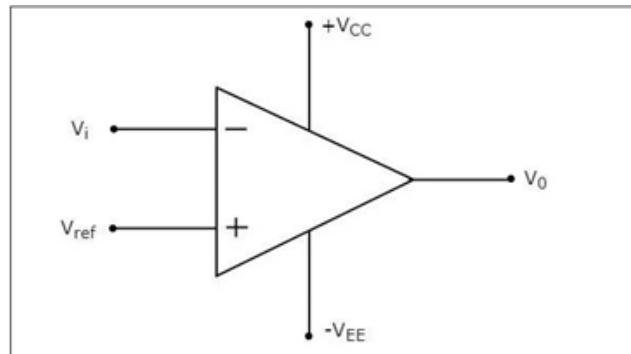
Op-Amp

1. Observe the following circuit.



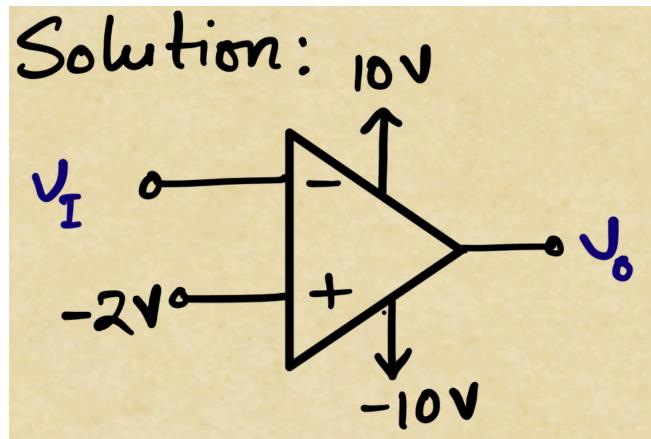
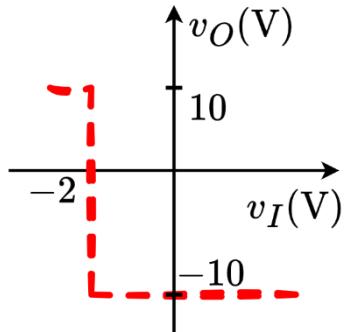
Calculate the value of V_o . Repeat the problem with $V_+=1$ mV and $V_-=0.2$ mV. Consider $A=2105$.

2. Draw output V_o for the following op-amp circuit.



$V_{CC} = 15V = -V_{EE}$, $V_{ref} = 1.5V$, V_i is a 6V p-p triangular signal as shown above.

3. Design a circuit using **op-amp** that has the voltage transfer characteristics as shown in the figure below. $v_o(V)$ is the **output voltage** and $v_i(V)$ is the **input voltage**.



4.

A valve is used to release (when valve is OPEN,) or maintain (when valve is CLOSED,) water pressure in a water tank. The valve operates on **ACTIVE LOW** logic. (i.e., the valve is OPENED when given a LOW voltage of 1 V, but remains CLOSED when provided a HIGH voltage of 6 V.)

A pressure sensor is installed in the water tank that outputs a voltage linearly proportional to pressure, as shown in the table below.

At 0.5 atm pressure	At 1 atm pressure	At 1.5 atm pressure
$v_{0.5\ atm} = 0.5\ V$	$v_{1\ atm} = 3\ V$	$v_{1.5\ atm} = 5.5\ V$

The pressure in the water tank can be measured by the formula $P = h\rho g$, where P , (in **Pascals (Pa)** unit) is the water pressure, h is the height of water in the tank (in *metres*), $\rho (= 1000\ kgm^{-3})$ is the density of water and g is the acceleration due to gravity (in ms^{-2}).

[1 atm = 101325 Pa]

- i. **Design** a circuit using Op-Amp comparator to automatically turn OPEN the valve if water level exceeds **10 m**.
- ii. **Draw** the voltage transfer characteristics (VTC) of the designed Op-Amp.

Solution:

When $h = 10 \text{ m}$: $P = h\rho g = 98000 \text{ Pa} = 0.967 \text{ atm}$

From the table we can interpolate and find the exact voltage at this pressure.

For $1 - 0.5 = 0.5 \text{ atm}$ pressure change, the voltage changes by 2.5 V

For 1 atm pressure change, the voltage changes by $2.5/0.5 \text{ V} = 5 \text{ V}$

So, for $0.967 - 0.5 = 0.467 \text{ atm}$ pressure change, the voltage changes by $5 * 0.467 \text{ V}$

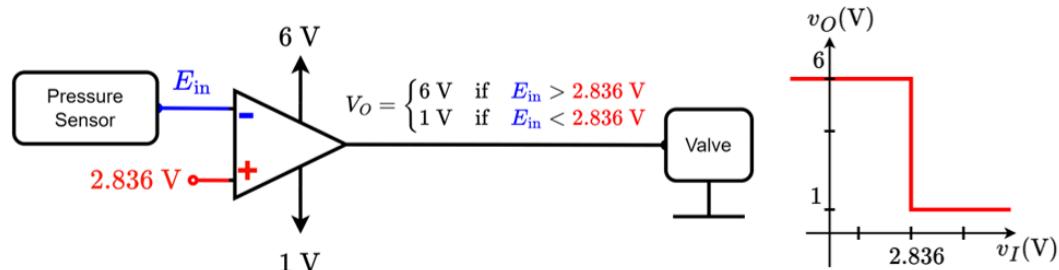
So, voltage at 0.967 atm pressure is $0.5 + 5 * 0.467 \text{ V} = 2.836 \text{ V}$

Active low logic:

High water level \rightarrow High pressure \rightarrow **High input voltage** \rightarrow Valve Open $-1 \text{ V} = V_L$

Low water level \rightarrow Low pressure \rightarrow **Low input voltage** \rightarrow Valve Closed $-6 \text{ V} = V_H$

So the comparator is in inverting configuration. As shown below:



5.

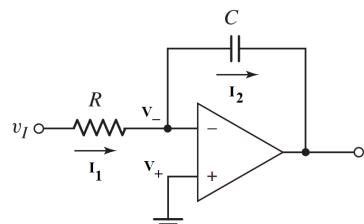


Figure 1 (a)

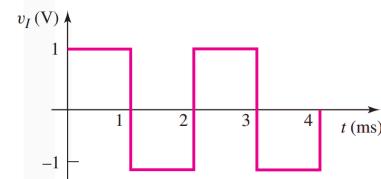


Figure 1 (b)

- Analyze the circuit drawn in Fig. 1(a) and determine the voltage values at the inverting and non-inverting nodes (V_- and V_+). [0.5+0.5]
 - Identify the relation between I_1 and I_2 . [1]
 - Analyze the circuit to derive the expression of output voltage V_o . You have to show all the steps. [3]
 - Now consider the input wave v_1 given in Fig. 1(b). For circuit parameters $R = 10 \text{ k}\Omega$ and $C = 0.1 \mu\text{F}$, determine the output voltage at $t = 1 \text{ ms}$. [1]
 - Design a circuit using Op-Amps to implement the following expression: [4]
- $$f = \frac{1}{4}x + 7y - \frac{d}{dt}z$$

Solution

part-(c)

This is an integrator circuit

$$\therefore V_o = \frac{-1}{RC} \int v_i dt$$

$$V_i = \begin{cases} 1, & 0 \leq t < 1 \\ -1, & 1 \leq t < 2 \\ 1, & 2 \leq t < 3 \\ -1, & 3 \leq t < 4 \end{cases}$$

$$\overset{So}{V_o} = \begin{cases} \frac{-1}{RC}(t) + K_1 \\ \frac{1}{RC}(t) + K_2 \\ \frac{-1}{RC}(t) + K_3 \\ \frac{1}{RC}(t) + K_4 \end{cases}$$

where, K_1, K_2, K_3, K_4 are const.

part-(d)

for $R = 10K\Omega$, $C = 0.1\mu F$,

$$V_o = \frac{-1}{10 \times 10^3 \times 0.1 \times 10^{-6}} (1 \times 10^{-3}) + K_1$$

$$\Rightarrow V_o = -1 + K_1 .$$

6.

$$i_D = I_S(e^{v_D/V_T} - 1)$$

$$\cong I_S e^{v_D/V_T}$$

[Sufficiently forward biased]

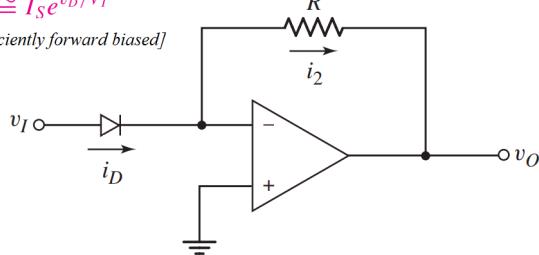


Figure 1

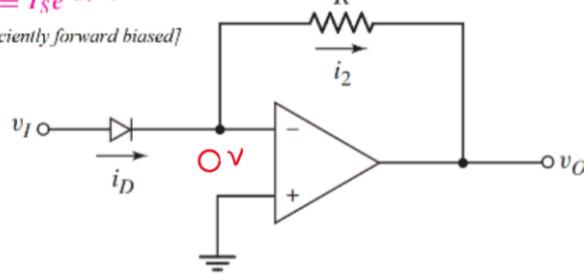
- (a) Analyze the circuit drawn in Fig. 1 and determine the voltage values at the inverting and non-inverting nodes (V_- and V_+). [0.5+0.5]
- (b) Identify and briefly explain the relation between i_2 and i_D . [1.5]
- (c) Analyze the circuit to derive the expression of output voltage V_o . You have to show all the steps. [3.5]
- (d) Design a circuit using Op-Amps to implement the following expression: [4]

part-c

$$i_D = I_S(e^{v_D/V_T} - 1)$$

$$\cong I_S e^{v_D/V_T}$$

[Sufficiently forward biased]



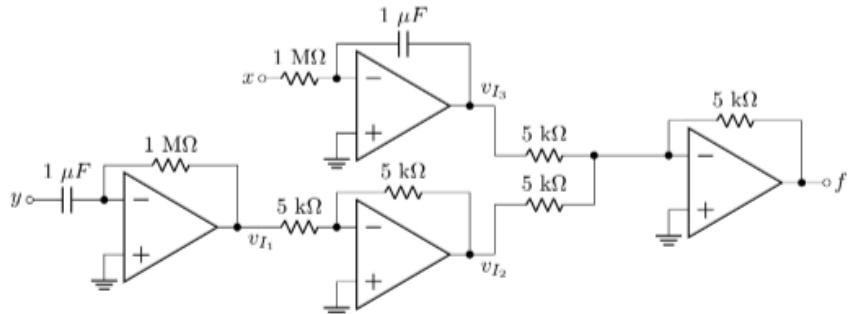
$$\tilde{i}_D = \tilde{i}_2$$

$$\hookrightarrow I_S e^{(v_D/V_T)} = \frac{0 - v_o}{R}$$

$$\hookrightarrow V_o = -I_S R e^{(v_D/V_T)}$$

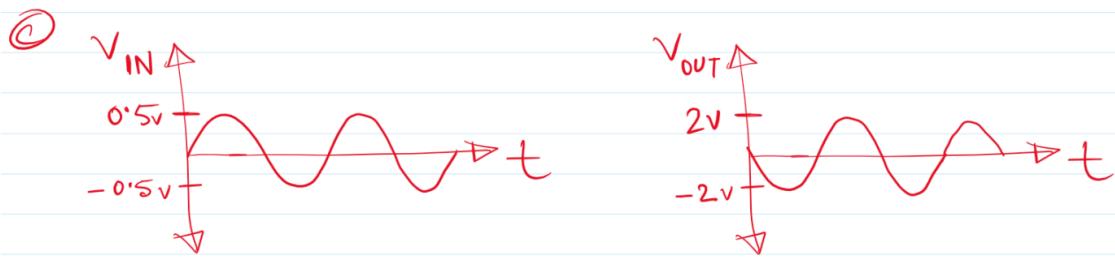
Figure 1

7.



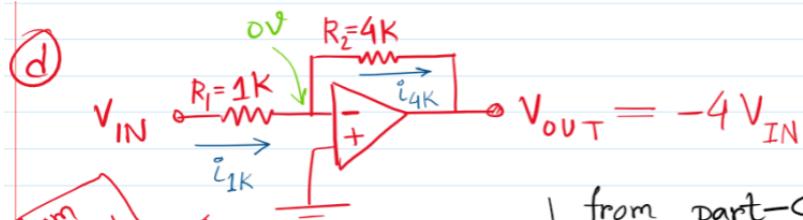
- (a) **Analyze** the circuit above to find an expression of f in terms of inputs x and y . Also, **determine** the intermediate outputs v_{I_1} , v_{I_2} , and v_{I_3} as denoted in the circuit. [4]
- (b) Draw the circuit of an inverting amplifier and **design** it in such a way that the voltage gain, $k = -4$. (*i.e.*, find the values of R_1 and R_2). [3]
- (c) **Show** the input and output waveforms of the inverting amplifier of part (b) assuming a sinusoidal input of 0.5 V amplitude. **Calculate** the amplitude of the output. [2]
- (d) Consider the inverting amplifier of part (b) again. Assume the input voltage can provide a maximum current of 0.5 μA. **Determine** the design changes required, if any, for the circuit to work. [1]

part-c



$$\begin{aligned} \text{Output Amplitude} &\rightarrow |\text{gain}| \times \text{Input Amplitude} \\ &= |-4| \times 0.5V = 2V. \end{aligned}$$

part-d



from part-b

$$i_{1k}(\text{max}) = 0.5 \mu\text{A}$$

$$\hookrightarrow \frac{V_{IN(\text{max})} - 0}{R_1} = 0.5 \text{ mA}$$

from part-c, we get,

$$V_{IN(\text{max})} = 0.5 \text{ V}$$

$$\text{So, } \frac{0.5 - 0}{R_1} = 0.5 \text{ mA}$$

$$\hookrightarrow R_1 = \frac{0.5}{0.5 \text{ mA}} = 1 \text{ M}\Omega$$

but, gain = $-4 = \frac{-R_2}{R_1} \rightarrow R_2 = 4R_1 = 4 \text{ M}\Omega$.

So, we need to set, $R_1 = 1 \text{ M}\Omega$ instead of $1 \text{ k}\Omega$

$R_2 = 4 \text{ M}\Omega$ instead of $4 \text{ k}\Omega$

**If the input voltage is not mentioned, then the resistance values will be set according to the gain and you will have to assume one of the resistances.

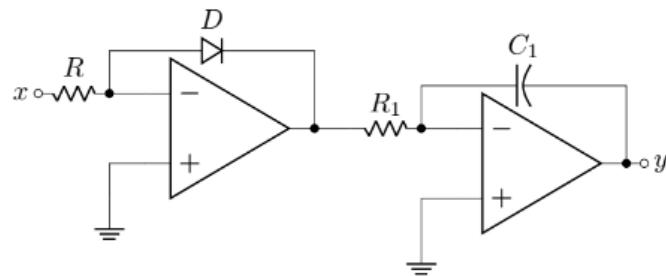
8.

- (a) **Design** a circuit using **Op-Amp comparator** to automatically turn ON (or OFF) the street lights. For this, you have a lux sensor installed on top of the street lights (facing above) that outputs a voltage proportional to amount of natural light, as listed below:

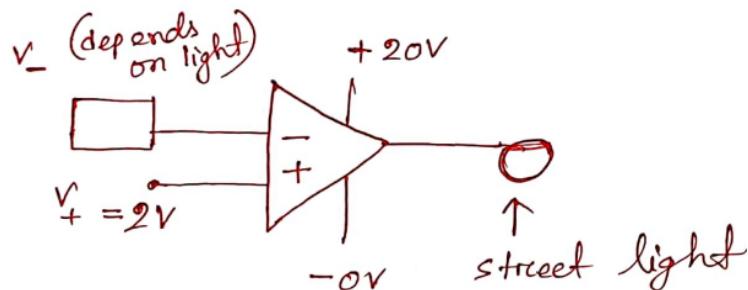
$$v_{\text{night}, 0 \text{ lux}} = 1 \text{ V} \quad v_{\text{dusk}, 20 \text{ lux}} = 2 \text{ V} \quad v_{\text{dawn}, 80 \text{ lux}} = 3 \text{ V}$$

The lights require 20 V and should be ON if the amount of light goes **below** 20 lux (at dusk). [3]

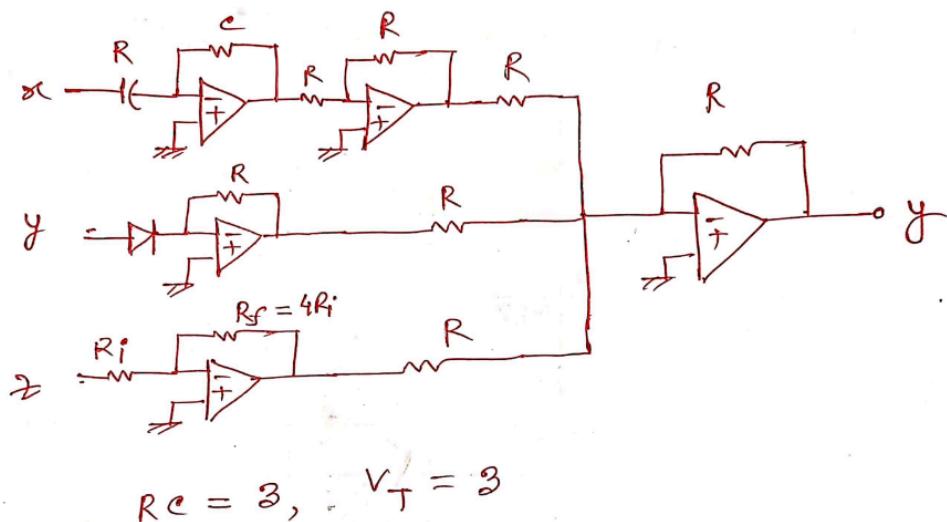
- (b) **Design** a circuit using Op-Amp to implement the expression: $f = -3 \frac{dx}{dt} + 2 \exp y + 4z$ [4]
 (c) **Analyze** the circuit below to find y as a function of x . For the diode, $I_S R = 1$ and $V_T = 1$. [3]



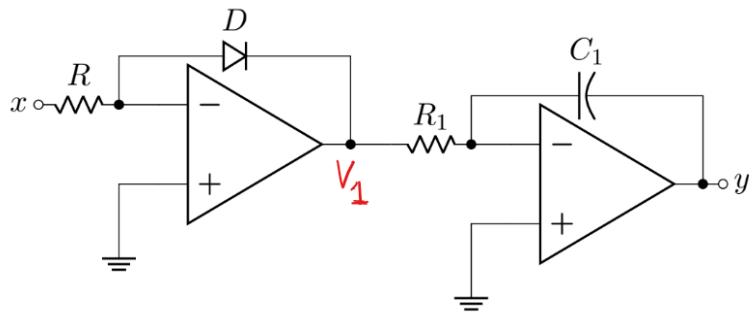
part-a



part-b



part-c

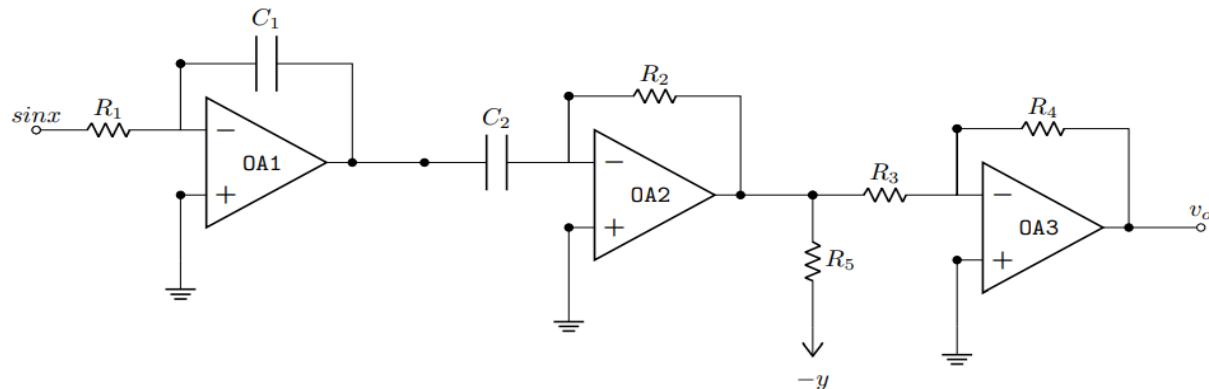


$$V_1 = -V_T \ln \frac{x}{I_S R}$$

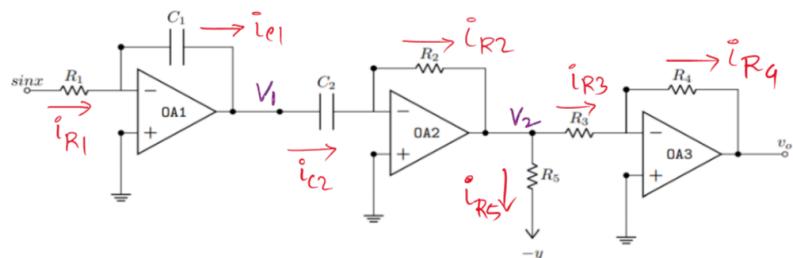
$$\begin{aligned} y &= -\frac{1}{R_C} \int V_1 dt \\ &= -\frac{1}{R_C} \int -V_T \ln \frac{x}{I_S R} dt \\ &= \frac{1}{R_C} \int \ln x \end{aligned}$$

$$\left[V_T = 1, I_S R = 1 \right]$$

9. Deduce the expression for output, V_o from the circuit above



Solution



$$\begin{aligned}
 V_1 &= \frac{-1}{RC} \int \sin x \, dt \\
 V_2 &= -RC \frac{d}{dt}(V_1) \\
 &= -RC \frac{d}{dt} \left(\frac{-1}{RC} \int \sin x \, dt \right) \\
 &= \sin x
 \end{aligned}$$

Applying KCL,

$$i_{R2} = i_{R5} + i_{R3}$$

$$\hookrightarrow i_{R1} = i_{R5} + i_{R3} \quad [\because i_{R1} = i_{C1} = i_{C2} = i_{R2}]$$

$$\hookrightarrow \frac{\sin x - 0}{R_1} = \frac{V_2 - (-y)}{R_5} + i_{R4} \quad [\because i_{R3} = i_{R4}]$$

$$\hookrightarrow \frac{\sin x}{R_1} = \frac{\sin x + y}{R_5} + \frac{0 - V_o}{R_4}$$

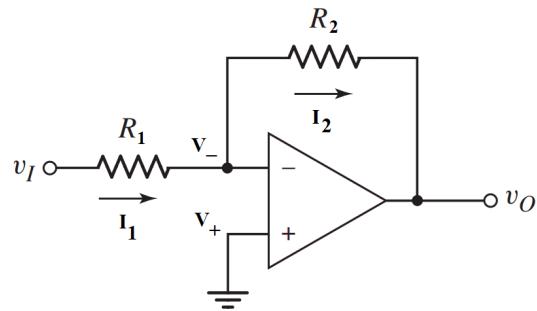
$$\hookrightarrow \frac{\sin x}{R_1} - \frac{\sin x + y}{R_5} = \frac{-V_o}{R_4}$$

$$\hookrightarrow V_o = - \left(\frac{R_4}{R_1} \sin x - \frac{R_4}{R_5} (\sin x + y) \right)$$

10. Design a circuit using op-amps to implement $y=7x$ by an

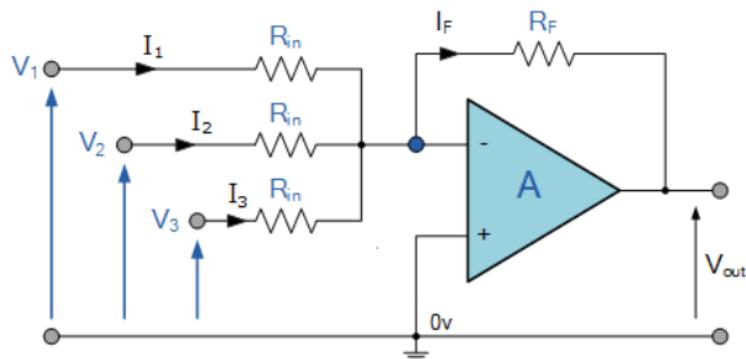
- (a) Inverting amplifier
- (b) Non-inverting amplifier

11.

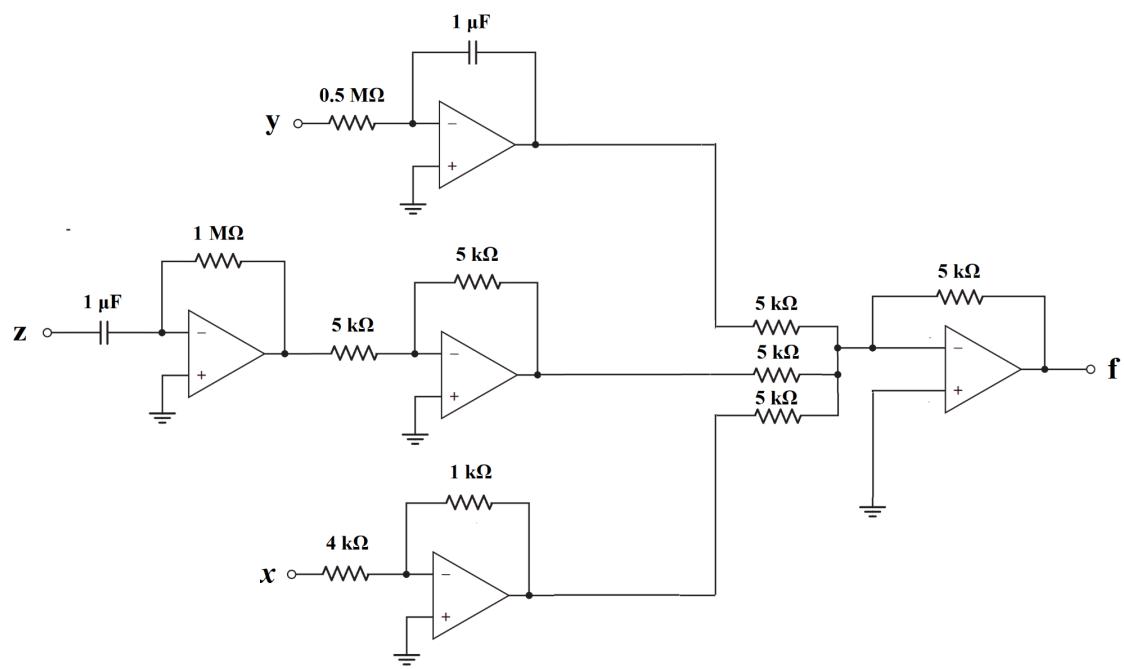


- (a) **Design** an inverting amplifier (i.e., find the values of R_1 and R_2 of the circuit shown in the Figure above) in such a way that the voltage gain is -5 .
- (b) Consider the circuit you drew in (a) again. Assume the input $v_i = 0.1 \sin\omega t$ (V) has a maximum current rating of $5 \mu\text{A}$. What design changes, if any, are required for this input, if the voltage gain remains the same? **[Check Problem 8]**
- (c) **Draw** the input and output waveforms of the circuit you designed in (c).

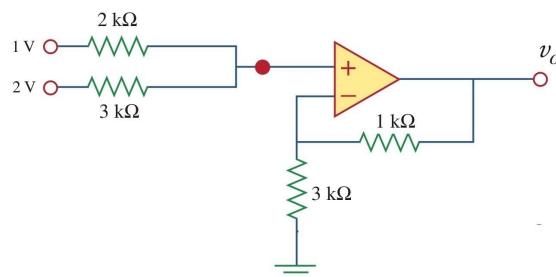
- **Analyze** the following circuit and derive the expression for the output voltage (V_{out}) in terms of the inputs. If $V_1 = 1$ V, $V_2 = 2$ V, and $V_3 = 1.5$ V, and all the resistors have equal values, calculate V_{out} .

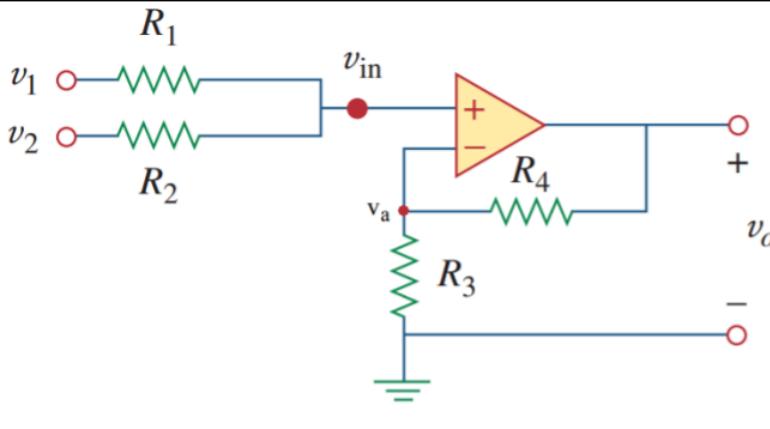


12. Analyze the following circuit to find an expression of f in terms of x , y , and z .



13. Consider the Ideal Op-Amp and find the value of V_o .





Solution

$$\frac{v_1 - v_{in}}{R_1} + \frac{v_2 - v_{in}}{R_2} = 0 \quad (1)$$

but

$$v_a = \frac{R_3}{R_3 + R_4} v_o \quad (2)$$

Combining (1) and (2),

$$v_1 - v_a + \frac{R_1}{R_2} v_2 - \frac{R_1}{R_2} v_a = 0$$

$$v_a \left(1 + \frac{R_1}{R_2} \right) = v_1 + \frac{R_1}{R_2} v_2$$

$$\frac{R_3 v_o}{R_3 + R_4} \left(1 + \frac{R_1}{R_2} \right) = v_1 + \frac{R_1}{R_2} v_2$$

$$v_o = \frac{R_3 + R_4}{R_3 \left(1 + \frac{R_1}{R_2} \right)} \left(v_1 + \frac{R_1}{R_2} v_2 \right)$$

$$v_o = \frac{R_3 + R_4}{R_3 (R_1 + R_2)} (v_1 R_2 + v_2)$$

14.

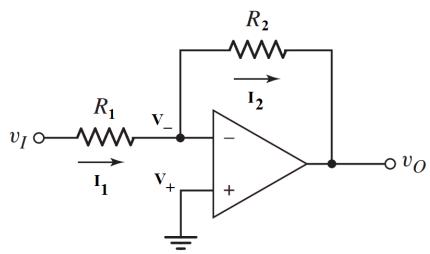
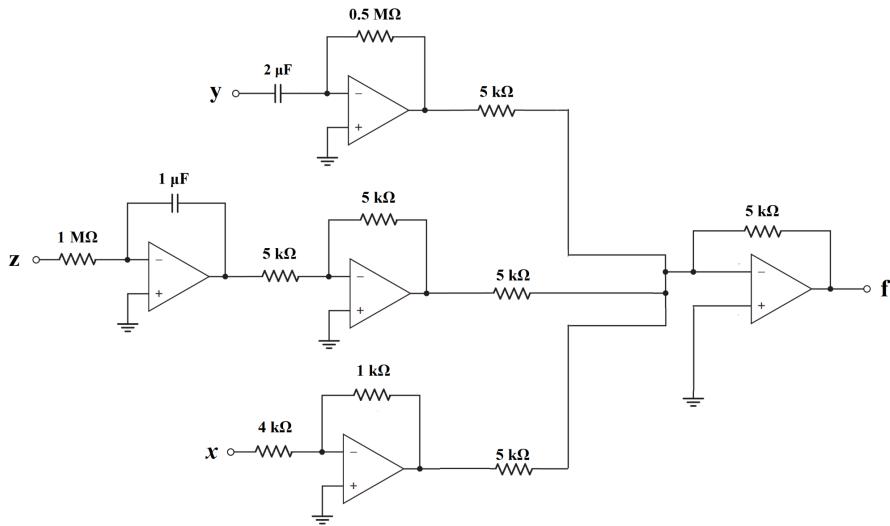


Figure 3(a)

Figure 3(b)

- (a) **Analyze** the circuit in Fig 3(a) to find an expression of f in terms of x , y , and z . [4]
- (b) **Design** an inverting amplifier (i.e., find the values of R_1 and R_2 of the circuit shown in Fig. 3(b)) in such a way that the voltage gain is -4 . [3]
- (c) **Draw** the input and output waveforms of the circuit you designed in (b). [2]
- (d) Consider the circuit in Figure 3(b) again. Assume the input $v_i = 0.1 \sin\omega t$ (V) has a maximum current rating of $4 \mu A$. What design changes, if any, is required for this input, if the voltage gain remains the same?

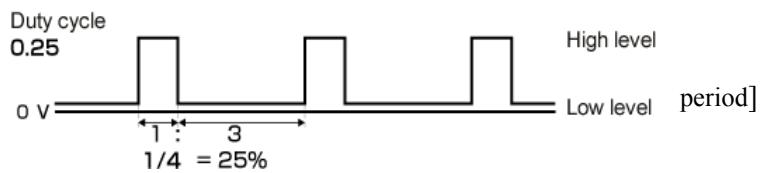
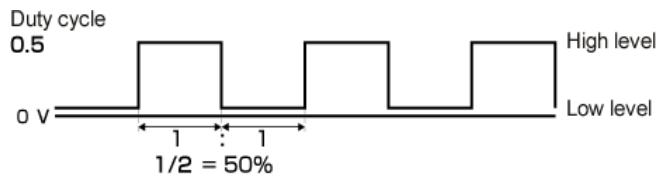
[Check Problem-8]

15.

Design an op-amp circuit to transform the sinusoidal voltage, $v_I = 5 \cdot \sin(\frac{2\pi}{5} \cdot t)$ (t is in units of ms, and time-period T is 5 ms), to:

[You must evaluate V_{REF}]

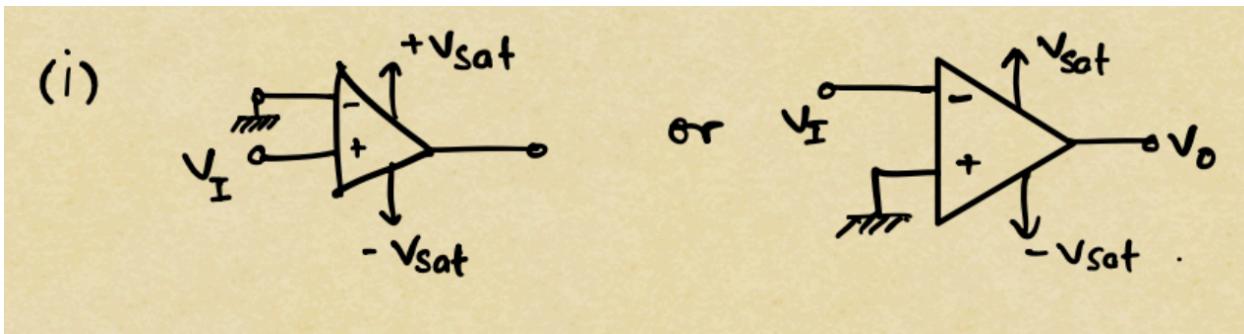
- i. A square wave with a duty cycle of **50%**.
- ii. A square wave with a duty cycle of **25%**.

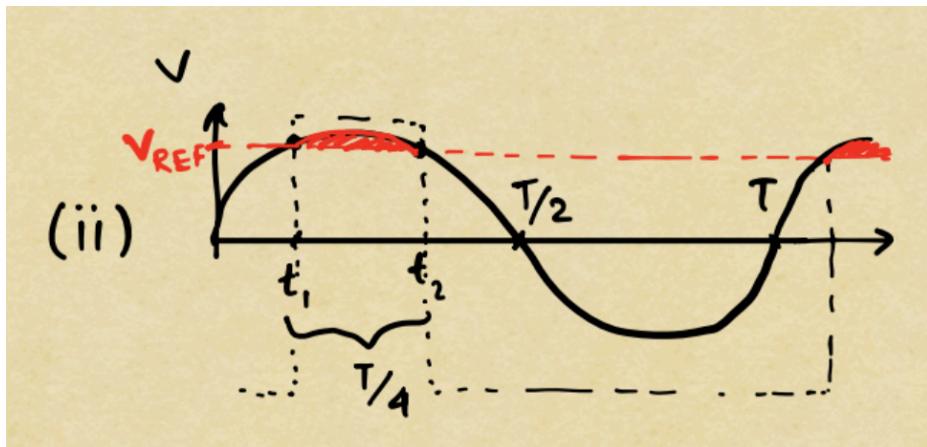


[Duty Cycle: Time of positive half cycle \div Time period]

For more information on duty cycle, click [here!](#)

[Hint: If $y = (\theta)$ is a sinusoidal function with period of 2π then $\theta = (\frac{y}{A})$ and $\pi - (\frac{y}{A})$. So, for 25% duty cycle find the value of y for which $\Delta\theta = (\pi - (\frac{y}{A})) - (\frac{y}{A}) = \frac{\text{Time period}}{4} = \frac{\pi}{2}$]





$$t_1 = \frac{5}{2\pi} \sin^{-1}\left(\frac{V_{REF}}{5}\right)$$

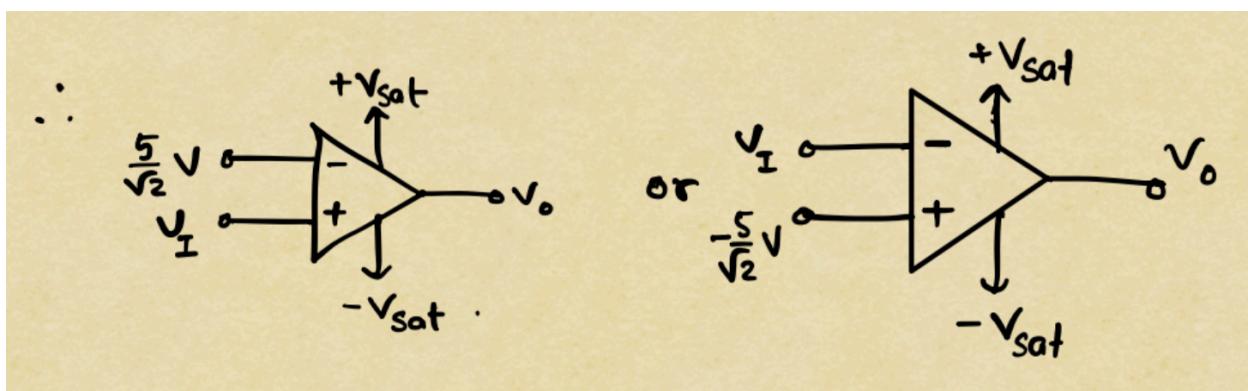
$$t_2 = \frac{T}{2} - t_1 = \frac{5}{2} - \frac{5}{2\pi} \sin^{-1}\left(\frac{V_{REF}}{5}\right)$$

$$\therefore t_2 - t_1 = \frac{T}{4} = \frac{5}{2} - 2 \cdot \frac{5}{2\pi} \sin^{-1}\left(\frac{V_{REF}}{5}\right)$$

$$\Rightarrow \frac{5}{4} = \frac{5}{2} - \frac{5 \times 2}{2\pi} \sin^{-1}\left(\frac{V_{REF}}{5}\right)$$

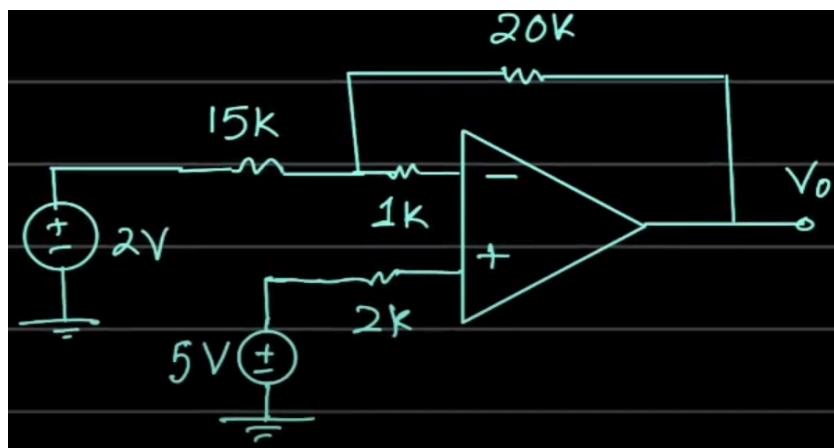
$$\Rightarrow V_{REF} = 5 \sin\left(\frac{2\pi}{5} \cdot \frac{5}{8}\right)$$

$$V_{REF} = \frac{5}{\sqrt{2}} V$$



17. Miscellaneous

Determine the output voltage, v_o

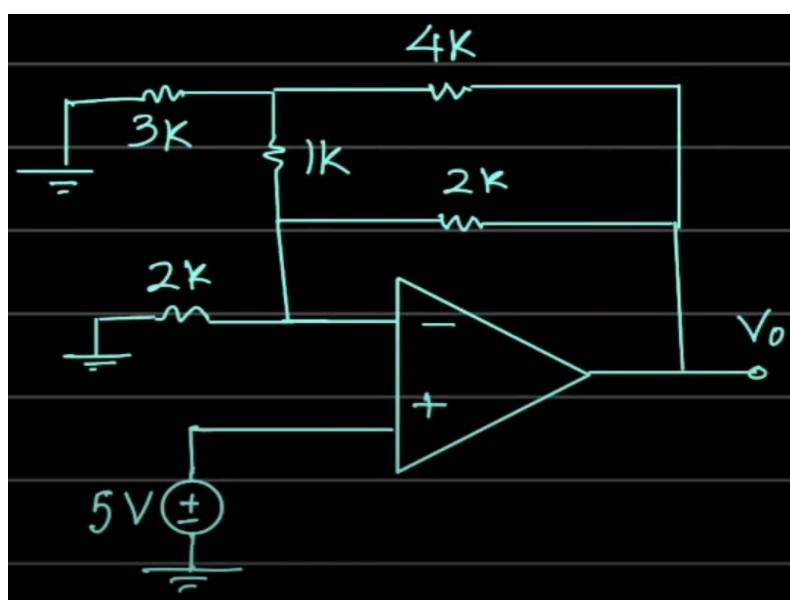


Solution: (from central playlist)

<https://youtu.be/KBWfa-NuYzk?list=PLPf6M92pkd7DRilBZLzKot-39S215ksSw&t=617>

18. Miscellaneous

Determine the output voltage, v_o

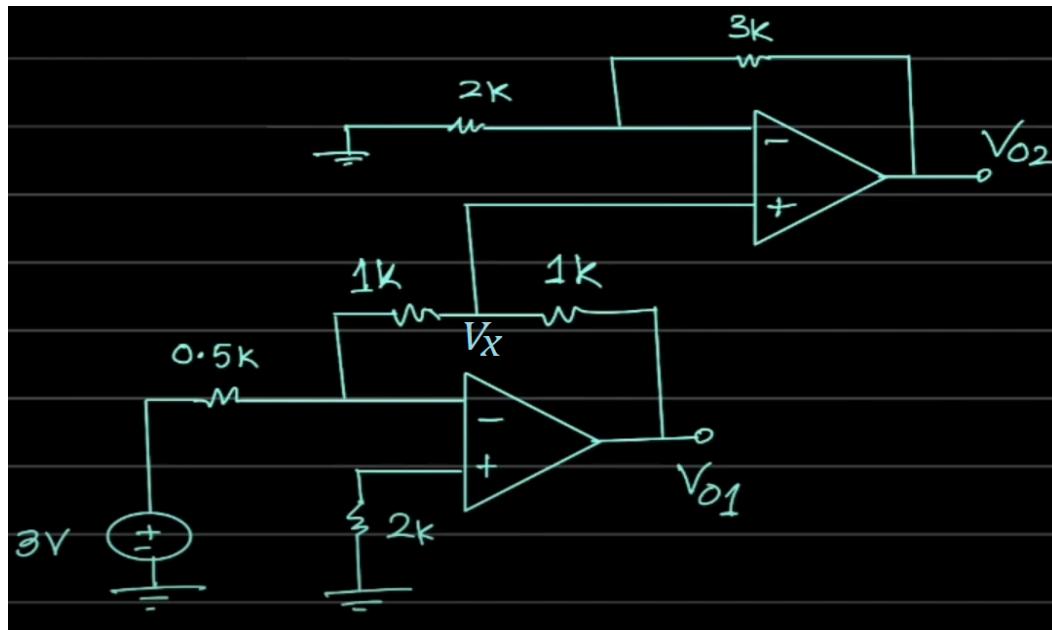


Solution: (from central playlist)

<https://youtu.be/KBWfa-NuYzk?list=PLPf6M92pkd7DRilBZLzKot-39S215ksSw&t=890>

19. Miscellaneous

Determine the voltages: V_{01} , V_X , V_{02}



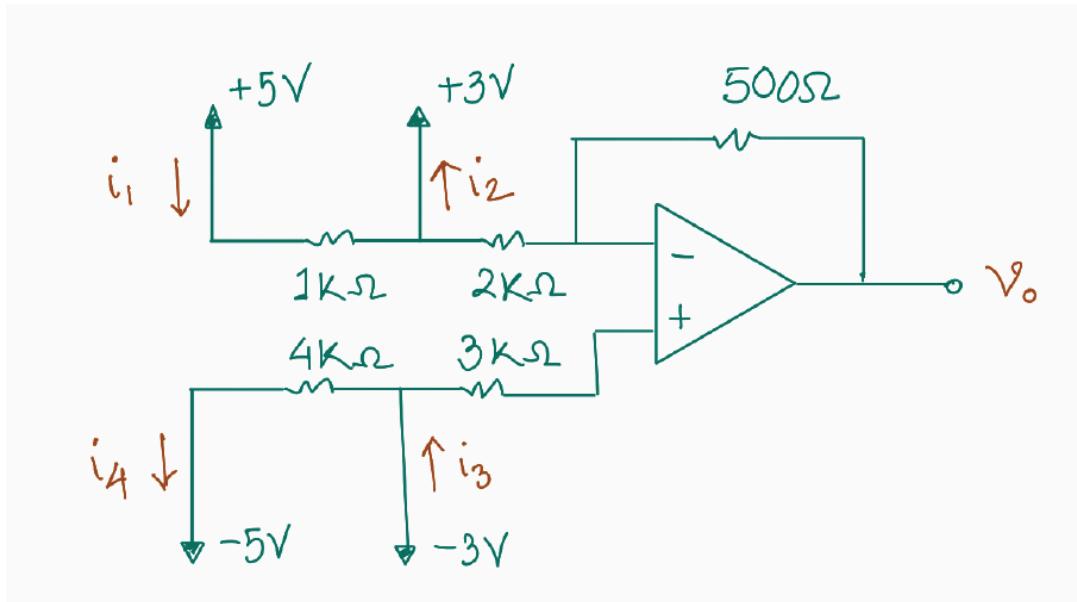
Solution: (from central playlist)

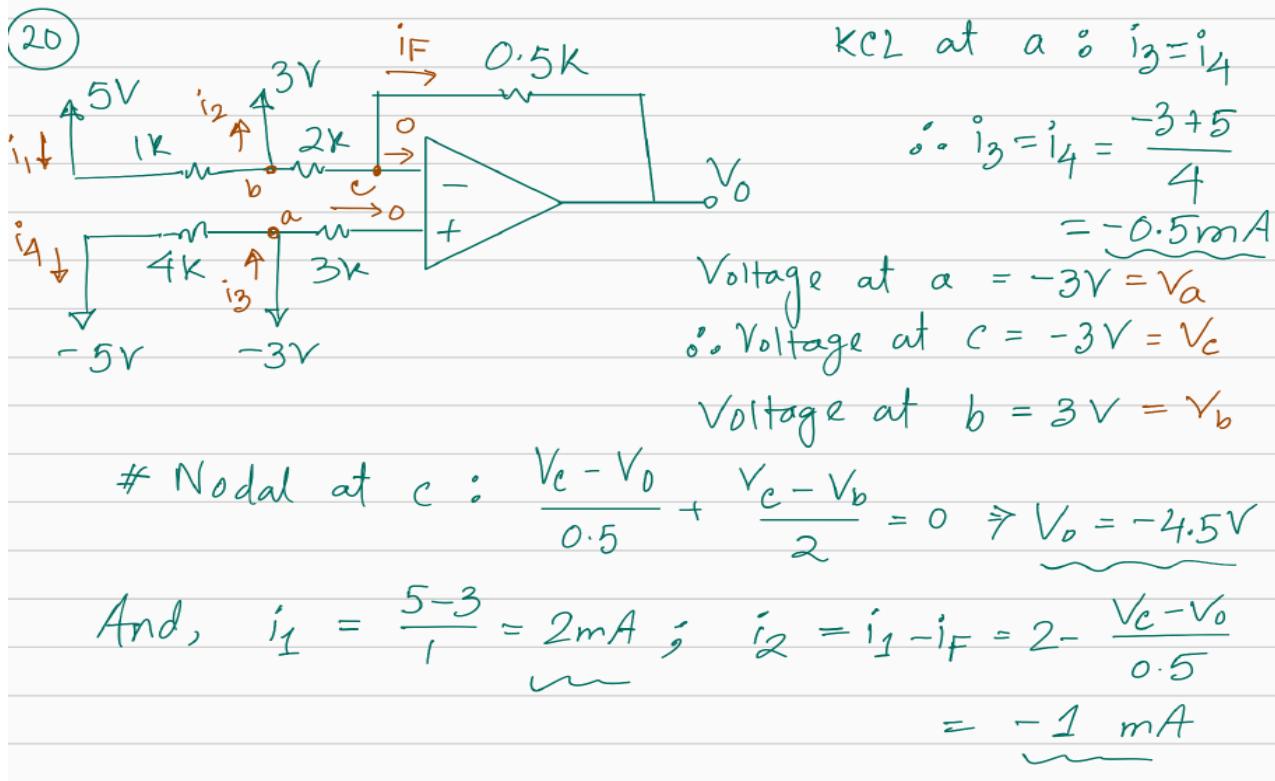
<https://youtu.be/KBWfa-NuYzk?list=PLPf6M92pkd7DRilBZLzKot-39S215ksSw&t=1198>

Additional Hint for finding V_X : Use Nodal Analysis on the V_X node instead of the current method shown in the video link above.

20. Miscellaneous

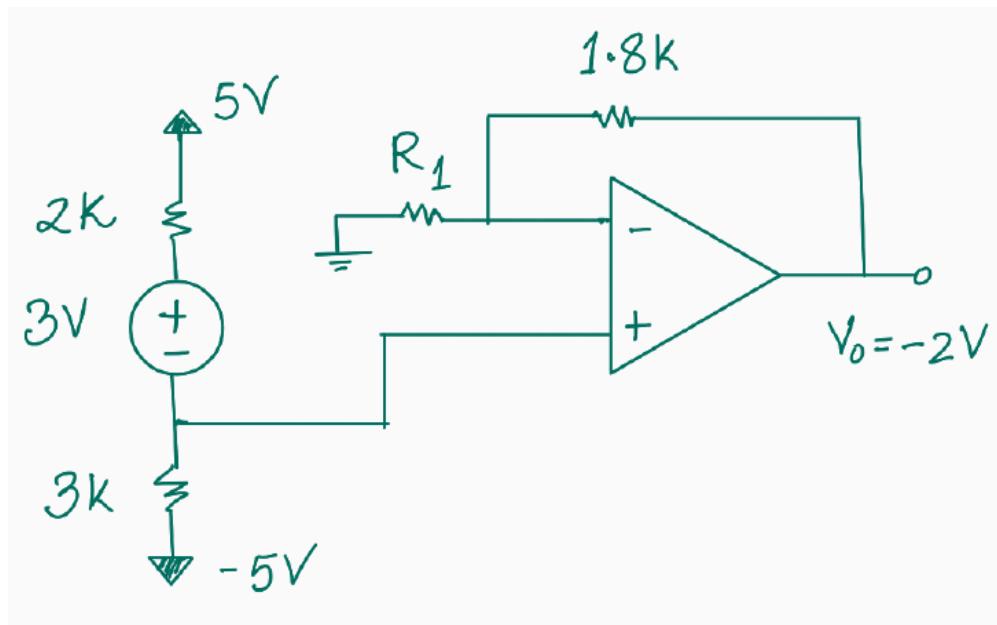
Determine the marked currents and the output voltage

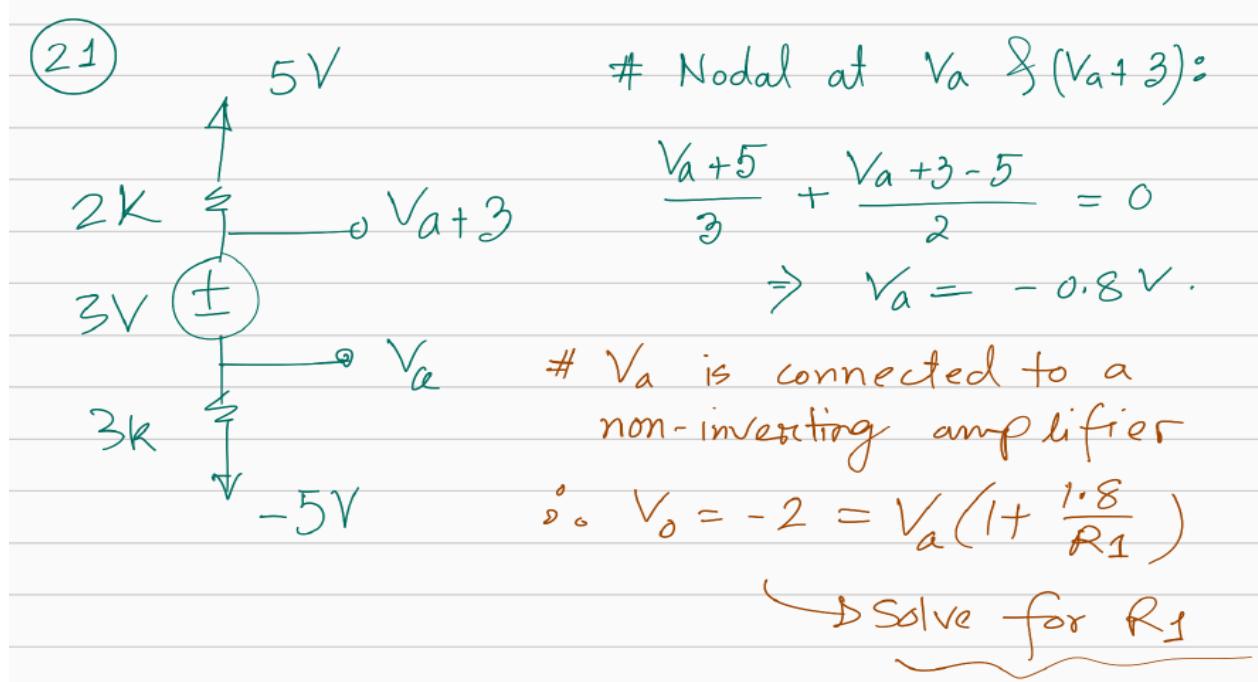




21. Miscellaneous

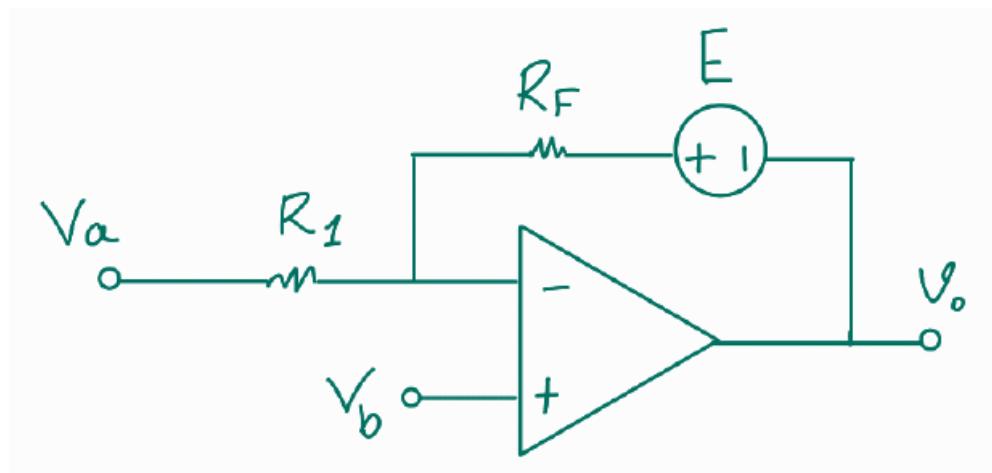
Determine the appropriate value of R_1





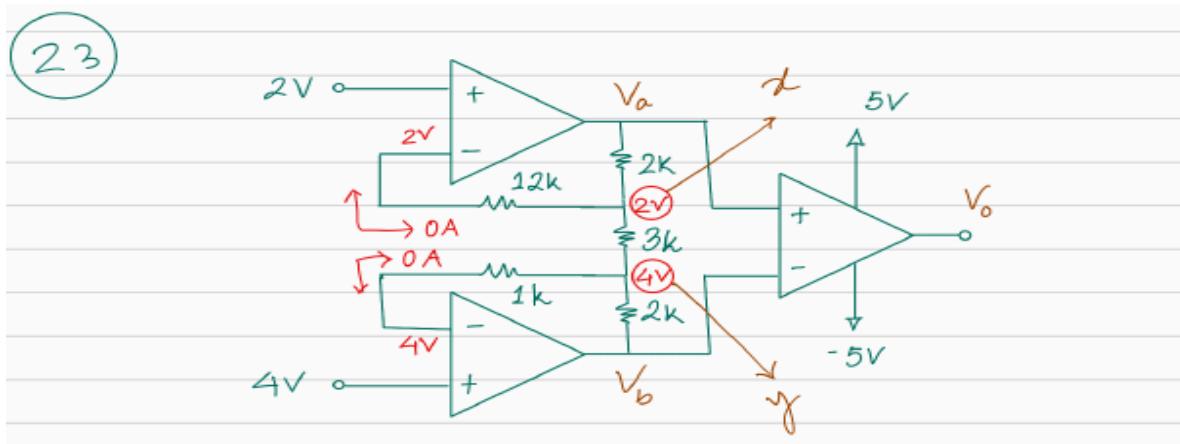
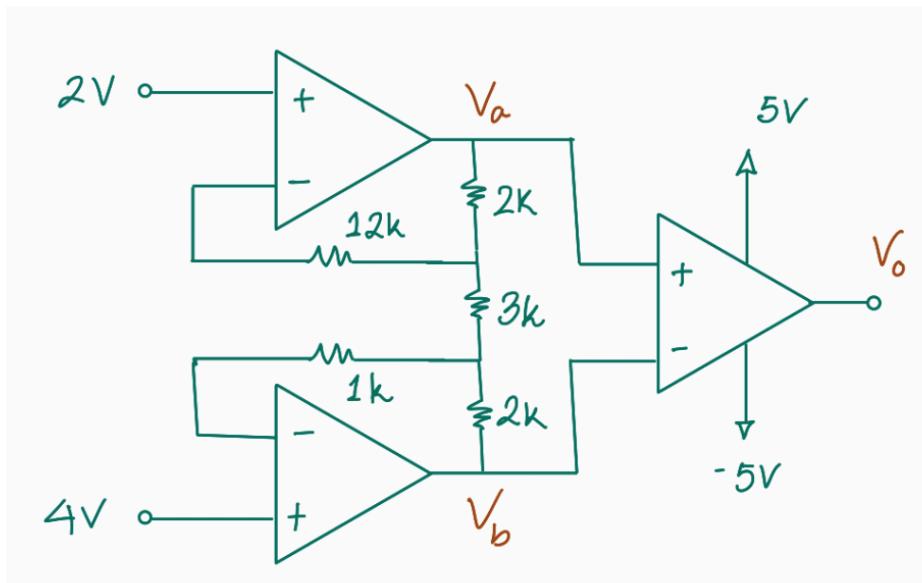
22. Miscellaneous

Express the output voltage v_o in terms of all the other quantities shown in the circuit below.



23. Miscellaneous

Determine the output of the comparator, V_o after finding V_a and V_b .



Applying Nodal on the x :

$$\frac{x - V_a}{2} + \frac{x - y}{3} = 0$$

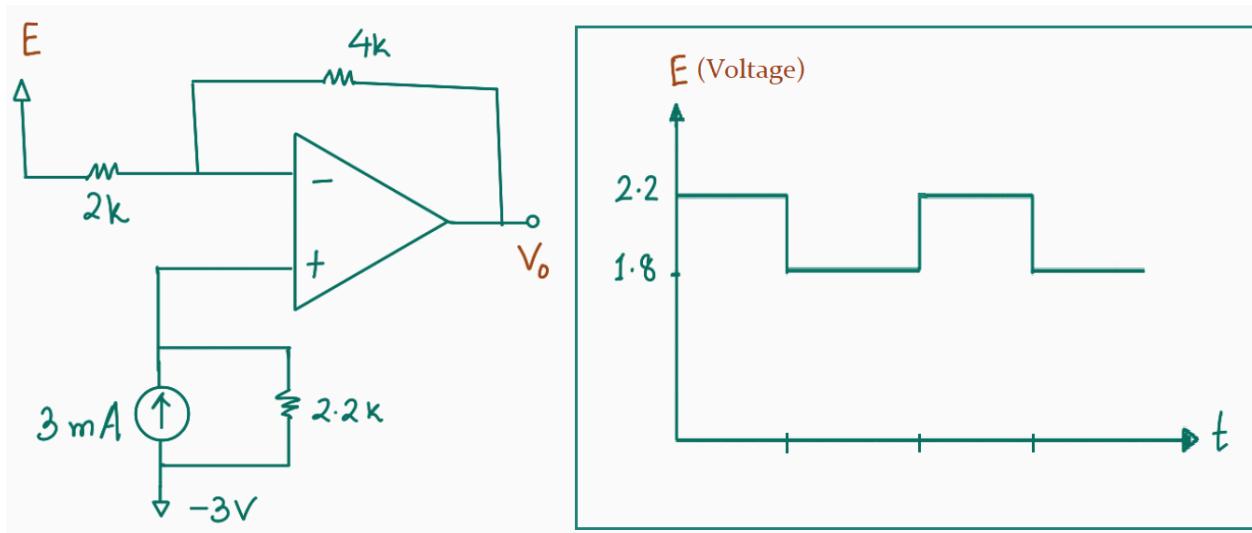
$$\Rightarrow \frac{2 - V_a}{2} + \frac{2 - 4}{3} = 0 \Rightarrow V_a = 0.67V$$

Also Nodal on y node : $V_b = 5.33V$

* For the comparator : $V_a < V_b$
 $\Rightarrow V^+ < V^-$
 $\therefore V_o = -5V$

24. Miscellaneous

Draw the correct waveform of V_0 (with voltage labels) alongside the input waveform of E .



$$V^+ = -3 + (2.2 * 3) = 3.6V \text{ [you may use source transformation here too]}$$

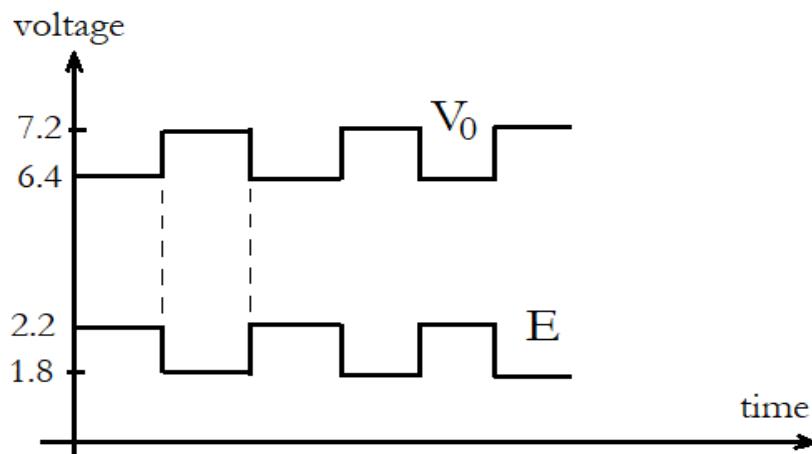
$$V^+ = V^- = 3.6V$$

When $E= 2.2V \Rightarrow$ Nodal Analysis at V^- :

$$(V^- - 2.2)/2 + (V^- - V_0)/4 = 0 \Rightarrow V_0 = 6.4V$$

When $E= 1.8V \Rightarrow$ Nodal Analysis at V^- :

$$(V^- - 1.8)/2 + (V^- - V_0)/4 = 0 \Rightarrow V_0 = 7.2V$$



25. Miscellaneous

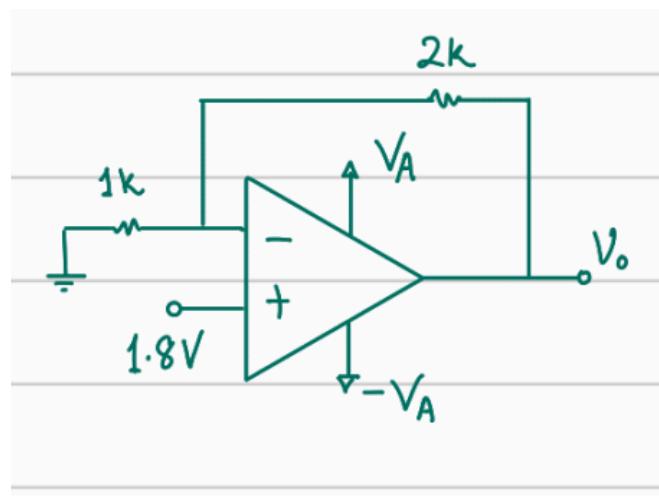
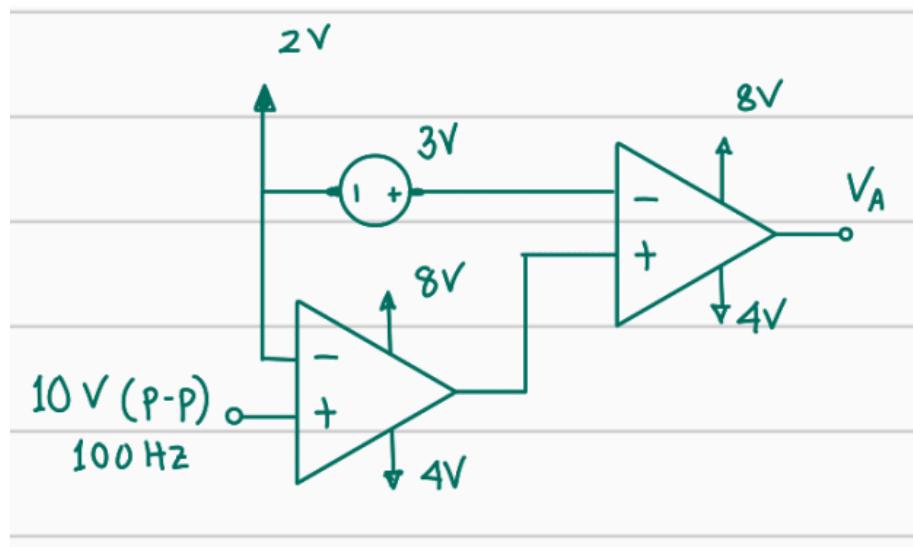
We know that the input-output relationship of an ideal inverting amplifier with op-amp is given by:

$$V_0 = -\frac{R_F}{R_1} V_{in}$$

However, realistic op-amps are non-ideal. Determine the input-output relationship of a **non-ideal inverting amplifier**. Use the equivalent circuit of an op-amp which contains A , R_i , R_o .

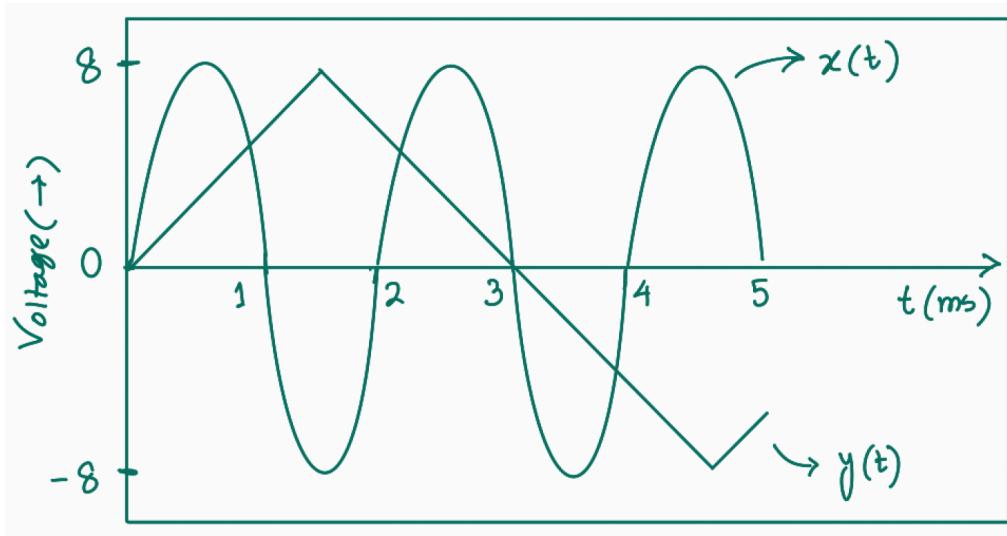
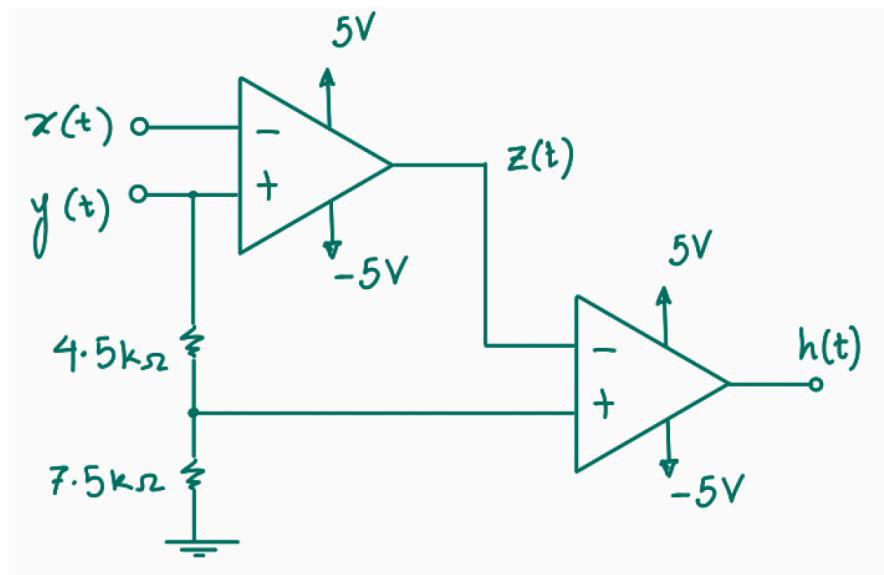
26. Miscellaneous

Draw the approximate waveforms of both V_A and v_0 from the circuit below.



27. Miscellaneous

After drawing both $z(t)$ and $h(t)$, determine the relation between them.

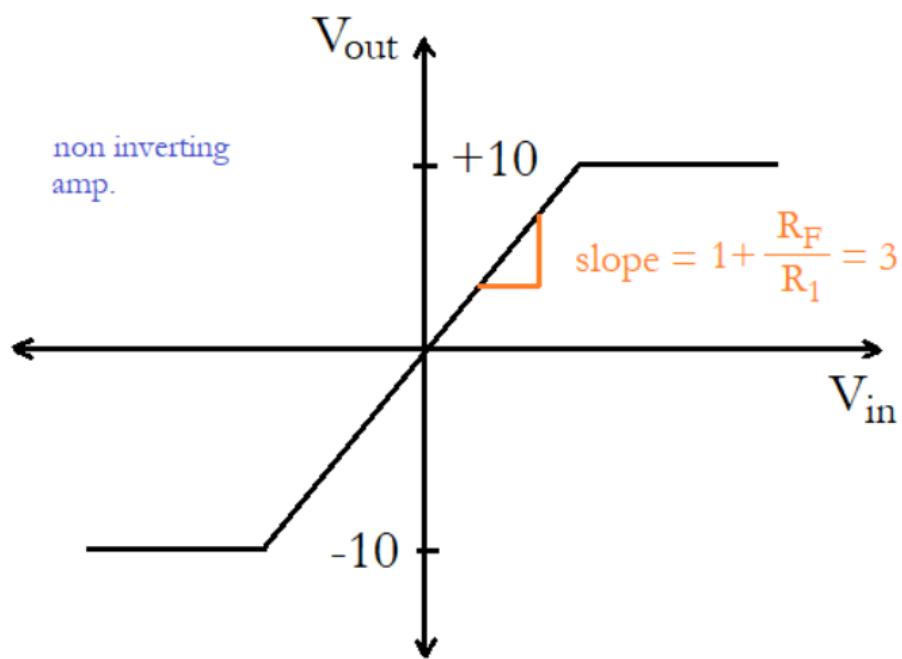
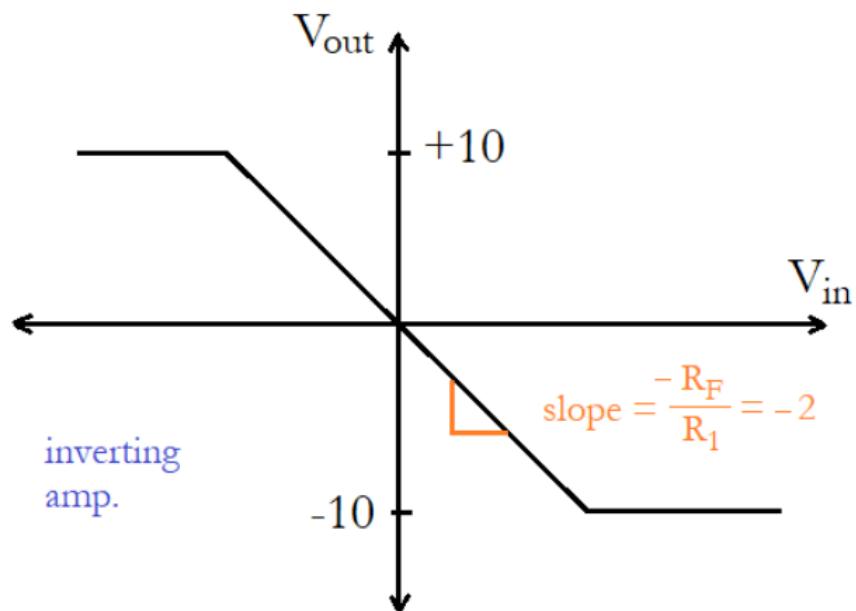


28. Miscellaneous

Draw the VTC of both an inverting and a non-inverting amplifier. The following information are known:

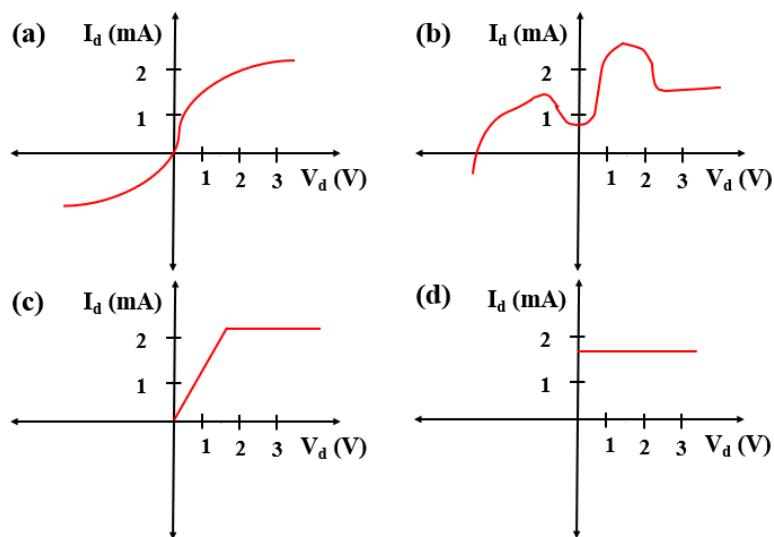
$$(i) \quad 2R_1 = R_F$$

$$(ii) \quad V_{sat}^+ = +10V, \quad V_{sat}^- = -10V$$



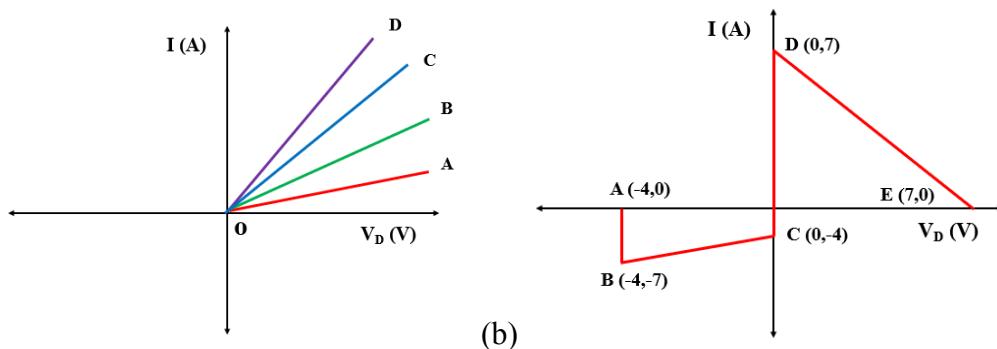
I-V

- Identify which of these I-V curves are Linear and which are Nonlinear:



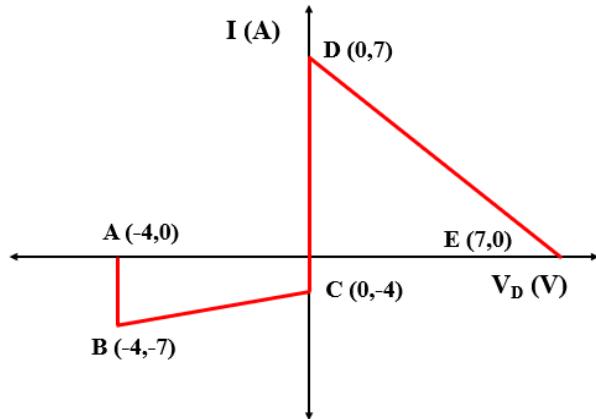
Ans: Linear: (d)

- Write down the slopes of these following regions in ascending order (you do not need to calculate the slopes)



Ans: (a) $|OA| < |OB| < |OC| < |OD|$, (b) Slopes of AB and CD are equal(infinity). The DE slope is negative. However, the value of slope is higher than BC here. $|BC| < |DE| < |AB|$

- Find out the slope of the following curves



Answer: Slope, $|m| = \left| \frac{y_2 - y_1}{x_2 - x_1} \right|$

$$|BC| = \left| \frac{y_2 - y_1}{x_2 - x_1} \right| = \left| \frac{-7 - 4}{-4 - 0} \right| = \frac{3}{4}$$

$$|DE| = \left| \frac{y_2 - y_1}{x_2 - x_1} \right| = \left| \frac{0 - 7}{7 - 0} \right| = 1 \quad [\text{Can you identify the issue in this curve?}]$$

$$|AB| = \left| \frac{y_2 - y_1}{x_2 - x_1} \right| = \left| \frac{-7 - 0}{-4 + 4} \right| = \infty$$

- Calculate and Show ‘C’ and ‘Io’ in the figures

[Hint: use $-\frac{V_o}{R} = Io = c$]

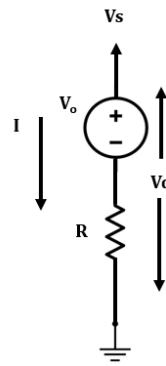
- Draw the alternative circuit diagram, I-V curve and calculate the parameters with the following information:

- $V_o = 5V, m = 2/k\Omega$
- $V_o = 3.5V, m = -2.5/k\Omega$
- $V_o = -5V, m = 5/k\Omega$

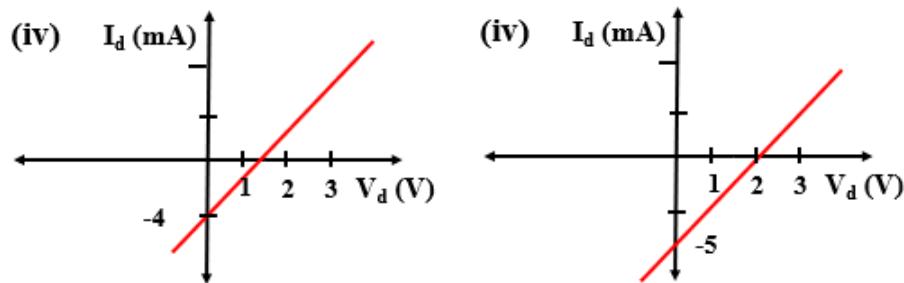
Solution:

- $|R| = \left| \frac{1}{m} \right|$ i.e. $\frac{1}{2} k\Omega, c = -\frac{V_o}{R} = -\frac{5}{0.5} mA = -2.5 mA$
- $|R| = \left| \frac{1}{m} \right|$ i.e. $\frac{1}{2.5} k\Omega, c = -\frac{3.5}{0.4} mA = -8.75 mA$
- $|R| = \left| \frac{1}{m} \right|$ i.e. $\frac{1}{5} k\Omega, c = -\frac{-5}{0.2} mA = 25 mA$

Alternative Diagram:

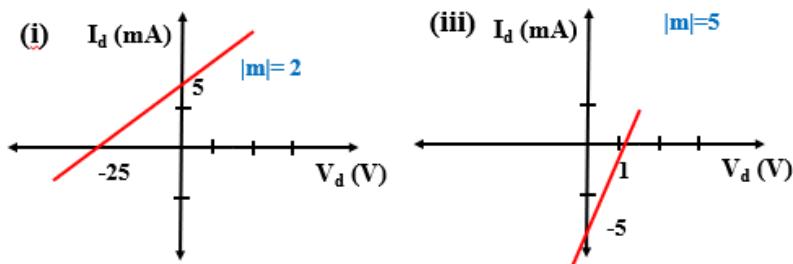


I-V curve:



- Calculate and Show 'C' and 'Vo' in the figures

[Hint: Use $IoR = - Vo$]



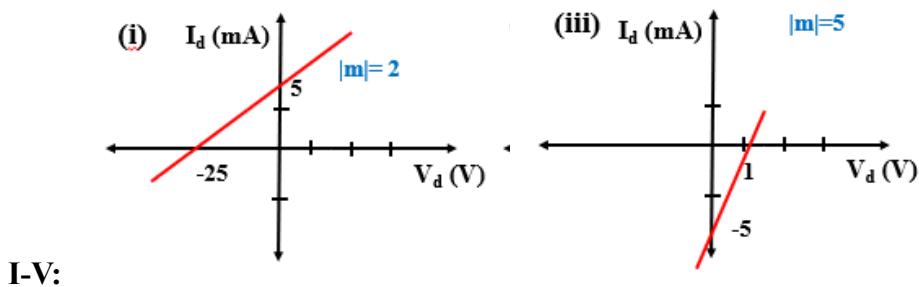
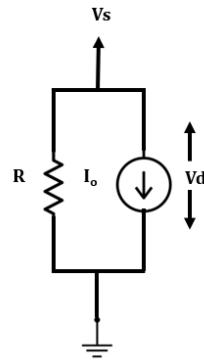
- Draw the alternative circuit diagram with the equivalent linear model, I-V curve and calculate the parameters with the following information:

- i. $Io = 5 \text{ mA}$, $m = 2/k\Omega$
- ii. $Io = 3.5 \text{ mA}$, $m = -2.5/k\Omega$
- iii. $Io = -5 \text{ mA}$, $m = 5/k\Omega$

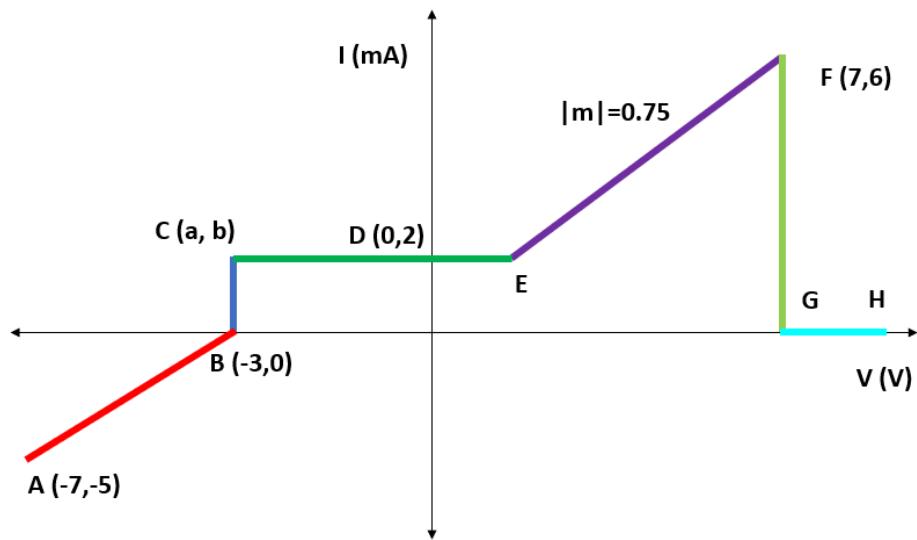
Solution:

- i. $|R| = |\frac{1}{m}|$ i.e. $\frac{1}{2} k\Omega$, $c = Io = 5 \text{ mA}$, $Vo = - IoR = - 2.5 \text{ V}$
- ii. $|R| = |\frac{1}{m}|$ i.e. $\frac{1}{2.5} k\Omega$, $c = Io = 3.5 \text{ mA}$, $Vo = - (- IoR) = 1.4 \text{ V}$; as m is negative
- iii. $|R| = |\frac{1}{m}|$ i.e. $\frac{1}{5} k\Omega$, $c = Io = - 5 \text{ mA}$, $Vo = - IoR = 1 \text{ V}$

Alternative diagram:



- From the I-V curve-
 - State the device model for each region,



Solution:

i.

AB: Voltage source in series with a resistor/ Current source in parallel with a resistor

BC: Voltage source

CD: Current source

EF: Voltage source in series with a resistor/ Current source in parallel with a resistor

FG: Voltage source

- A Voltage Source, $V_o = 10 \text{ V}$ in series with a resistor of $R = 3 \text{ k}\Omega$.
 - Write down the equation representing this curve
 - Determine the unknown parameters
 - Label the I-V curve

Solution:

- $y = mx + c$

Or, $I = m \cdot V_s - \frac{V_o}{R}$

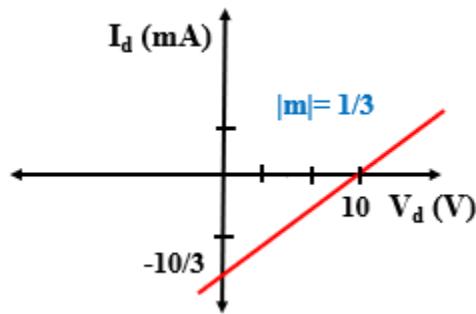
ii. $V_o = 10 \text{ V}$, $R = 3 \text{ k}\Omega$

$$|m| = \left| \frac{1}{R} \right| = \frac{1}{3}$$

Y axis intersection: $c = -\frac{V_o}{R} = -\frac{10V}{3k\Omega} = -\frac{10}{3} \text{ mA}$

X axis intersection: $V_o = 10 \text{ V}$

iii.



- A Voltage Source, $V_o = -10 \text{ V}$ in series with a resistor of $R = 3 \text{ k}\Omega$.
 - Write down the equation representing this curve
 - Determine the unknown parameters
 - Label the I-V curve

Solution:

- $y = mx + c$

Or, $I = m \cdot V_s - \frac{V_o}{R}$

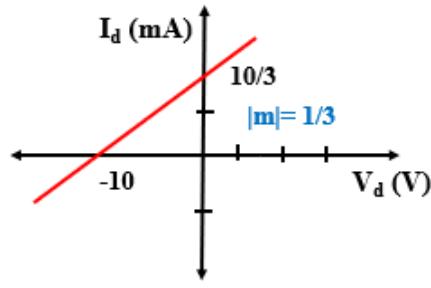
ii. $V_o = -10 \text{ V}$, $R = 3 \text{ k}\Omega$

$$|m| = \left| \frac{1}{R} \right| = \frac{1}{3}$$

Y axis intersection: $c = -\frac{V_o}{R} = -\frac{-10V}{3k\Omega} = \frac{10}{3} \text{ mA}$

X axis intersection: $V_o = -10 \text{ V}$

Iii.



- A Current Source, $I_o = 5 \text{ mA}$ in parallel with a resistor of $R = 5 \text{ k}\Omega$.

- i. Write down the equation representing this curve
- ii. Determine the unknown parameters
- iii. Label the I-V curve

Solution:

i. $y = mx + c$

Or, $I_s = \frac{V_s}{R} + I_o$

ii. $V_o = 10 \text{ V}$, $R = 5 \text{ k}\Omega$

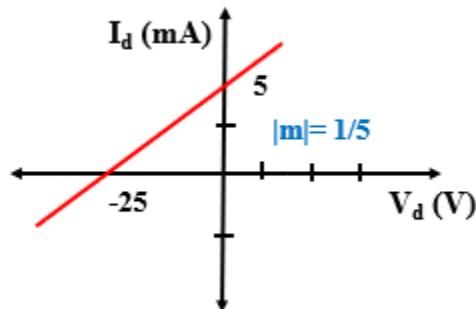
$|m| = \left| \frac{1}{R} \right| = \frac{1}{5}$

Y axis intersection : $c = I_o = 5 \text{ mA}$

X axis intersection: $I_o R = -V_o$

Or, $V_o = -5 * 5 \text{ V} = -25 \text{ V}$

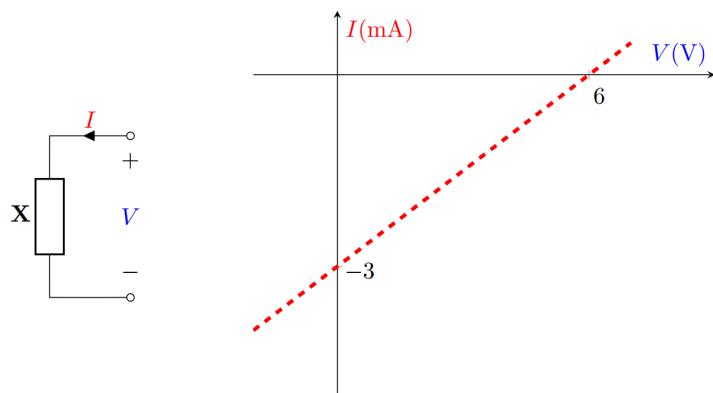
iii.



- You are provided with the following circuit elements:

- Two $1\text{ k}\Omega$ resistors
- A 4 V voltage source
- A 2 V voltage source

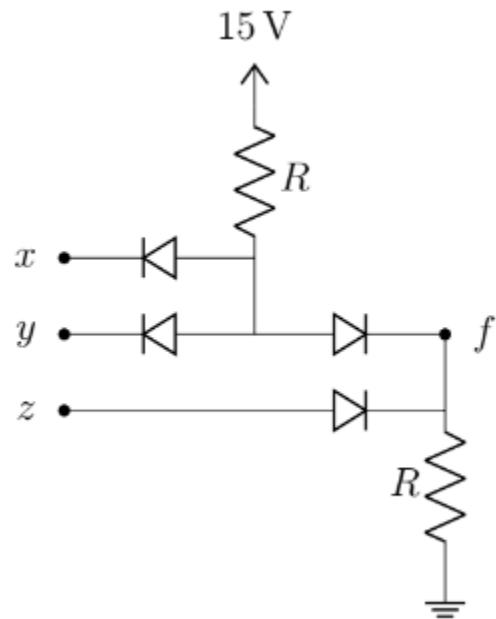
Can you implement a circuit element X that has an IV characteristics, as seen in the right figure below, but by **ONLY USING THE ELEMENTS MENTIONED ABOVE**? The voltage polarity and current direction should be as shown in the left figure.



Diode Logic Gates

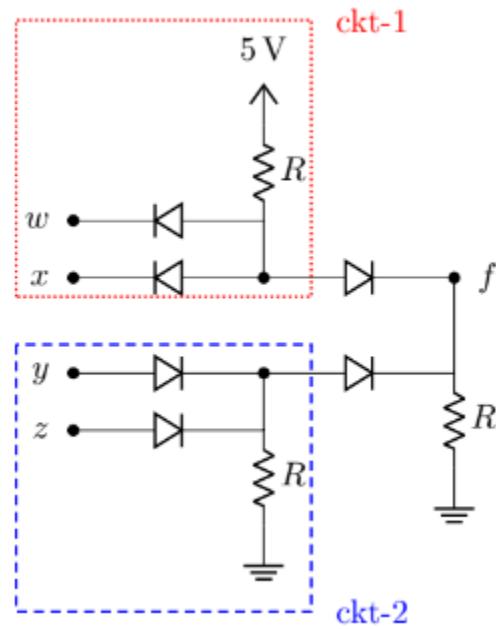
- Assuming x, y, z are boolean variables, analyze the circuits below to find an expression of “f” in terms of x, y, and z.

i.



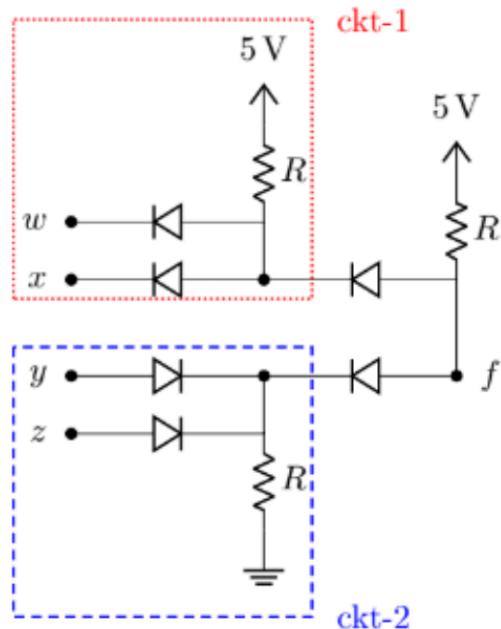
Soln: $f = (x \cdot y) + z$

ii.



$$\text{Soln: } f = (w \cdot x) + (y + z)$$

iii.



$$\text{Soln: } f = (w \cdot x) \cdot (y + z)$$

- Implement the following expressions using ideal diodes:
 - i. $xy + yz$
 - ii. XOR [Hint: Can you implement a NOT gate with a diode?]
 - iii. XNOR
 - iv. $(A+B)XY$
- Design a 4 input AND gate using ideal diodes
- Design a 3 input OR gate using ideal diodes
- There will be 5 questions from 5 different topics in your exam and you will have to answer 4 out of these . You will need to fulfill the following conditions-
 - i. You **must** answer 3 questions from topic “A”, “B” and “C”
 - ii. You can answer one question from **either** “D” or “E”

Deduce the logic function using boolean variables A,B,C,D and E to implement your algorithm for choosing the questions.

- For this question, assume all the diodes are ideal.

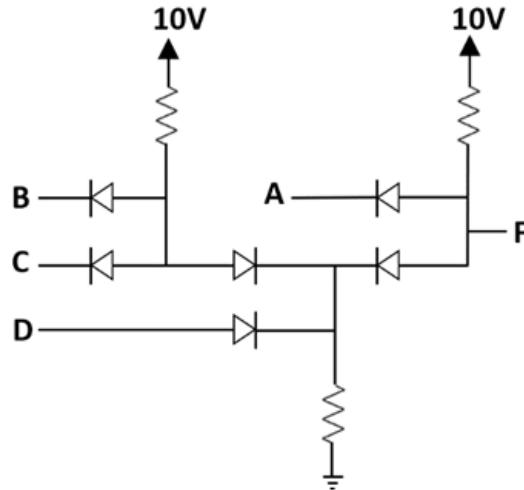


Figure 1

- (a) Assuming A, B, C, D are boolean variables, analyze the circuit of Figure 1 to find an expression of F in terms of A, B, C and D.

Solution: $F = (B \cdot C + D) \cdot A$

- (b) Analyze the circuit in Figure 1 to find the output voltage(s) F and complete the table in Figure 2, assuming A, B, C and D are voltage signals

A	B	C	D	F
4V	3V	4V	6V	
5V	3V	4V	2V	
13V	3V	4V	15V	

Figure 2

Hint: AND gate $\rightarrow \min(\)$ operation, OR gate $\rightarrow \max(\)$ operation

- (c) Design a circuit using ideal diodes to implement the logic function

$$f = (x+y)z$$

- Maisha is designing a game where she needs to determine an algorithm for level upgrades. The quests in level-1 are expressed using Boolean variables A, B, C, D, and E. For upgrading from level-1 to level-2 she will need to fulfill the following conditions-

- Quest “A” and “B” must be completed
- At Least one quest has to be completed from “C”, “D” and “E”

(a) **Deduce** the logic function, F, using Boolean variables A, B, C, D, and E to implement Maisha’s algorithm. [3]

(b) **Determine** the values of “F” in the following table using the logic function from (a). [2]

A	B	C	D	E	F
0	0	1	0	1	?
0	1	1	1	0	?
1	0	0	0	0	?
1	1	1	0	0	?

(c) **Draw** the circuit diagram implementing the logic function from (a). [3]

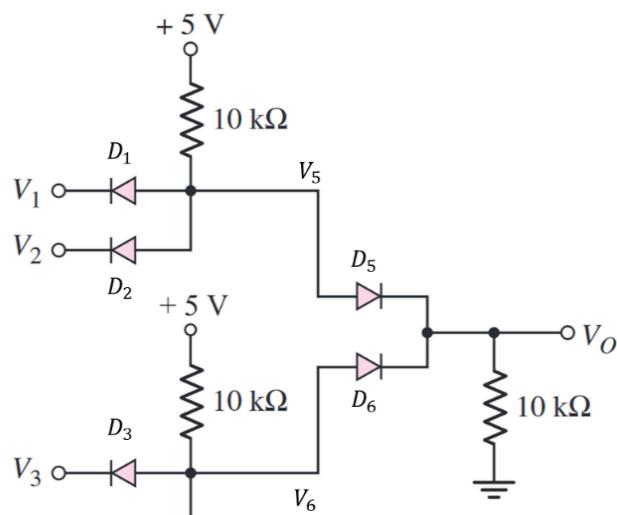
(d) **Discuss** whether you can design a NAND gate with Si diodes. [2]

Solution:

NAND gates require AND gate and NOT gate to implement. We can build AND gates using Si diodes. But we cannot implement NOT gate using Si diodes. So, we cannot implement NAND gate with Si diodes as it is dependent on NOT gate’s implementation using Si diode.

- In the adjacent figure we have the following parameters:

$$\begin{aligned}
 V_{D1} &= 0.3 \text{ V}, & V_1 &= 2 \text{ V} \\
 V_{D2} &= 0.5 \text{ V}, & V_2 &= 1.7 \text{ V} \\
 V_{D3} &= 0.7 \text{ V}, & V_3 &= 1.5 \text{ V} \\
 V_{D4} &= 0.9 \text{ V}, & V_4 &= 1.1 \text{ V} \\
 V_{D5} &= V_{D6} = 1.1 \text{ V}
 \end{aligned}$$



- Find V_5 and V_6 . [5]
- Find V_O . [5]

- iii. [BONUS – 5 Marks]: Solve the circuit to get V_o when $V_1 = 7 V$, $V_2 = 8 V$ and all other parameters remain the same.

Solution:

$$V_5 = \min(V_1 + V_{D1}, V_2 + V_{D2}) = \min(2.3, 2.2) = 2.2 V$$

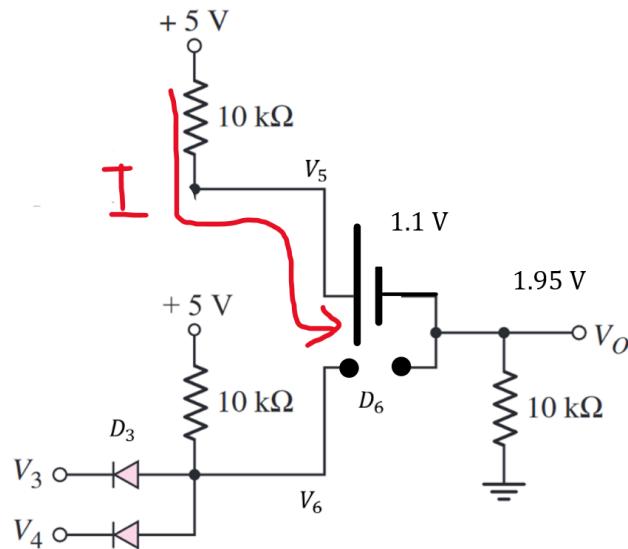
$$V_6 = \min(V_3 + V_{D3}, V_4 + V_{D4}) = \min(2.2, 2.0) = 2.0 V$$

$$V_o = \max(V_5 + V_{D5}, V_6 + V_{D6}) = \max(2.2 - 1.1, 2.0 - 1.1) = 2.2 - 1.1 V = 1.1 V$$

Bonus:

When $V_1 = 7 V$ and $V_2 = 8 V$, D_1 and D_2 are both in reverse bias as both V_1 and V_2 are greater than the 5 V supply voltage. So, between V_5 and V_6 (which is still 2.0 V, as obtained from previous answer), the higher voltage will propagate to V_o . But, we still don't know what V_5 is.

So, here is what we will do. We will assume for now that V_5 is higher than V_6 . As, both diodes will not simultaneously be forward biased, D_5 is assumed to be forward biased. So the circuit becomes:



From the above circuit, $I = (5 - 1.1)/(10 + 10) mA = 0.195 mA$ and $V_5 = 5 - 10I = 3.05 V$.

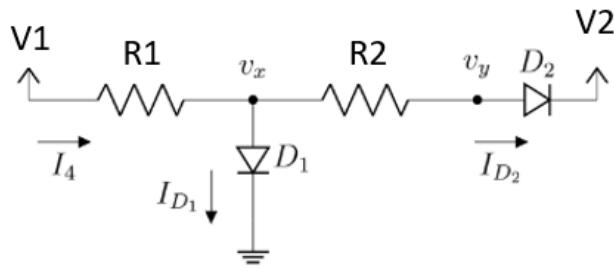
Here, $V_5 = 3.05 V > V_6(2 V)$. So, our assumption that V_5 is higher than V_6 is true. So, the result is:

$$V_o = 3.05 - 1.1 V = 1.95 V (\text{Answer})$$

Diode: Method of assumed states

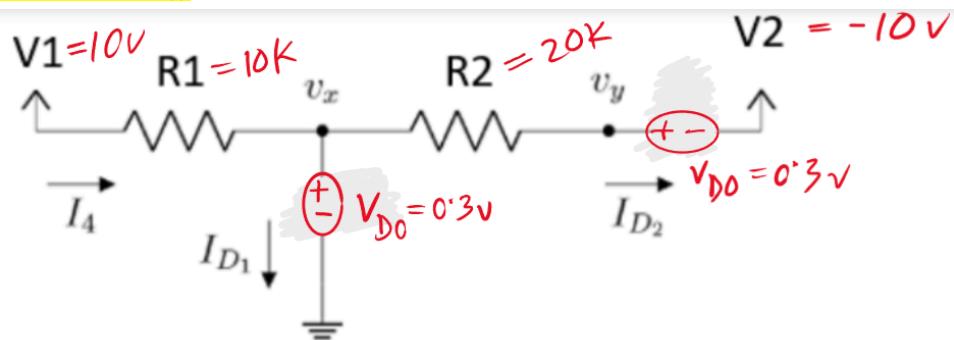
For the following circuits (a) Analyze the following circuit to find the values of I_{D1} , I_{D2} , V_x and V_y . Here, use the Method of Assumed State using the CVD model of diode with $V_{D0} = 0.3$ V. (b) Validate your assumptions about the states of the diodes.

1.



- i. $V1 = 10$ V, $V2 = -10$ V, $R1 = 10$ K, $R2 = 20$ K
- ii. $V1 = -5$ V, $V2 = 20$ V, $R1 = 10$ K, $R2 = 20$ K

Solution ==> (i)



Assumption $\rightarrow D_1, D_2$ both ON

Calculation

$$V_x = 0.3 \text{ V}$$

$$V_y = (-10 + 0.3) \text{ V} = -9.7 \text{ V}$$

$$I_q = \frac{10 - V_x}{R_1} = \frac{10 - 0.3}{10 \text{ K}} = 0.97 \text{ mA}$$

$$I_{D2} = \frac{V_x - V_y}{R_2} = \frac{0.3 - (-9.7)}{20 \text{ K}} = 0.5 \text{ mA}$$

$$\text{Now, } I_q = I_{D1} + I_{D2}$$

$$\hookrightarrow I_{D1} = I_q - I_{D2}$$

$$\hookrightarrow I_{D1} = (0.97 - 0.5) \text{ mA}$$

$$\hookrightarrow I_{D1} = 0.47 \text{ mA}$$

Verification

$$\text{for } D_1 \rightarrow i_{D1} > 0$$

$$\hookrightarrow 0.47 \text{ mA} > 0 \quad \swarrow$$

True

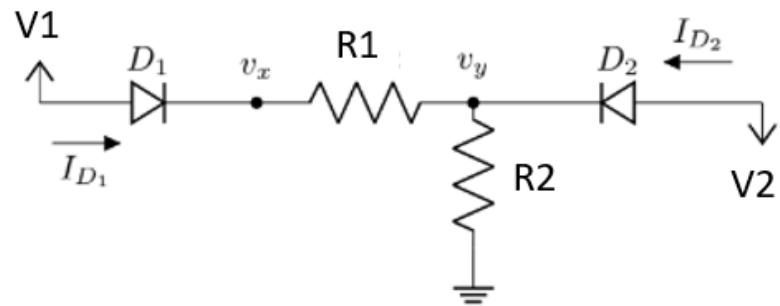
$$\text{for } D_2 \rightarrow i_{D2} > 0$$

$$\hookrightarrow 0.5 \text{ mA} > 0 \quad \swarrow$$

True

∴ Assumption correct.

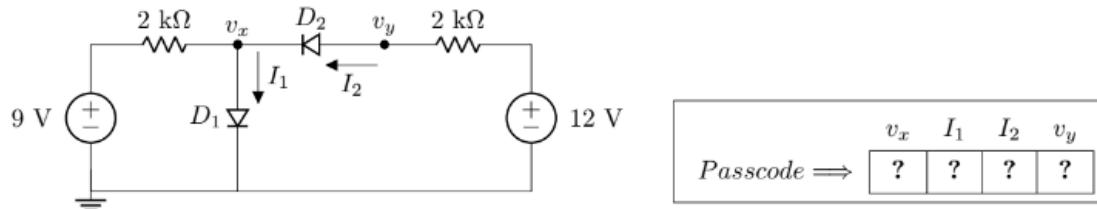
2.



- i. $V_1 = 5 \text{ V}$, $V_2 = -3.5 \text{ V}$, $R_1 = 1 \text{ K}$, $R_2 = 10\text{K}$
- ii. $V_1 = 5 \text{ V}$, $V_2 = -3.5 \text{ V}$, $R_1 = 10 \text{ K}$, $R_2 = 10\text{K}$

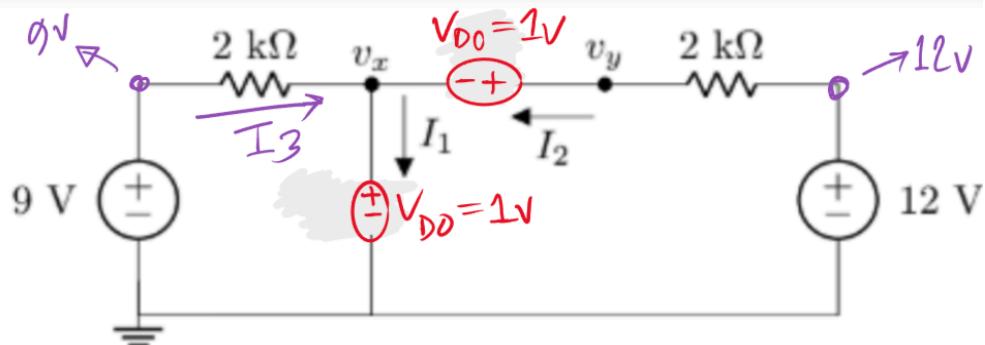
3.

Sherlock Holmes found a piece of paper from the pocket of one of Professor Moriarty's victim with the circuit shown below. One side of the paper is missing and the only other available information was that the **D1 diode is on**. Sherlock needs to know the values of v_x , v_y , I_1 , and I_2 as it generates the passcode for the victim's locker, which can help him catch Moriarty. Sherlock knows nothing about diodes and asked for your help to solve the case.



- (a) Show the alternative representation of the given circuit. [1.5]
- (b) Analyze the circuit to calculate the values of v_x , v_y , I_1 and I_2 , and hence the passcode. You must validate your assumption. Use the constant voltage drop model with a forward voltage drop, $V_{D0} = 1\text{ V}$. [5+2]
- (c) Passive sign convention states that a device is delivering power if $p = v \times I$ for the device is negative, and consuming power if p is positive. Deduce whether D_1 is consuming or delivering power. [1.5]

Solution \Rightarrow part-b



Assumption $\rightarrow D_1, D_2$ both ON

Calculation

$$v_x = 1\text{ V}, v_y = v_x + 1 = 2\text{ V}$$

$$I_3 = \frac{9 - v_x}{2k} = \frac{9 - 1}{2k} = 4\text{ mA}$$

$$I_2 = \frac{12 - v_y}{2k} = \frac{12 - 2}{2k} = 5\text{ mA}$$

$$I_1 = I_3 + I_2 = (4 + 5) \text{ mA} = 9 \text{ mA}$$

Verification

for $D_1 \rightarrow i_{D1} > 0$

$$\hookrightarrow I_1 > 0$$

$$\hookrightarrow 9 \text{ mA} > 0 \rightarrow \text{True}$$

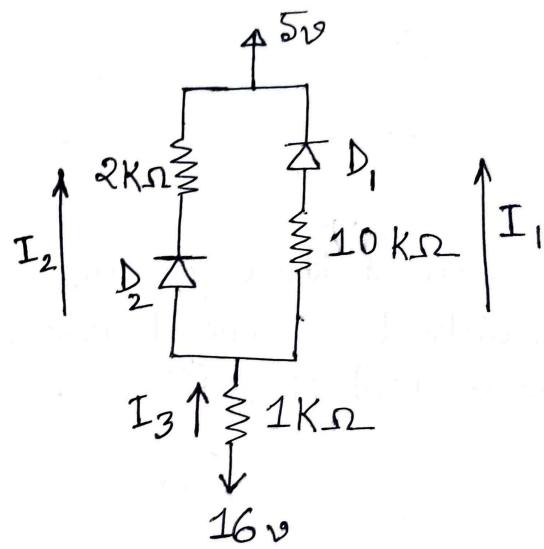
for $D_2 \rightarrow i_{D2} > 0$

$$\hookrightarrow I_2 > 0$$

$$\hookrightarrow 5 \text{ mA} > 0 \rightarrow \text{True}$$

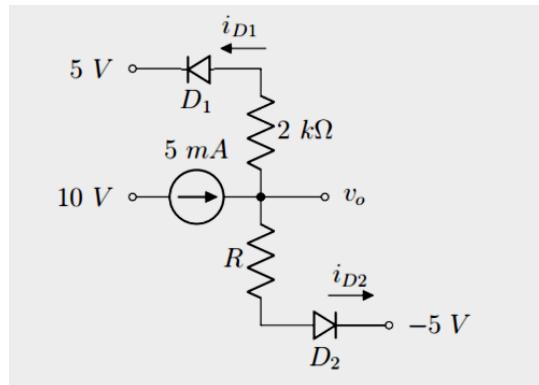
So, Assumption Correct.

4.



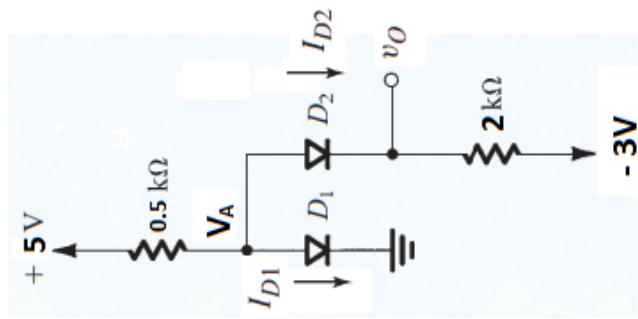
Analyze the circuit given above. Calculate the values of I_1 , I_2 , I_3 . You must validate your assumptions. Use the Constant-Voltage Drop model(CVD Model) with $V_{D0} = 0.8 \text{ V}$.

5.



Find V_o , i_{D1} and i_{D2} for $R = 1 \text{ k}\Omega$. Assume diode constant voltage drop model with $V_{D0} = 0.7 \text{ V}$. In each case, write down the states of the diodes (ON/OFF). You must verify your assumptions.

6.



Analyze the following circuit. Calculate the values of V_A , V_0 , I_{D1} , and I_{D2} . You must validate your assumptions. Use the Constant-Voltage Drop model with a cut in voltage of 0.6V [$V_{D0}=0.6V$].
[Hints: You may start with calculating the voltage values first]

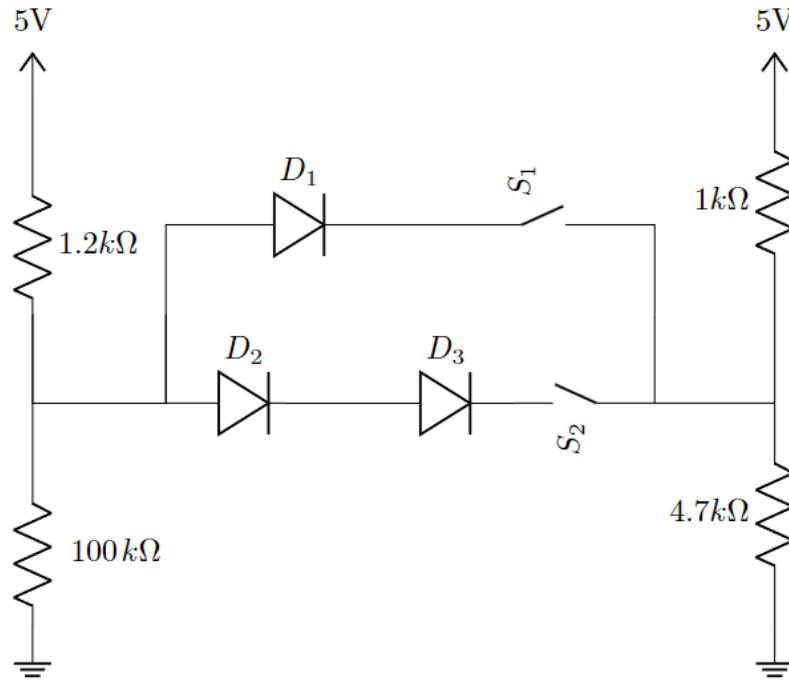
- Please find some other examples here: [Week 4 \(Method of Assumed State Examples\).pdf](#)

7.

The switches S1 and S2 are shown in open configuration below.

Assume, $V_{D0} = 0.7V$ (CVD model)

- Find the current passing through the $100k\Omega$ resistor when only S1 is closed.
- Find the current passing through the $100k\Omega$ resistor when only S2 is closed.



(i) Assume, D1 is on

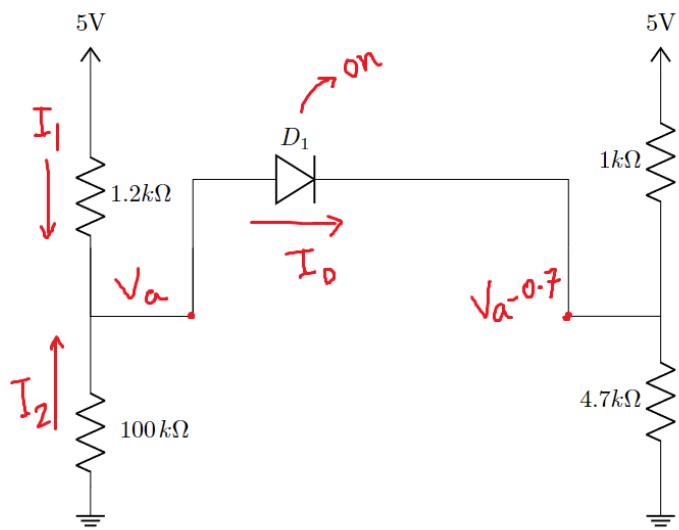
Nodal Analysis at V_a :

$$\begin{aligned}(V_a - 5)/1.2 + V_a/100 + \\ (V_a - 0.7)/4.7 + (V_a - 0.7 - 5)/1 = 0\end{aligned}$$

$$\Rightarrow V_a = 4.871 \text{ V}$$

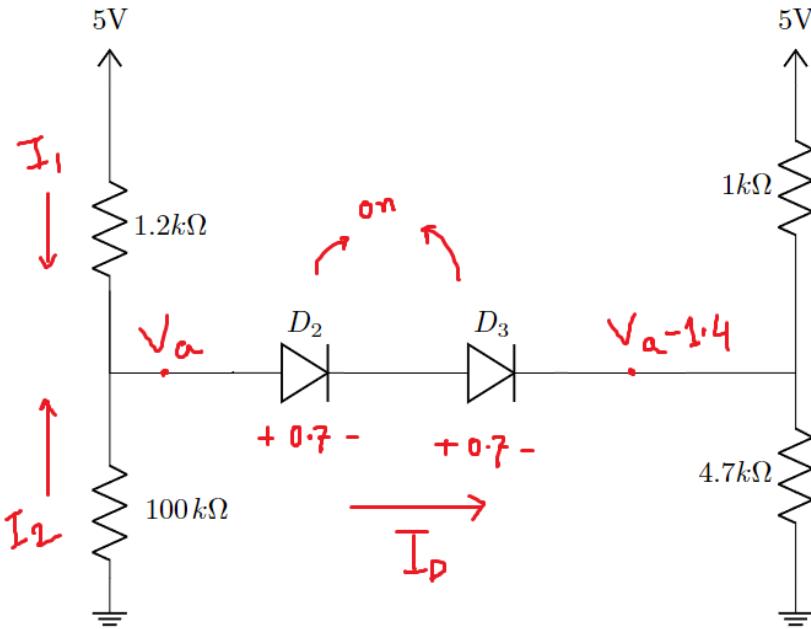
$$\begin{aligned}\therefore I_D &= I_1 + I_2 \\ &= (5 - V_a)/1.2 + (0 - V_a)/100 \\ &= 0.059 \text{ mA} > 0\end{aligned}$$

[Assumption correct]



Ans: I_2 or $-I_2$

(i) Assume, both D₂ and D₃ is on



Nodal Analysis at V_a:

$$(V_a - 5)/1.2 + V_a/100 + (V_a - 1.4)/4.7 + (V_a - 1.4 - 5)/1 = 0$$

$$\Rightarrow V_a = 5.284 \text{ V}$$

$$\begin{aligned} \therefore I_D &= I_1 + I_2 \\ &= (5 - V_a)/1.2 + (0 - V_a)/100 \\ &= -0.29 \text{ mA} < 0 \end{aligned}$$

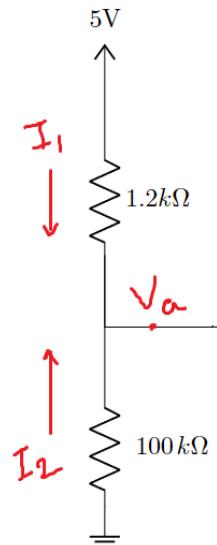
[Assumption Invalid : both diode will remain off as they are in series]

Therefore, the middle circuit will not be included.

The current inside 100k needs to be recalculated from the ckt drawn on the right.

$$I_2 = -I_1 = -5/(1.2 + 100) = -0.049 \text{ mA}$$

Ans: - 0.049 or 0.049 mA



Rectifiers

1.

The input of a full-wave rectifier is a cosine voltage with peak $V_M = 5$ V and frequency 60 Hz, and output load resistance is $R = 2$ k Ω . Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.7$ V.

(a) Briefly explain the purpose of a rectifier and describe its operation.

(b) Show the input and output waveforms.

(c) Calculate the DC value of the output voltage.

Now after connecting a capacitor in parallel with the load, the output becomes a ripple voltage $V_{\text{out}} = V_{DC} \pm 0.2$ V

(d) Calculate the **peak-to-peak ripple voltage**, and from that, the value of the capacitor.

(e) Calculate the average of the output voltage V_{DC} after connecting the capacitor. Compare this with the DC value determined in 'c' and comment on the difference between these two.

2.

The input of a **Half-wave rectifier** is a sine voltage with peak $VM = 10$ V and frequency 55 Hz, and output load resistance is $R = 2.5$ k Ω . Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.4$ V.

(a) Calculate the DC value of the output voltage.

Now after connecting a capacitor in parallel with the load, the output becomes a ripple voltage $V_{\text{out}} = V_{DC} \pm 0$ V.

(d) Calculate the **peak-to-peak ripple voltage**, and from that, the value of the capacitor.

(e) Calculate the average of the output voltage V_{DC} after connecting the capacitor. Compare this with the DC value determined in 'c' and comment on the difference between these two.

(f) Draw the **Voltage Transfer Characteristic (VTC) curve**

3.

The input of a full-wave rectifier is expressed by, $V_s(t) = 7\sin(400\pi t)$, and output load resistance is $R = 5$ k Ω . Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.3$ V.

(a) Calculate the input and output wave frequency.

(b) Show the input and output waveforms.

(c) Calculate the DC value of the output voltage.

Now after connecting a capacitor, $C = 100$ μF in parallel with the load.

(d) Calculate the peak-to-peak ripple voltage,

(e) Calculate the average of the output voltage V_{DC} after connecting the capacitor. Compare this with the DC value determined in 'c' and comment on the difference between these two.

(f) How can you provide better filtering for the output waves?

(g) What is the frequency of the Ripple voltage?

4.

The input of a **Half-wave rectifier** is a **Square** wave voltage with peak $V_M = 15$ V and frequency 0.5 Hz, and output load resistance is $R = 5 \text{ k}\Omega$. Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.7$ V.

i. Show the input and output waveforms.

ii. Draw the VTC curve

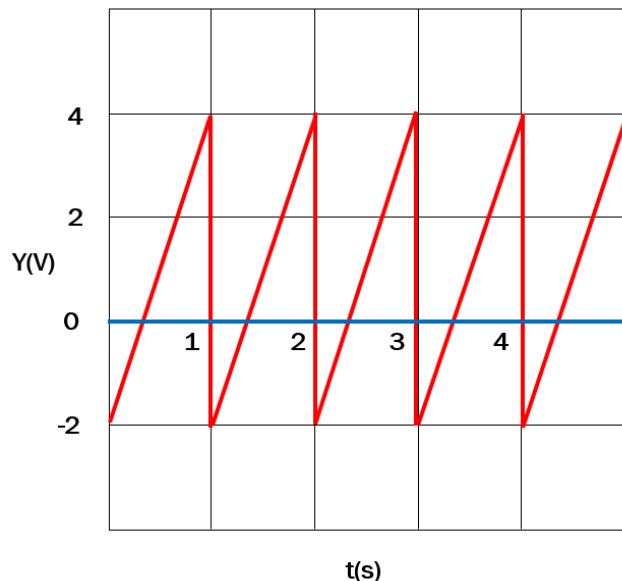
5.

The input of a **full-wave rectifier** is a **Square** wave voltage with peak $V_M = 15$ V and frequency 0.5 Hz, and output load resistance is $R = 5 \text{ k}\Omega$. Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.7$ V.

i. Show the input and output waveforms.

ii. Draw the VTC curve

6.



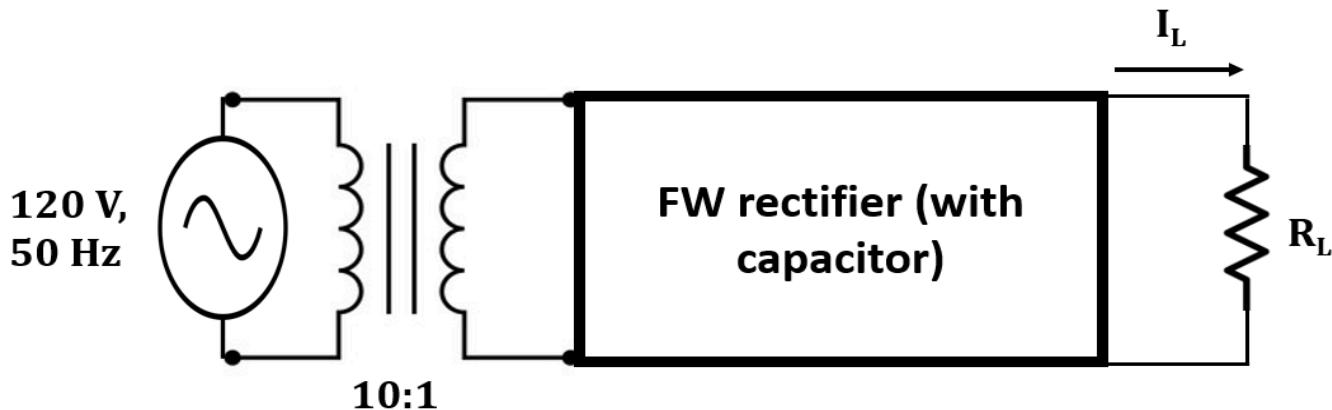
The input of a Half-wave rectifier is exhibited in the Figure above and output load resistance is $R = 5 \text{ k}\Omega$. Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.7$ V.

i. Show the input and output waveforms.

ii. Draw the VTC curve

7.

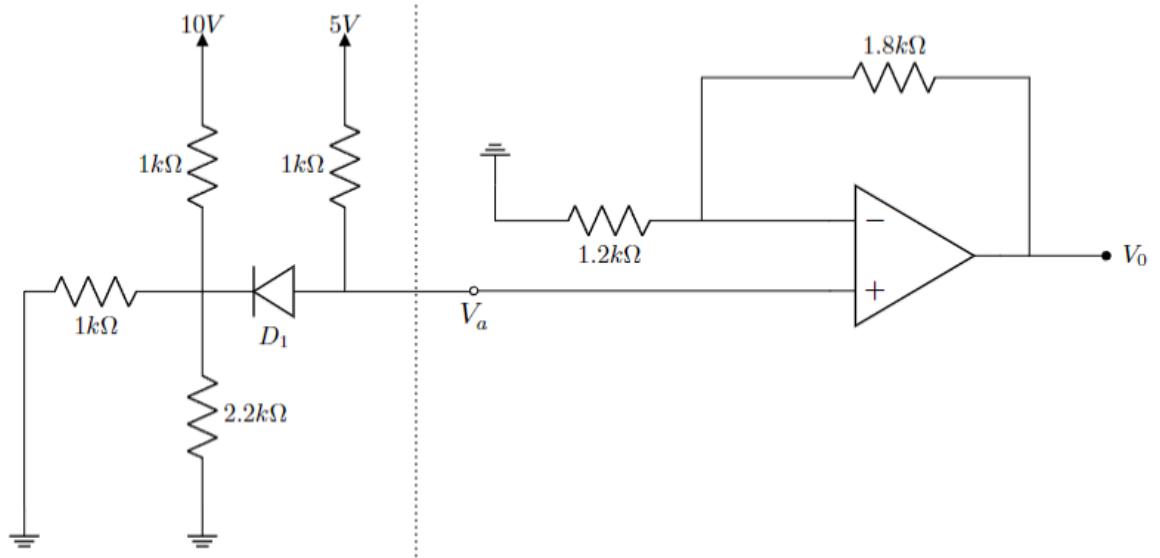
A full-wave rectifier is designed to deliver a maximum current $I_L = 120 \text{ mA}$ to the load. The rectifier produces an output with a ripple of 5% of the peak output voltage. An input line voltage of 120 V (peak), 50 Hz is available. A 10:1 step-down transformer is used to transform the supply voltage to 12 V (peak).



- (a) Draw the Voltage Transfer Characteristics of the full-wave rectifier. [2]
- (b) Calculate the peak output voltage. [1]
- (c) Determine the value of the Load Resistor to deliver a maximum load current of 120mA. [2]
- (d) Deduce the value of the Capacitor and the DC average value. [1]
- (e) Assume the transformer is removed and the rectifier is directly connected to the AC power supply line. Discuss the state of the diodes. [Hint: use the Peak Input Value of the rectifier input] [3]

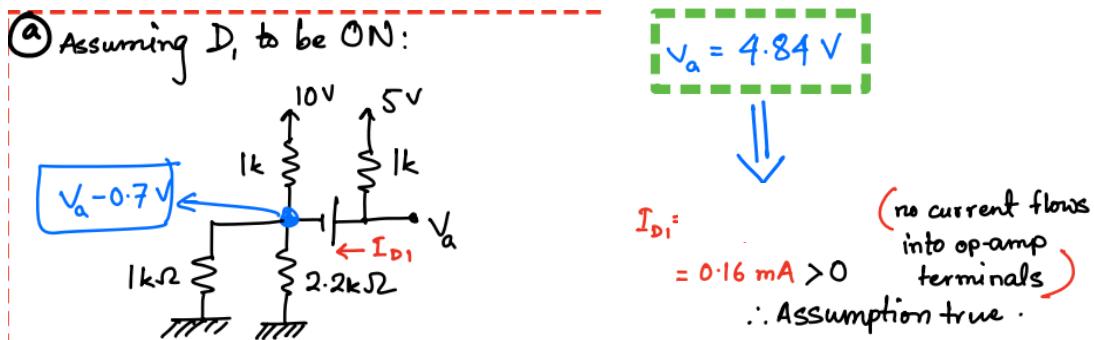
Hybrid Problems

1.



The saturation voltages of the Op-Amp are given as- $V_{sat}^+ = +10V$ and $V_{sat}^- = -10V$. The forward voltage drop of the diode, V_D is 0.7V.

- (a) Determine the operating mode diode, D_1 . Verify your assumption with necessary calculations.
- (b) Calculate the voltage at - (i) node 'Va', (ii) non-inverting terminal of the Op-Amp, (iii) inverting terminal of the Op-Amp.
- (c) Find out the output voltage, V_o of the Op-Amp.



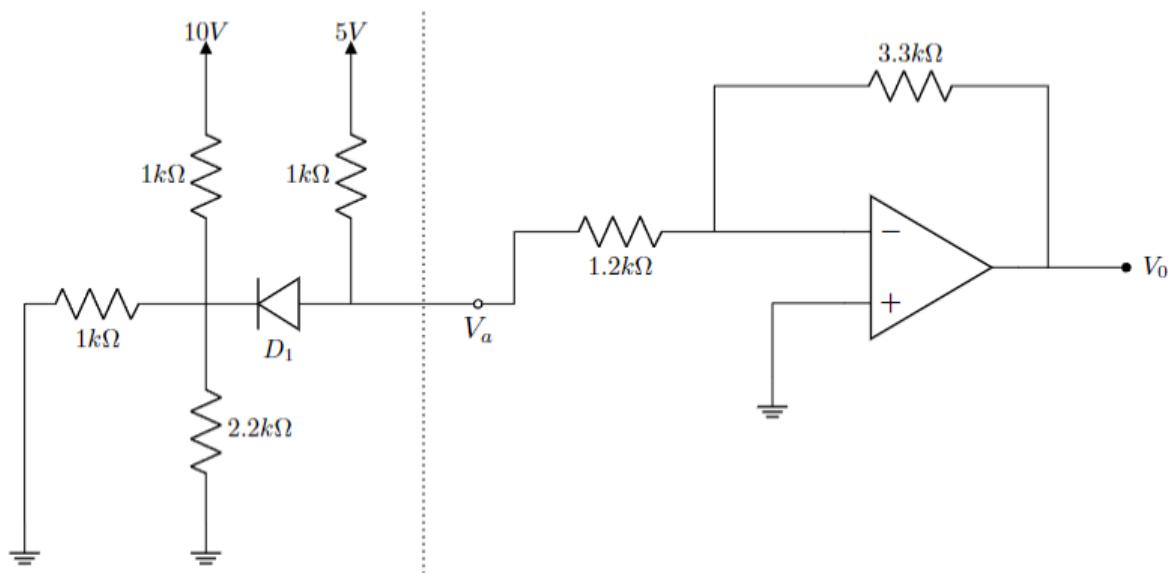
Node equation at supernode (V_a)

$$(V_a - 0.7) \left(1 + \frac{1}{2.2}\right) + V_a - 10 - 5 = 0$$

$$V_o = (1 + 1.8/1.2) * V_a$$

$V_a = 4.84V$

2.

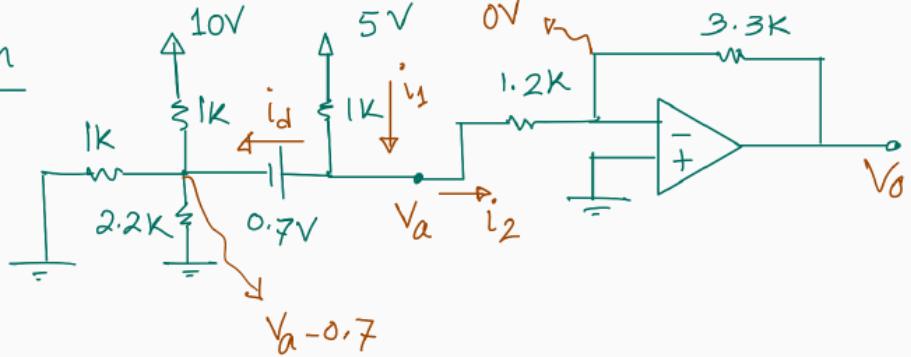


The saturation voltages of the Op-Amp are given as- $V_{sat}^+ = +10V$ and $V_{sat}^- = -10V$. The forward voltage drop of the diode, V_D is 0.7V.

- (a) **Determine** the operating mode diode, D_1 . Verify your assumption with necessary calculations.
- (b) **Calculate** the voltage at - (i) node 'Va', (ii) non-inverting terminal of the Op-Amp, (iii) inverting terminal of the Op-Amp.
- (c) Find out the output voltage, V_0 of the Op-Amp.

Soln:

Assume D₁ on

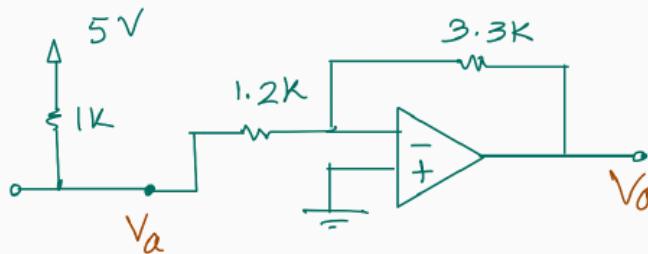


$$\text{Nodal: } (V_a - 0.7) \left(1 + 2.2 + 1 \right) + V_a (1 + 1.2) = 10 + 5 \\ \Rightarrow V_a = 3.898 \text{ V}$$

$$\therefore i_d = i_1 - i_2 = \frac{5 - V_a}{1} - \frac{V_a - 0}{1.2} = -2.15 \text{ mA} < 0 \text{ mA}$$

$\therefore D_1$ "cannot" be ON

$\therefore D_1$ is OFF \rightarrow Left side Open \rightarrow Equivalent ckt :

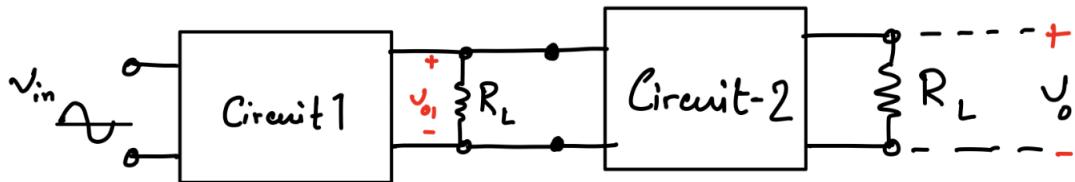


\Rightarrow This is an inverting amplifier with 5V and $(1k + 1.2k)$ at the inverting terminal

$$\therefore V_o = -\frac{3.3}{1+1.2} \times 5V = -6.82 \text{ V}$$

3.

You are provided with the diagram below as a starting point for designing an AC to DC converter. Input voltage source is a sinusoidal voltage source (V_{in}), with 2V peak to peak voltage (i.e. 1 V amplitude) and the DC voltage is around 10 V (with ripple) at the output terminals (v_o).

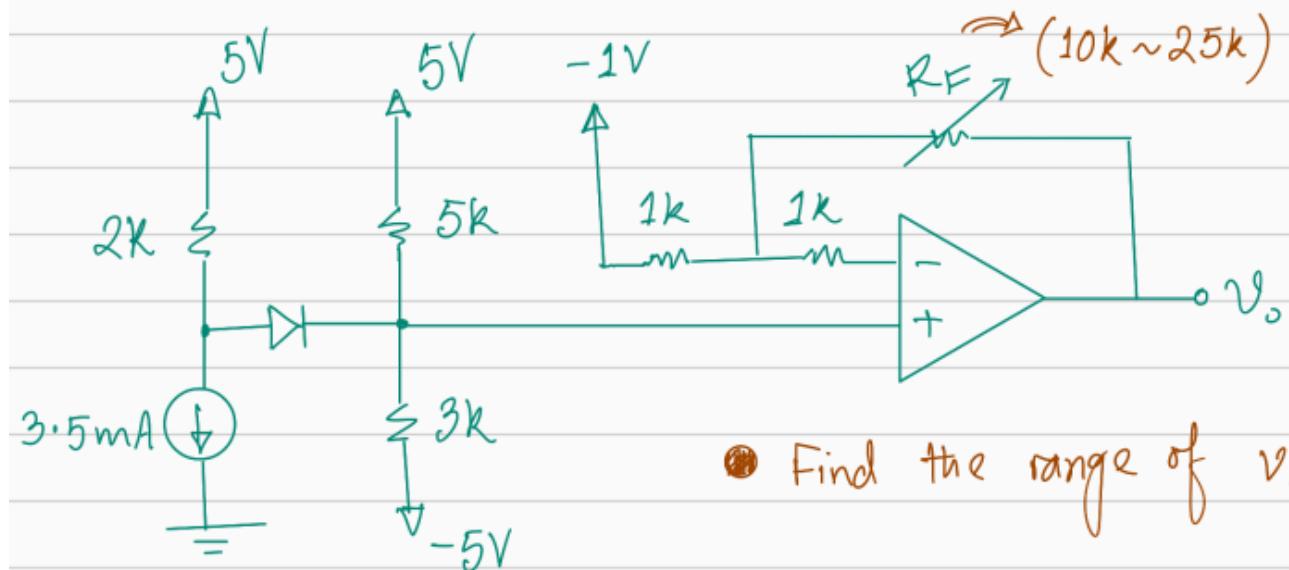


So, in order to solve this problem, you are provided with a single diode (with $V_{D0} = 0.7$ V), two resistors (R_1 and R_2 , excluding the load resistors R_L) and an UA741 op-amp.

- (a) Design **circuit-1** with the single diode and $R_L = 10 k\Omega$ (R_L is already provided in the diagram as output terminals of **circuit-1**) to get a rectified voltage and determine the DC value of the output voltage (v_{o1}) of the circuit. [1+2]
- (b) Determine the ripple voltage of v_{o1} . [Ripple voltage is defined as the difference between the maximum and minimum value of a DC voltage.] [2]
- (c) What should be the value of a capacitor used at the output end of **circuit-1** with R_L to reduce the ripple voltage of v_{o1} to 0.1 V. How should the capacitor be connected with R_L in the diagram? [4+1]
- (d) Design an amplifier using an operational amplifier as **circuit-2** to increase the DC voltage level of the output voltage of the circuit designed in (c) to 10 V. Find the ripple voltage of the amplified voltage signal. [4+1]

4.

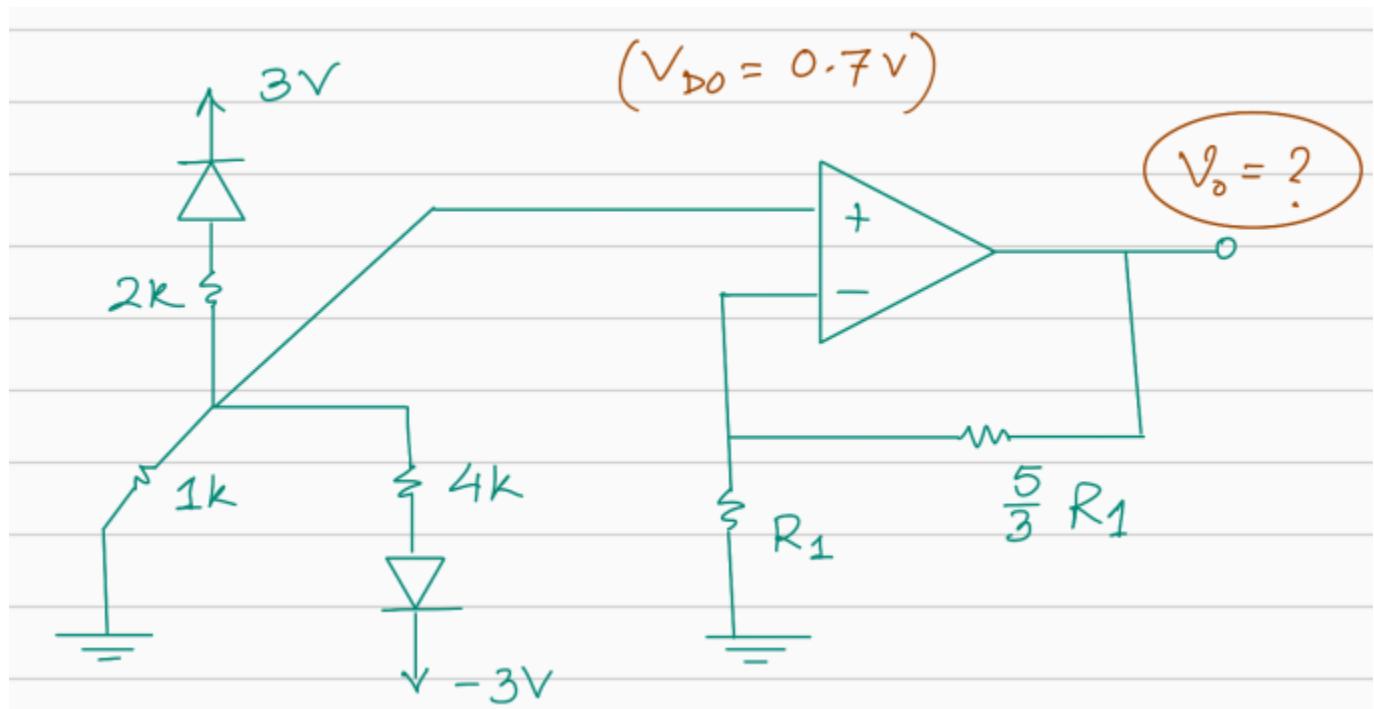
$$(V_{D0} = 0.7V)$$



• Find the range of V_o

5.

$$(V_{D0} = 0.7V)$$



Rectifiers

1. The input of a full-wave rectifier is a cosine voltage with peak $V_M = 5$ V and frequency 60 Hz, and output load resistance is $R = 2$ k Ω . Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.7$ V.

(a) Briefly explain the purpose of a rectifier and describe its operation. [1]

(b) Show the input and output waveforms. [2]

(c) Calculate the DC value of the output voltage. [1]

Now after connecting a capacitor in parallel with the load, the output becomes a ripple voltage $\mathbf{Vout} = V_{DC} \pm 0.2$ V

(d) Calculate the **peak-to-peak ripple voltage**, and from that, the value of the capacitor. [2]

(e) Calculate the average of the output voltage V_{DC} after connecting the capacitor. Compare this with the DC value determined in 'c' and comment on the difference between these two. [2]

2. The input of a **Half-wave rectifier** is a sine voltage with peak $VM = 10$ V and frequency 55 Hz, and output load resistance is $R = 2.5$ k Ω . Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.4$ V.

(a) Calculate the DC value of the output voltage. [1]

Now after connecting a capacitor in parallel with the load, the output becomes a ripple voltage $\mathbf{Vout} = V_{DC} \pm 0.3$ V.

(b) Calculate the **peak-to-peak ripple voltage**, and from that, the value of the capacitor. [2]

(c) Draw the **Voltage Transfer Characteristic (VTC) curve** [2]

3. The input of a full-wave rectifier is expressed by, $Vs(t) = 7\sin(400\pi t)$, and output load resistance is $R = 5$ k Ω . Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.3$ V.

(a) Calculate the input and output wave frequency. [2]

(b) Show the input and output waveforms.

Now after connecting a capacitor, $C = 100$ μ F in parallel with the load.

(c) Calculate the peak-to-peak ripple voltage,

(d) How can you provide better filtering for the output waves?

(e) What is the frequency of the Ripple voltage?

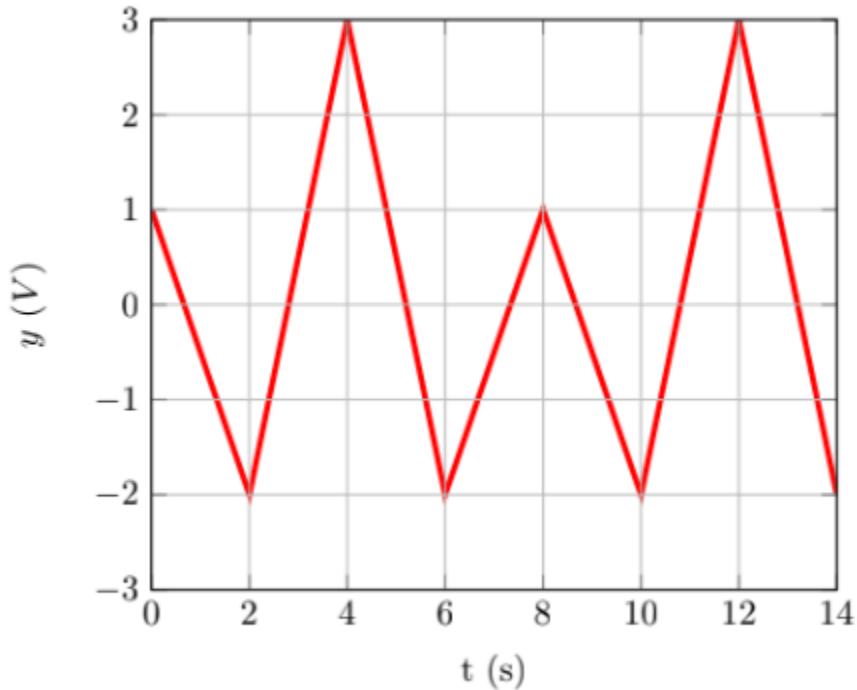
4. The input of a **Half-wave rectifier** is a **Square** wave voltage with peak $V_M = 15$ V and frequency 0.5 Hz, and output load resistance is $R = 5$ k Ω . Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.7$ V.

i. Show the input and output waveforms. [4]

ii. Draw the VTC curve [2]

5. The input of a **full-wave rectifier** is a **Square** wave voltage with peak $V_M = 15$ V and frequency 0.5 Hz, and output load resistance is $R = 5$ k Ω . Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.7$ V.

- Show the input and output waveforms. [4]
- Draw the VTC curve [2]



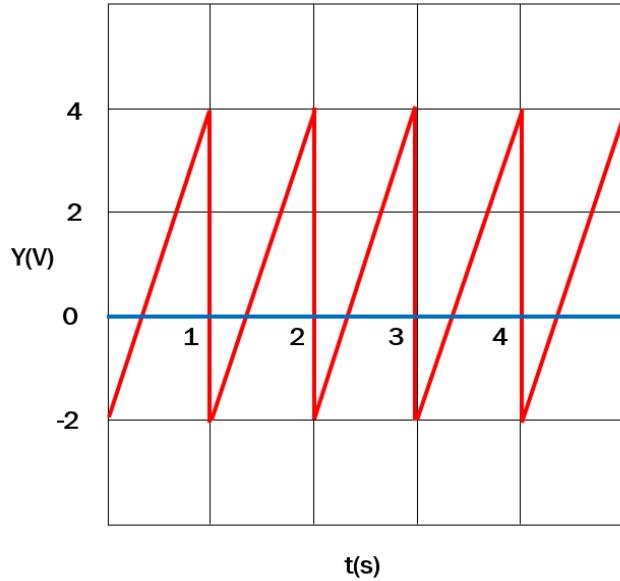
(b) Input of the FW rectifier

6.

Part 2: A voltage waveform $V_i = 15 \sin(2000\pi t)$ V is fed into a Half-wave rectifier with a load resistance $R = 5 \text{ k}\Omega$. Silicon diodes are used in this circuit for which the forward drop is $V_{D_0} = 0.7$ V.

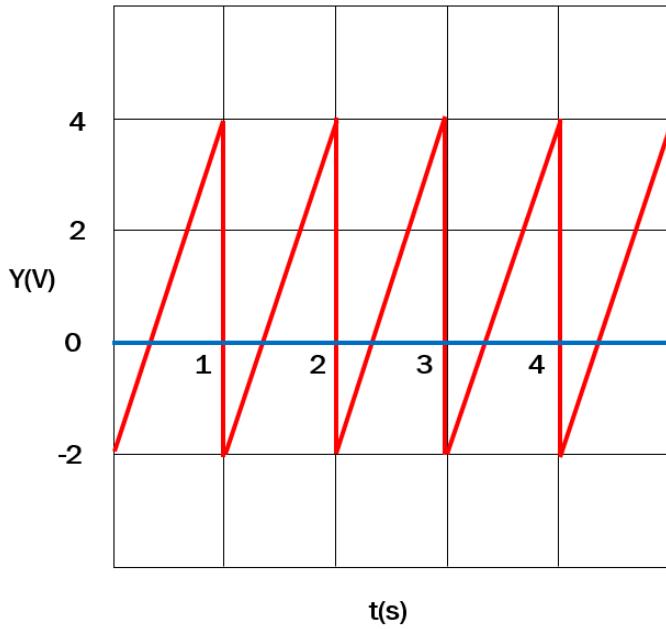
- Illustrate** the input and output waveforms in separate graphs. Label the graph and **indicate** the voltage levels properly. [2]
- Calculate** the DC/Average value of the output. [1]
- A capacitor is now added to reduce the fluctuation of the output voltage, which makes the peak to peak ripple voltage 4% of the maximum output voltage V_P . **Deduce** is the value of the capacitor from the given data. [2]
- The input of a Full-wave rectifier is shown in Figure 1(b) above and output load resistance is $R = 10 \text{ k}\Omega$. Germanium diodes are used in this circuit for which the forward drop is $V_{D_0} = 0.3$ V. **Show** the input and output waveforms [1]

7.

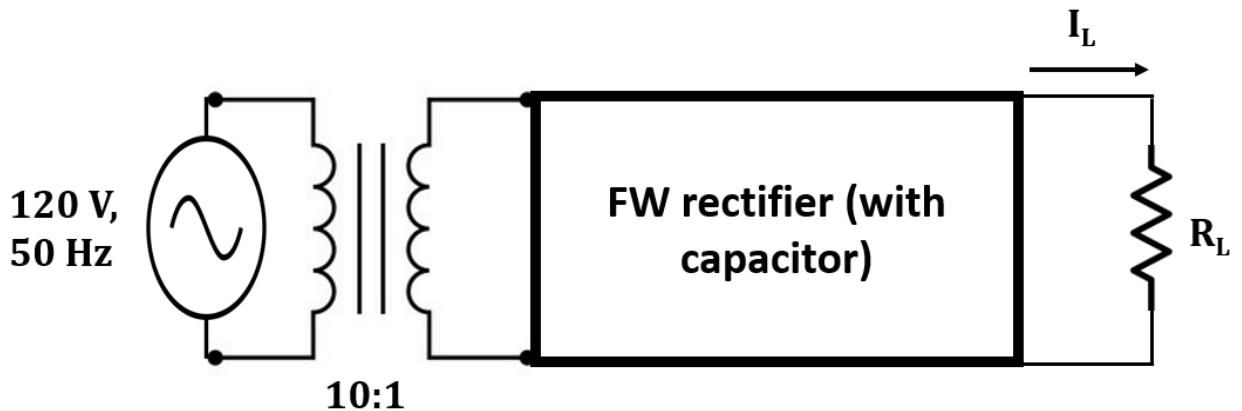


The input of a **Half-wave rectifier** is exhibited in the Figure above and output load resistance is $R = 5 \text{ k}\Omega$. Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.7 \text{ V}$.

- Show the input and output waveforms. [3]
- Draw the VTC curve [2]
- Calculate input and output frequency [3]



- The input of a **full-wave rectifier** is exhibited in the Figure above and output load resistance is $R = 5 \text{ k}\Omega$. Silicon diodes are used in this circuit for which the forward drop is $V_{D0} = 0.7 \text{ V}$.
 - Show the input and output waveforms. [3]
 - Draw the VTC curve [2]
 - Calculate input and output frequency [3]
- A full-wave rectifier is designed to deliver a maximum current $I_L = 120 \text{ mA}$ to the load. The rectifier produces an output with a ripple of 5% of the peak output voltage. An input line voltage of 120 V (peak), 50 Hz is available. A 10:1 step-down transformer is used to transform the supply voltage to 12 V (peak).



- (a) Draw the Voltage Transfer Characteristics of the full-wave rectifier. [2]
- (b) Calculate the peak output voltage. [1]
- (c) Determine the value of the Load Resistor to deliver a maximum load current of 120mA. [2]
- (d) Deduce the value of the Capacitor and the DC average value. [1]
- (e) Assume the transformer is removed and the rectifier is directly connected to the AC power supply line. Discuss the state of the diodes. [Hint: use the Peak Input Value of the rectifier input] [3]

Zener Diode

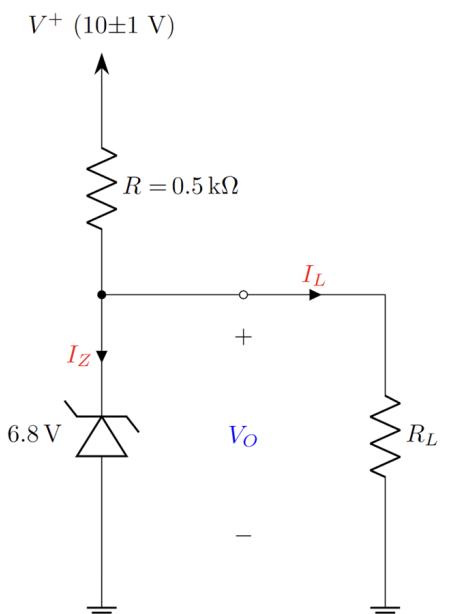
Q1

The 6.8-V Zener diode in the circuit of **Figure** is specified to have the following parameters. The supply voltage V^+ is nominally 10 V but can vary by ± 1 V.

- (a) Find V_o with no load and with V^+ at its nominal value
- (b) (For $R_L = 0.5 \text{ k}\Omega$). Find the I_z . In this scenario, calculate the Zener voltage V_o , load current I_L and input current I
- (c) Find the R_L that would give rise to worst-case scenario at worst case V^+ . In this worst-case scenario, calculate the Zener voltage V_o , load current I_L and input current I
- (d) (For $R_L = 2 \text{ k}\Omega$). Find the I_z . In this scenario, calculate the Zener voltage V_o , load current I_L and input current I
- (e) Design the circuit, i.e., find the minimum value of the input voltage V^+ such that, voltage regulation is maintained even in the worst-case scenario for $R_L = 2 \text{ k}\Omega$. (Forget that V^+ is 10 V)

$V^+ = 10 \pm 1 \text{ V}$

$V_z = 6.8 \text{ V at } I_z = 5 \text{ mA}$
$r_z = 20 \Omega$
$I_{ZK} = 0.2 \text{ mA}$



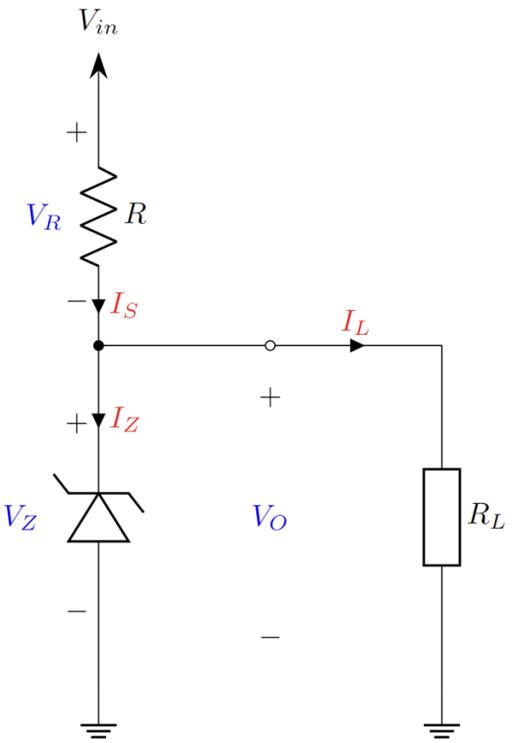
- (f) Determine whether the circuit will maintain regulation if V^+ is increased. If yes, argue if it should be increased or not.

Q2

The Zener diode in the circuit of Figure is specified to have the following parameters. The supply voltage V_{in} is nominally 5 V but can vary by $\pm 10\%$. Load current can vary from 0 mA to 50 mA.

$V_{in} = 5 \text{ V} \pm 10 \%$

$V_{z0} = 3 \text{ V}$
$r_z = 0 \Omega$
$I_{ZK} = 1 \text{ mA}$.



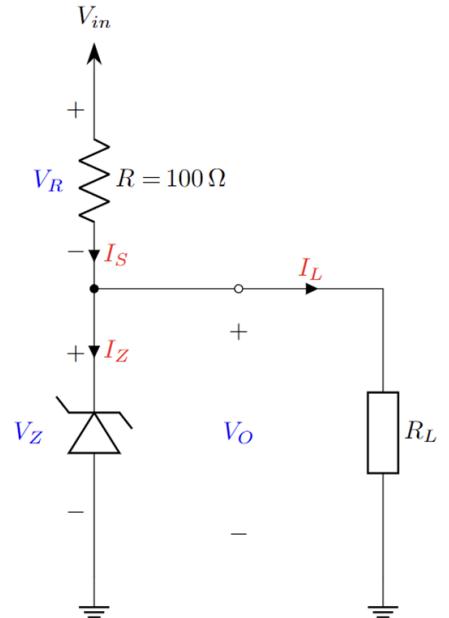
- a) Find minimum and maximum input Voltage, V_{in} (min) and V_{in} (max), maximum and minimum load current I_L (max) and I_L (min), minimum diode current I_Z (min).
- b) Find the I_Z , V_{in} and I_L at the worst-case scenario.
- c) For the worst case what is I_S and V_R .
- d) Find R for which diode maintains regulation at worst case scenario

Q3

The Zener diode in the circuit of Figure is specified to have the following parameters.

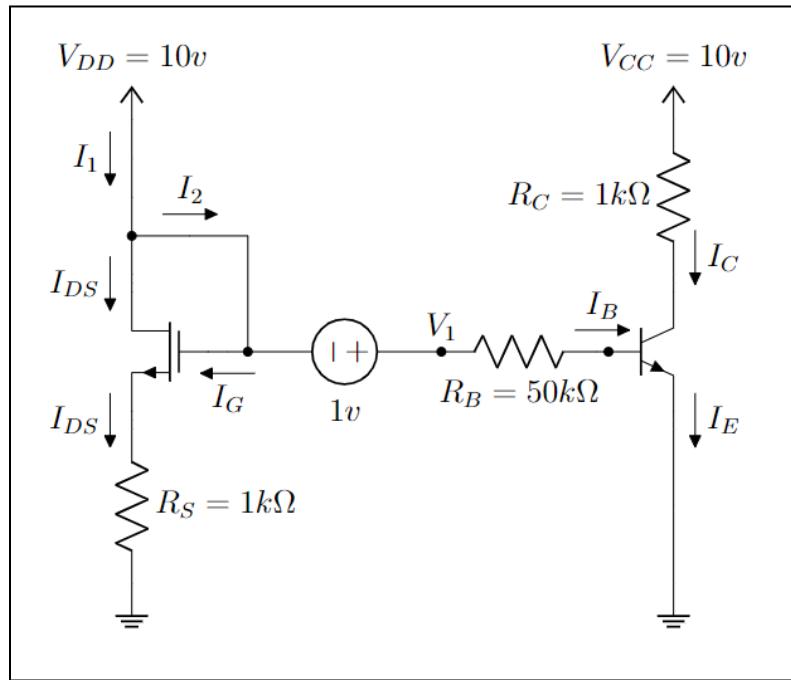
$V_{z0} = 3 \text{ V}$
$r_z = 20 \Omega, 0 \Omega$
$I_{ZK} = 1 \text{ mA}$.

- a. Find minimum input voltage, V_{in} (min) for which the diode maintains regulation, when $R_L=10 \text{ k}\Omega$.
- b. Find worst case R_L if the input voltage V_{in} is nominally 5 V but can vary by $\pm 10\%$



BJT

Q1

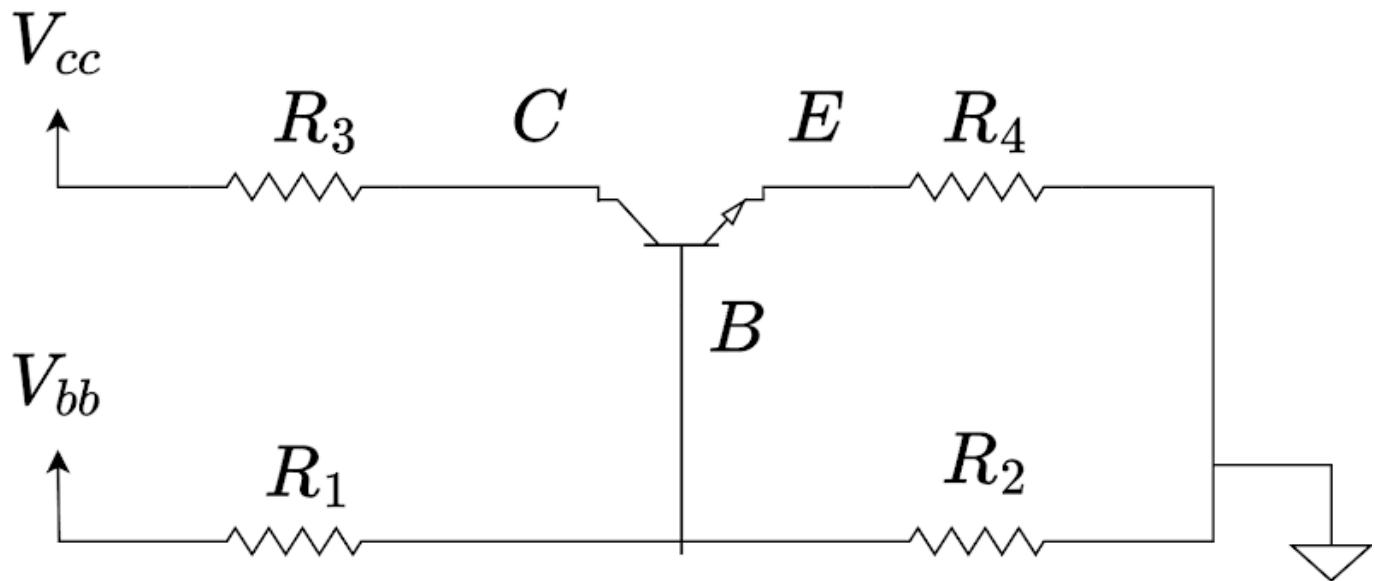


In the circuit above, the MOSFET and BJT have the following parameters,

$$K = 4 \text{ mA/V}^2, V_T = 0.9 \text{ v}, \beta = 100, V_{BE(\text{active})} = 0.7 \text{ v}, V_{BE(\text{sat})} = 0.8 \text{ v}$$

- (a) Find out the gate voltage of the MOSFET.
- (b) Calculate V_1 .
- (c) Find out the expression for V_{GS} , V_{DS} and V_{ov} .
- (d) Find the operating mode of the MOSFET using the expressions from ©. [Hint: You don't need any assumption]
- (e) Calculate I_{DS} and V_{DS} using the given parameters.
- (f) Assume that the BJT is in the saturation mode. Now, calculate I_B , I_C , I_E . You must validate the given assumption.

Q2



In the above circuit, $V_{bb} = 5V$, $V_{cc} = 15V$, $R_1 = 20k\Omega(40k\Omega)$, $R_2 = 80k\Omega(60k\Omega)$, $R_3 = 2k\Omega$ and $R_4 = 1k\Omega$. Also, assume current gain, $I_c/I_b = 100$.

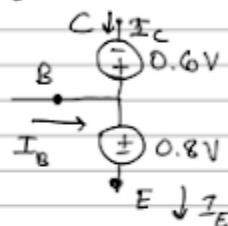
- a) Draw the equivalent circuit of BJT during saturation and active modes. [2]
- b) Solve the above circuit and calculate I_B , I_C , I_E , V_{CE} and V_C using the method of assumed states. [Hint: try to find the Thevenin equivalent of the left hand side circuit from the B terminal and ground] [3]
- c) If V_{bb} is changed from 5V to 5.1V, what happens to the outputs of the circuits? Calculate I_B , I_C , I_E , V_{CE} and V_C again. Now for a 0.1V increase in input V_{bb} , what is the change of I_c ? Use $\Delta I_C = I_{C,new} - I_{C,old}$. [3+1]
- d) Explain any use case of the differences in voltage increase between input and output. What could the use case be to such a phenomenon? [1]

Solution

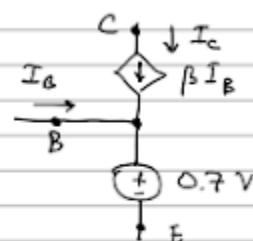
Set A



(a) BJT equiv. ckt: i) saturation

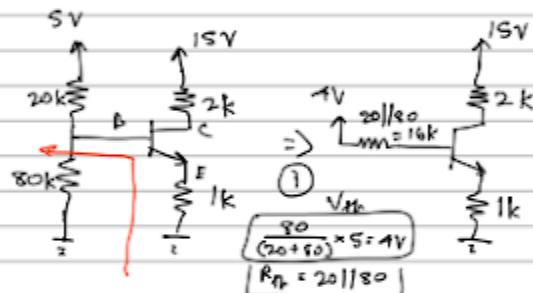


ii) active



(b) Redraw ckt for clarity:
(Assume saturation)

i) Applying theorem at
B node and ground



from KVL in base ckt:

$$I_B = \frac{1 - 0.7}{16 + (1 + \beta)} = 0.0282 \text{ mA}, \quad I_C = \beta I_B = 2.82 \text{ mA}$$

$$I_E = I_B + I_C = (1 + \beta) I_B = 2.8982 \text{ mA}, \quad V_E = 15 - I_C \times 2 = 9.36 \text{ V}$$

$$V_B = I_E \times 1 = 2.9982 \text{ V} \quad V_{CE} = V_C - V_E = 6.5118 \text{ V}$$

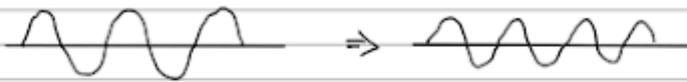
$\rightarrow V_{CE} > 0.2 \text{ V}$, $I_B, I_C, I_E > 0$: Assumption correct

(c) Same calc. as above but with $V_{BB} = 5.1 \text{ V}$

$$\begin{aligned} 1.02 \text{ V} & \quad I_B = \frac{1.02 - 0.7}{16 + 10 \times 1} = 0.0249 \text{ mA}, \quad I_C = 2.89 \text{ mA}, \quad I_E = 2.918 \text{ mA} \\ 10 \text{ k} & \quad V_C = 15 - I_C \times 2 = 9.22 \text{ V}, \quad V_E = 2.918 \text{ V}, \quad V_{CE} = V_C - V_E \\ 2 \text{ k} & \quad = 6.302 \text{ V} \\ 1 \text{ k} & \quad \Delta V_{BB} = 0.1 \text{ V}, \quad \Delta I_C = 2.89 - 2.82 = 0.07 \text{ mA} \end{aligned}$$

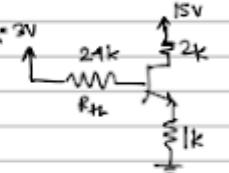
① Input change of 0.1 V \rightarrow output change of 0.07 mA

[Any signal can be attenuated, can be used as attenuator
to reduce the swings of a signal]

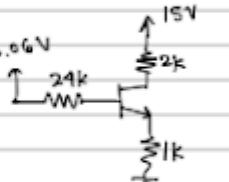


Set B

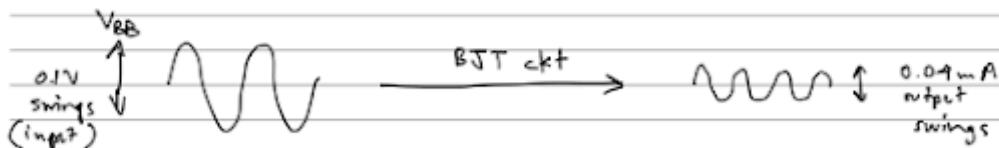
Same as set-A, R_f , R_L values changed

(b)  $I_b = \frac{3 - 0.7}{2k + 1k} = 0.0184 \text{ mA}, I_c = 1.84 \text{ mA}$ $I_E = 1.8584 \text{ mA}, V_{CE} = (15 - 2I_c) - 1 \times I_E = 9.9616 \text{ V}$

$V_C = 15 - 2I_c = 11.32 \text{ V}, V_E = 1.8584 \text{ V}$

(c)  $I_b = 0.0188 \text{ mA}, I_c = 1.88 \mu\text{A}, I_E = 1.907 \mu\text{A}$ $V_C = 15 - 2I_c = 11.24 \text{ V}, V_E = 1.907 \text{ V}$ $V_{CE} = 9.333 \text{ V}$

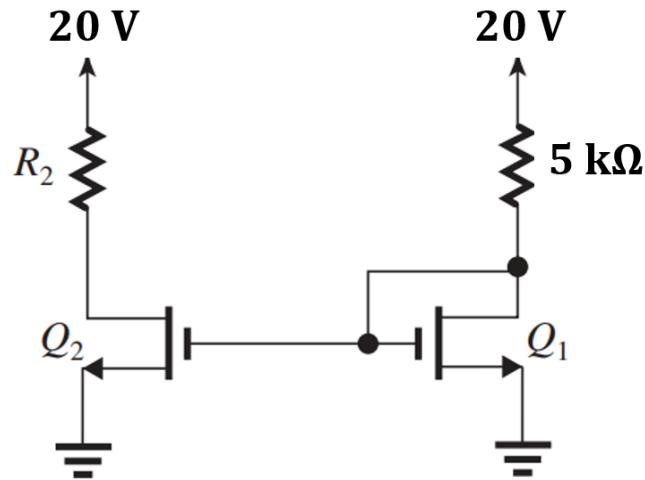
$\Delta V_{BB} = 0.1 \text{ V}, \Delta I_c = 1.88 - 1.81 = 0.07 \text{ mA}$



* Acts as a kind of signal swing attenuator.

MOSFET

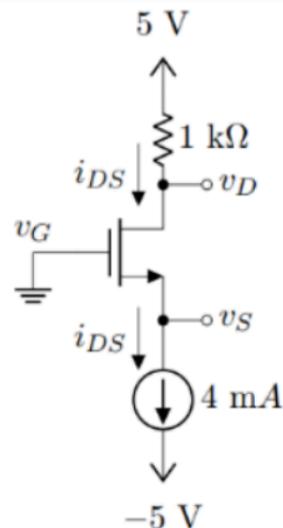
Q1.



In the circuit above, the MOSFETs have the following parameters, $k'n=2 \text{ mA/V}^2$, $W/L= 2.5$, $V_T=0.5 \text{ V}$.

- Find out** the operating mode of Q1 [Hint: For Triode mode $V_{ds}<V_{ov}$ and for Saturation $V_{ds}\geq V_{ov}$]
- Determine** the value of R_2 that results in Q2 operating at the edge of the saturation region.
- Calculate the on-state resistance**, R_{on} for Q2. Assume, gate voltage of Q2 is 20 V.
- An inverter is designed using Q2 and a 10K resistor. **Draw** the VTC graph for the inverter.

Q2.



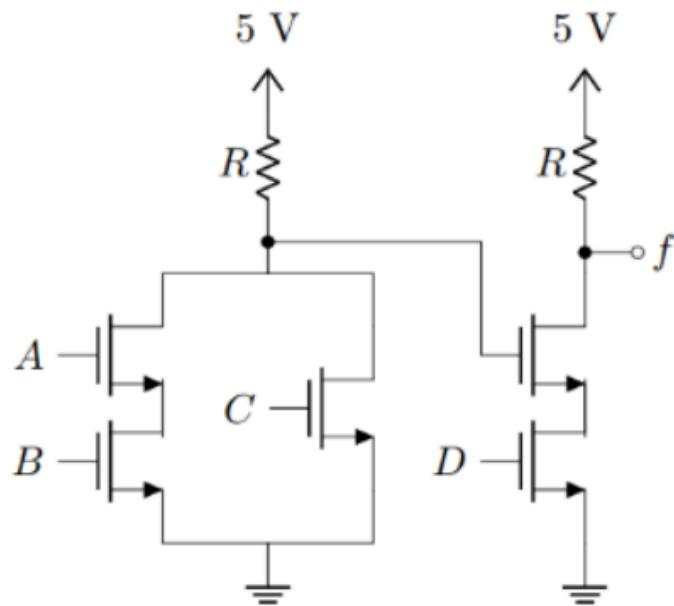
Circuit 1

Refer to the **Circuit** above. For the MOSFET, $V_T = 1$ V and $k = k'_n \frac{W}{L} = 4$ mA/V².

- Identify** the value of the gate voltage v_G and the drain-source current i_{DS} .
- Calculate** the value of the drain voltage v_D using the 1 kΩ resistor.
- Analyze** the circuit to find v_S . Here, **use** the Method of Assumed State. You must **validate** your assumptions. [Hint: assume $v_S = x$]

Q3

For the following circuit, find f in terms of boolean input **A**, **B**, **C**, **D**.



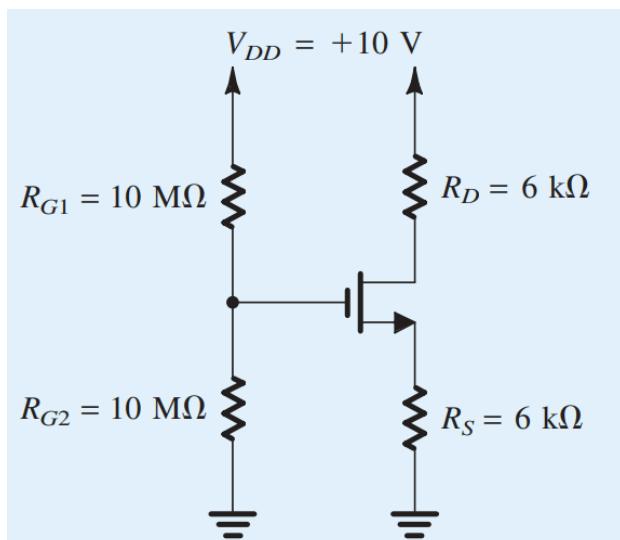
Q4

Use MOSFET to implement the Boolean Logic function, $F = \underline{AB} + \underline{C}$

Q5

I. Draw the VTC of a NOR gate using MOSFET S-model. ii. Draw the VTC of a NOR gate using MOSFET SR-model. Let, $R_{on} = 100$ ohms, $R_L = 10$ Kohms, $V_{ss} = 5$ V.

Q6



Analyze the circuit to find i_D and v_D using Method of Assumed State. You must validate your assumptions.

Here, $V_T = 1V$, $k = 5 \text{ mA}/\text{V}^2$

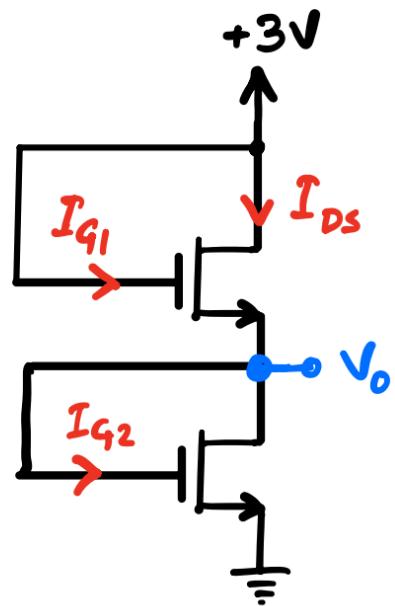
Q7

- (a) $f = (A + B)C$
- (b) $f = (\overline{AB} + CD)$
- (c) $f = AB + A + CD$ (with and without simplifying the logic)

Q8

In the circuit shown in the figure below, the transistor is characterized by $V_T = 1 V$, $k = 1 \text{ mA}/\text{V}^2$. (Hint: Identify the modes of the two MOSFET, and equate the two currents.)

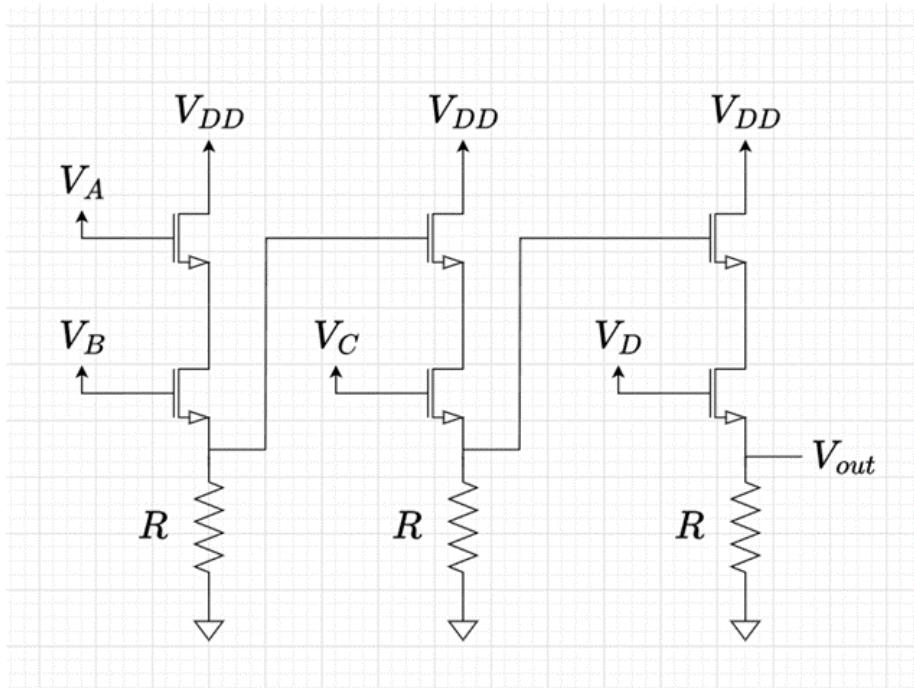
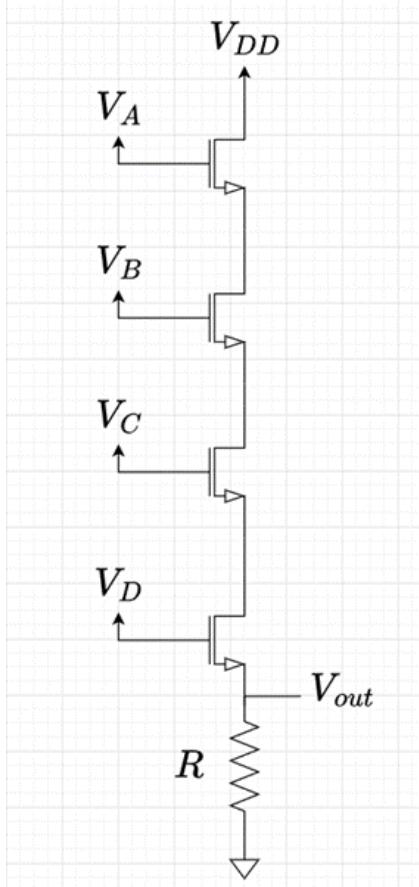
- (a) [3 marks] Find the value of V_O indicated in the figure.
- (b) [3 marks] Find the values of I_{DS} , I_{G1} and I_{G2} .



Q9 (1st ckt has too many equations and variables to solve by hand, 2nd ckt can be solved, each mosfet ckt should give you 2 equations in 2 variables with appropriate substitutions, try to solve 2nd ckt to get some practice solving with SR models)

Another hint: SR model is simply the approximate of the MOSFET equation, $I_d = k(V_{ov} \cdot V_{ds} - V_{ds}^2/2)$ with V_{ds}^2 negligible, thus giving us, $I_d = k \cdot V_{ov} \cdot V_{ds}$. This should be clear since voltage

by current is resistance, and here, $V_{ds} / Id = 1 / (k * V_{ov}) = R_{on}$ as we learned. So, SR model is a simpler model of MOSFET equation in triode region!



Circuit-1

Circuit-2

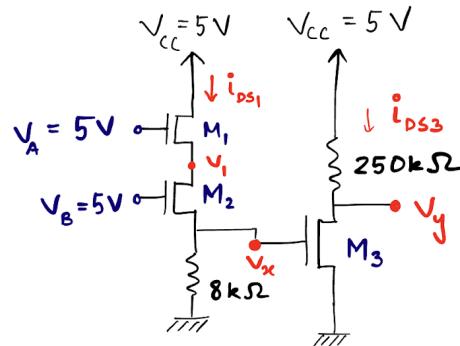
The above 2 circuits are implemented for logic gates using n-MOSFETs. All input voltages, V_{DD} , V_A , V_B , V_C and V_D are 5V. Given, each n-MOSFET has the following parameters for

its SR model: $V_T = 1V$, $k = 2.5 \times 10^{-4} A/V^2$ (be wary of units!) and $R_{on} = 1/(kV_{OV} \Omega)$. Also given, $V_{OV} = V_{GS} - VT$ (For this problem, approximate V_{GS} to be equal to V_G)

- Write down the SR model of an n-MOSFET. [1]
- Find the logic expressions for circuit-1 and circuit-2. [2]
- Using the SR-model of MOSFET, solve circuit-1 and circuit-2 and find the output voltage, V_{out} when all inputs, V_A , V_B , V_C and V_D are high(+5V). Given, $R = 800 \Omega$. Do the two circuits give the correct output as per their logic expressions? [3]
- If the outputs of the two circuits are used as gate voltage to a similar n-MOSFET, will it work as intended? That is, will a logical high in output be seen as logical high in the input of any n-MOSFET? If not, what can you do to remedy this. Explain with necessary calculations. [4]

Q10

MOSFET Design



For the following circuit with MOSFETs, assume that $V_T = 1 V$, $k_n = 50 \mu A/V^2$ and the aspect ratio W/L is 1 for all the MOSFETS.

- If the gate voltage to M3 MOSFET, $V_x = 0.938$ V, and MOSFET M2 is in triode mode, find the voltage V_1 . [3]
- Find V_y . [2]
- If $W/L=2$, then $V_1 = 2.1454$ V. Find V_x for this case. [2]
- Can you explain, whether there will be any changes in the output voltage at V_y for $W/L = 2$ from that in ('b'). Also, comment on whether a larger or smaller value of W/L ratio is preferred in this case. [2+1]

Solution:

$$\textcircled{a} \quad i_{DS1} = \frac{v_x}{8} = \frac{0.05}{2} (5 - v_t - 1)^2$$

$$v_t = 4 \pm \sqrt{\frac{0.938}{8} \times \frac{2}{0.05}}$$

$$= 1.835V$$

$$\left[\begin{array}{l} \text{Verify: } M_1: v_{G1} = v_A = 5V \\ \quad v_{D1} = v_{ce} = 5V \\ \quad \therefore v_{D1} > v_{G1} - v_t \rightarrow \text{Sat} \end{array} \right]$$

$$M_2: v_{G2} = 5 \\ v_{DS2} = 1.835V < v_{G2} \rightarrow \text{Triode}$$

$$\textcircled{b} \quad v_x < v_t : v_y = 5V$$

$$\textcircled{c} \quad \frac{w}{L} = 2 :$$

$$i_{DS1} = \frac{v_x}{8} = \frac{0.05}{2} \left(\frac{w}{L} \right) (5 - 2.145 - 1)^2$$

$$\Rightarrow v_x = 1.377V$$

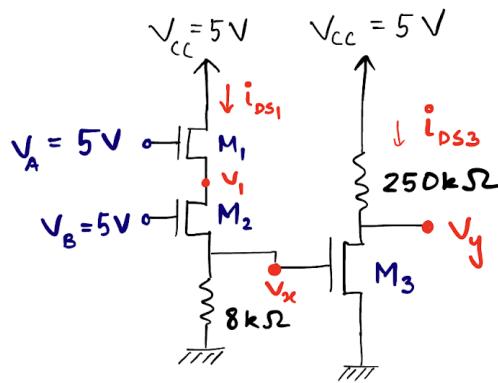
d. Assuming saturation:

$$\left. \begin{array}{l} v_{G1S} = 1.377 \\ v_{DS} = 0.377 \end{array} \right\} v_y = ?$$

$$i_{DS} = (0.377)^2 \times \frac{0.1}{2} = 7.1 \mu A$$

$$\therefore v_y = 5 - i_{DS} \cdot 250 = 3.223 > v_{ov}$$

↳ Sat. verified.



For the following circuit with MOSFETs, assume that $V_t = 1 \text{ V}$, $k_n = 20 \mu \text{A/V}^2$ and the aspect ratio W/L is 1 for all the MOSFETs.

(a) If the gate voltage to M3 MOSFET, $V_x = 0.492 \text{ V}$, and MOSFET M2 is in triode mode,

find the voltage V_1 . Verify the modes for both M1 and M2 [3]

(b) Find V_y . [2]

(c) If W/L=4, then $V_1 = 2.04 \text{ V}$. Find V_x for this case. [2]

(d) Can you explain, whether there will be any changes in the output voltage at V_y for W/L = 4 from that in 'b'. Also, comment on whether a larger or smaller value of W/L ratio is preferred in this case. [2+1]

Solution

$$\textcircled{a.} \quad i_{DS1} = \frac{V_x}{8} = \frac{0.02}{2} (5 - V_1 - 1)^2$$

$$V_1 = 4 \pm \sqrt{\frac{0.492}{8} \times \frac{2}{0.02}}$$

$$= 1.52 \text{ V}$$

$$\left[\begin{array}{l} \text{Verify: } M_1 : V_{G1} = V_A = 5 \text{ V} \\ \quad V_{D1} = V_{cc} = 5 \text{ V} \\ \quad \therefore V_{D1} > V_{G1} - V_t \rightarrow \text{Sat} \end{array} \right. .$$

$$\left. \begin{array}{l} M_2 : V_{G2} = 5 \\ \quad V_{DS2} = 1.52 \text{ V} < V_{G2} \rightarrow \text{Triode} \end{array} \right]$$

⑥ $v_x < v_T$: $v_y = 5V$

⑦ $\frac{w}{L} = 4$:

$$i_{DS1} = \frac{v_x}{8} = \frac{0.02}{2} \left(\frac{w}{L}\right) (5 - 2.04 - 1)$$

$$\Rightarrow v_x = 1.229312 V$$

⑧ Assuming saturation:

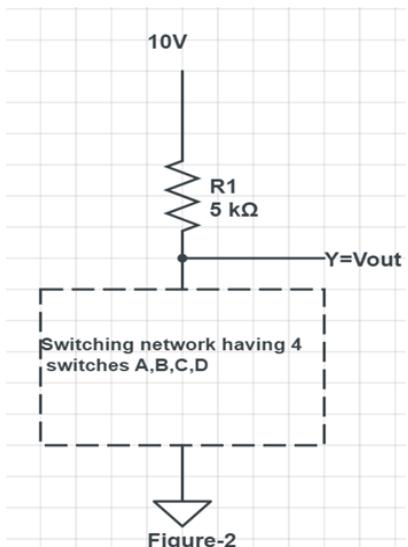
$$\begin{aligned} v_{GS} &= 1.229312 \\ v_{ov} &= 0.22913 \end{aligned} \quad \left| \begin{array}{l} v_y = ? \\ \end{array} \right.$$

$$i_{DS} = (0.22913)^2 \times \frac{0.08}{2} = 2 \mu A$$

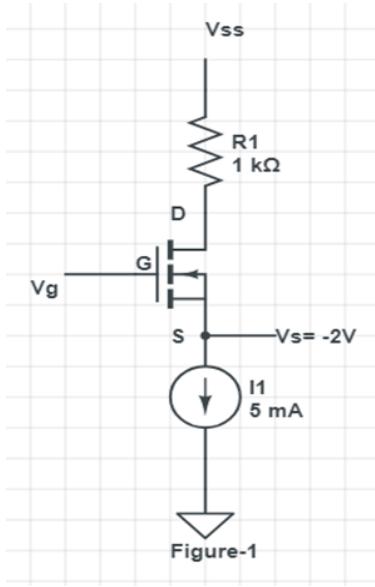
$$\therefore v_y = 5 - i_{DS} \cdot 250 = 4.475 V > v_{ov}$$

\hookrightarrow Sat. verified.

Q11



Conditions for Network on
 i) switch A must be on
 ii) Switches B,C simultaneously on or D on



- a) For figure-2, place the switches as nmos devices and write the output logic function Y in terms of A,B,C,D assuming nmos switch model. [2]
- b) From figure-2, assuming SR model for nmos find the output voltage when only A and D switches are ON(Assume $R_{on} = 0.1 \text{ k}\Omega$) [3]
- c) For figure-1, $k=2 \text{ mA/V}^2$, $V_T = 1 \text{ V}$ [3+2]
- i) Find the gate voltage so that the mosfet is in saturation mode.
 - ii) Then find the minimum supply voltage V_{ss} to operate the device in this condition. [Hints , $V_{ov}=V_{DS}$]
- d) **Bonus** - from figure-2 is it possible to drive a not gate cascaded to V_{out} ?
 $[V_T = 0.5 \text{ V}, V_{out}(\text{low}) = V_{out} \text{ of question(b)}]$ [2]

Solution

Q1 Set A

$$I_{DS} = \frac{1}{2} k V_{DS}^2$$

$$\Rightarrow 5 = \frac{1}{2} \times 2 \times V_{DS}^2$$

$$\Rightarrow V_{DS} = \sqrt{5}$$

$$\therefore V_{GS} - V_T = \sqrt{5}$$

$$\Rightarrow V_{GS} = \sqrt{5} + V_T = \sqrt{5} + 1 = 3.29$$

$$\therefore V_G - V_S = 3.29$$

$$\Rightarrow V_G = 3.29 + V_S = 3.29 - 2 \\ = 1.29 V$$

2nd part minimum V_{GS}

$$\begin{aligned} \Rightarrow V_{SS} &= 5 \times 1 + V_{DS} + V_S \\ &= 5 + \sqrt{5} - 2 \\ &\approx 5.29 V \end{aligned} \quad \left| \begin{array}{l} V_{DS} = V_{DS} = \sqrt{5} \\ V_{GS} = V_{GS} = \sqrt{5} \end{array} \right.$$

b) $Y = \overline{A(Bc+D)}$

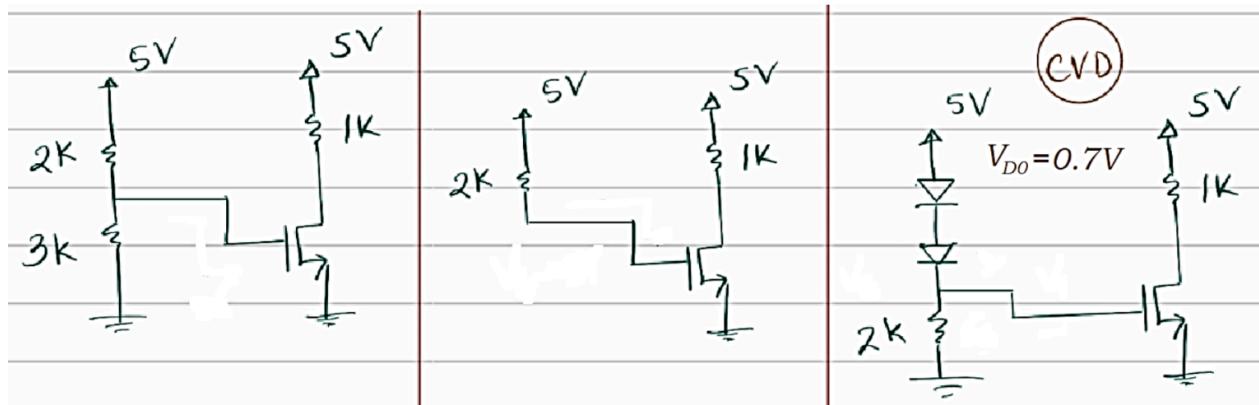
c)

$$V_{out} = 10 \times \frac{0.2}{5+0.2} = 0.385 V$$

d) $V_{out} < V_T$, so possible to turn off

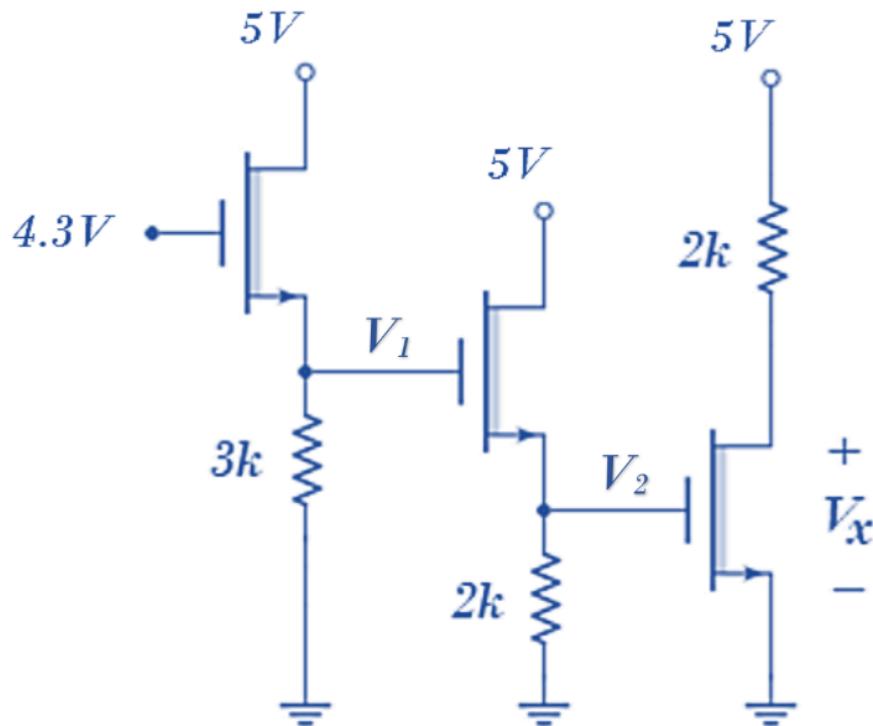
Q12 (MOSFET+Diode)

For all three circuits below, you are given $V_T = 1V, K_n = 1 \text{ mA/V}^2$. Determine which one of the three $1k\Omega$ dissipates the most power?

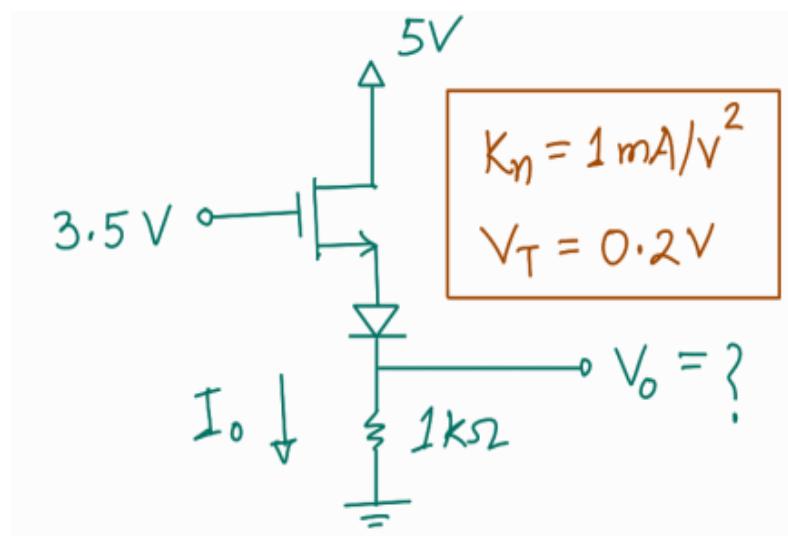


Q13

Using $V_T = 1V, K_n = 2 \text{ mA/V}^2$, determine V_x for the circuit below.



Q14 (MOSFET+Diode)



Solⁿ

$$V_{GS} = 3.5 - V_s, \quad V_{DS} = 5 - V_s$$

$$\text{Diode } \rightarrow \text{CVD} \rightarrow V_s - V_o = 0.7 \\ \Rightarrow V_s = 0.7 + V_o$$

$$\therefore V_{GS} = 3.5 - 0.7 - V_o = 2.8 - V_o$$

$$\&, V_{DS} = 5 - 0.7 - V_o = 4.3 - V_o$$

$$\text{Finally, } V_{ov} = V_{GS} - V_T = 2.6 - V_o$$

* Assume Saturation: $I_o = \frac{K_n}{2} V_{ov}^2$

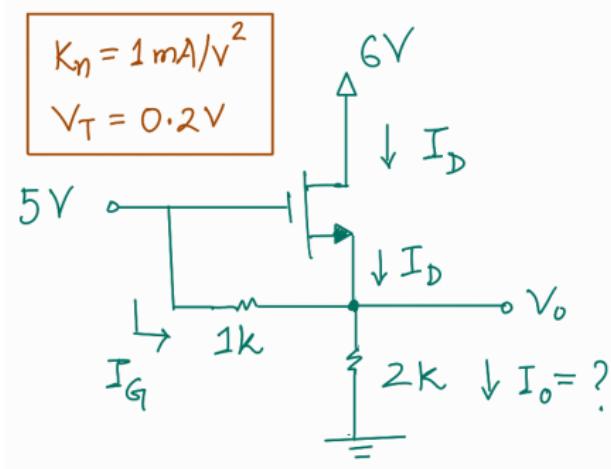
$$\Rightarrow \frac{V_o - 0}{1} = \frac{1}{2} (2.6 - V_o)^2$$

$$\Rightarrow V_o = 1.11, \quad \cancel{6.49}$$

* Verify: $\left. \begin{array}{l} V_{GS} = 2.8 - 1.11 = 1.69 > V_T \\ V_{DS} = 4.3 - 1.11 = 3.19 \\ V_{ov} = 2.6 - 1.11 = 1.49 \\ \text{Therefore, } V_{DS} > V_{ov} \end{array} \right\} \text{Assumption Correct}$

Ans:
 $V_o = 1.11V$

Q15



$$V_{GS} = 5 - V_o$$

$$V_{DS} = 6 - V_o$$

$$V_{ov} = V_{GS} - V_T = 4.8 - V_o$$

KCL gives us:

$$I_o = I_D + I_G$$

$$\Rightarrow \frac{V_o}{2} = I_D + \frac{5 - V_o}{1}$$

$$\Rightarrow I_D = \frac{V_o}{2} - (5 - V_o) \Rightarrow I_D = \frac{3V_o}{2} - 5 \dots (i)$$

Assume Saturation

for the MOSFET: This assumption affects only the current going through the MOSFET, I_D

$$\therefore I_D = \frac{K_n}{2} V_{ov}^2$$

$$\Rightarrow I_D = \frac{1}{2} (4.8 - V_o)^2 \dots (ii)$$

Equating (i) & (ii): $\frac{1}{2} (4.8 - V_o)^2 = \frac{3V_o}{2} - 5$

$$\Rightarrow V_o = 3.89, \cancel{7.21}$$

Verify: $V_{GS} = 5 - 3.89 = 1.11$

$V_{DS} = 6 - 3.89 = 2.11$

$V_{ov} = 4.8 - 3.89 = 0.91$

$\therefore V_{DS} > V_{ov}$

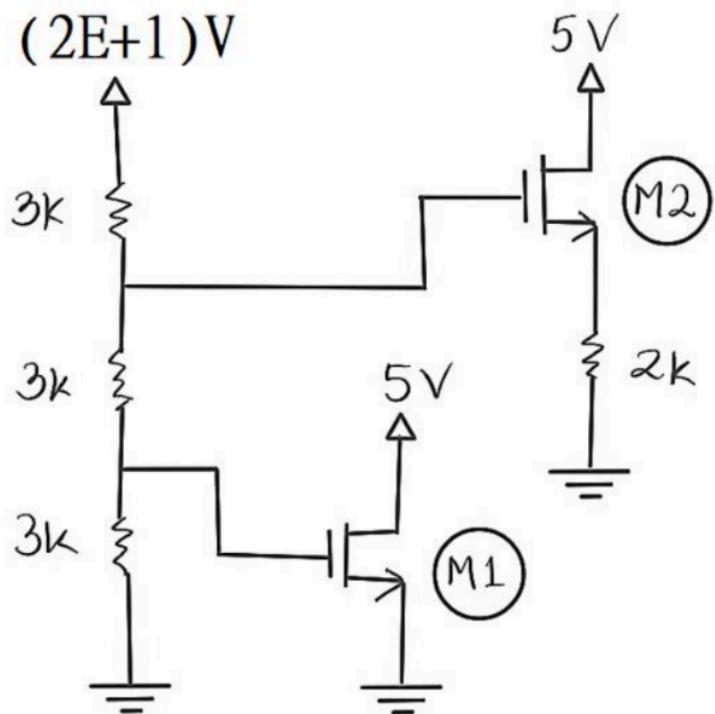
$\left. \begin{array}{l} \\ \\ \\ \end{array} \right\} \text{Assumption Correct}$

Ans:

$$I_o = \frac{V_o}{2} = 1.945 \text{ mA}$$

Q16

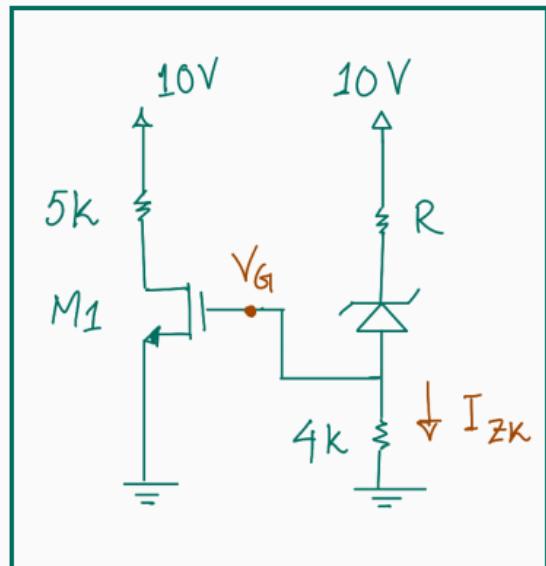
You are given (i) $E=2$, or, (ii) $E=5$. Determine the operation modes of the $M1$ and $M2$ MOSFETs. Also, find the power dissipated in the $2k\Omega$ resistor.



For both mosfets,
 $V_T = 0.3 V$
 $k_n = 0.1 mA/V^2$

Hybrid

Q1 [MOSFET, Zener]



Given, $r_z = 100\Omega$, $I_{ZK} = 1.2 \text{ mA}$
 $V_{ZD} = 3.3 \text{ V}$

(Q1) : Find the maximum value of R so that the zener diode stays in knee-voltage condition

(Q2) : Find the operating region of the Mosfet M_1 using the value of R in (Q1).

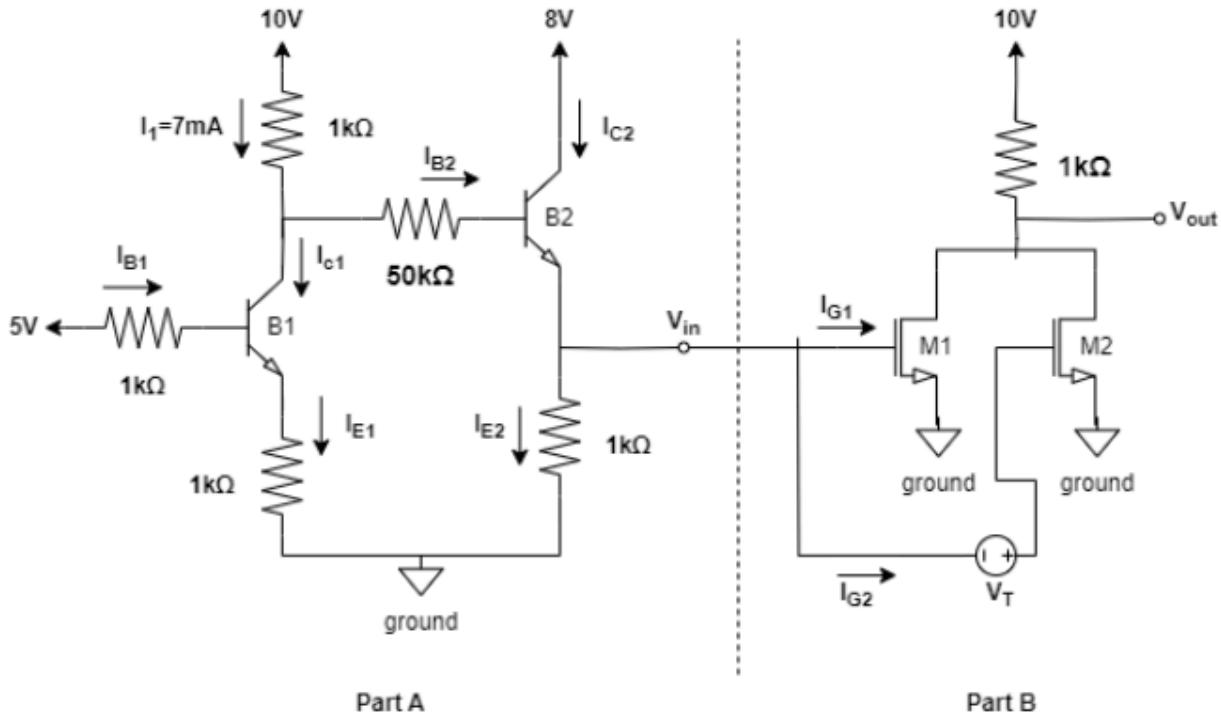
$$K_n = 1 \text{ mA/V}^2$$

$$V_T = 0.2 \text{ V}$$

Hint : (Q1) At worst case scenario, KVL gives us : ($R = R_{\max}$)
 $\Rightarrow 10 = I_{ZK} \cdot R + (I_{ZK} r_z + V_{ZD}) + 4 I_{ZK} \rightarrow R_{\max} = 1.48 \text{ k}\Omega$

$$(Q2) \quad V_G = 10 - R \times I_{ZK} - V_z \\ \Rightarrow V_G = 10 - R \times I_{ZK} - (V_{ZD} + I_{ZK} r_z) \quad \left. \begin{array}{l} \\ \\ \end{array} \right\} \text{Then use "Method of Assumed States"} \\ \text{So, } I_G = 0 \text{ mA } (***)$$

Q2 [MOSFET,BJT]



In the circuit above, the BJTs have the following specification: $\beta=100$, Forward Active Region: $V_{BE} = 0.7 V$, $I_c = \beta I_{B'}$ Saturation Region: $V_{BE} = 0.8 V$, $V_{CE} = 0.2 V$, or the MOSFETs: $V_T = \text{Threshold Voltage of } M1 \text{ and } M2$.

- Determine i_{g1} and i_{g2}
- Justify why the SR model of MOSFET is more efficient than the S model ? [1]
- Assume, B1 and B2 are in the Saturation region. Calculate i_{c2} .
- Assume, B1 is in the Forward Active region. Calculate V_{in} .
- Draw the VTC of Part- B assuming, $V_T = 8 V$. [Use S model of MOSFETs]

Solution

(a) $i_{G_1} = i_{G_2} = 0$

(b) SR Model considers channel resistance.

(c) From B₁

$5 - 0 = I_{B1} + 0.8 + I_{E1}$

$I_{B1} + I_{E1} = 4.2$

$10 - 0 = 2 + 0.2 + I_{E1}$

$I_{E1} = 2.8$

$\therefore I_{B1} = 4.2 - 2.8 = 1.4 \text{ mA}$

$\therefore I_{C1} = 2.8 - 1.4 = 1.4 \text{ mA}$

$\therefore I_{B2} = I_1 - I_{C1} = 2.8 - 1.4 = 1.4 \text{ mA}$

From B₂

$8 - 0 = 0.2 + I_{E2}$

$\therefore I_{E2} = 7.8 \text{ mA}$

$\therefore I_{C2} = I_{E2} - I_{B2} = 7.8 - 1.4 = 6.4 \text{ mA}$

$I_{C2} = 6.4 \text{ mA}$

(d) B₁ in Forward Active.

$\therefore 5 - 0 = I_{B1} + 0.8 + I_{E1}$

$I_{E1} = 4.3 - I_{B1}$

$$I_{E1} = \beta I_{B1} = 100 I_{B1}$$

$$I_{E1} = I_{B1} + I_{C1}$$

$$\Rightarrow 4.3 - I_{B1} = I_{B1} + 100 I_{B1}$$

$$\therefore I_{B1} = 0.042156 \text{ mA}$$

$$\therefore I_{C1} = 100 I_{B1} = 4.2156 \text{ mA}$$

$$I_{B2} = I_1 - I_{C1} = 7 - 4.2156 = 2.78432 \text{ mA}$$

For B_2

Assumption \Rightarrow saturation

$$6 - 0 = 0.2 + I_{E2}$$

$$\therefore I_{E2} = 7.8 \text{ mA}$$

$$\therefore I_{C2} = I_{E2} - I_{B2} = 7.8 - 2.78432 \\ = 5.0156 \text{ mA}$$

Verification

$$\frac{I_{C2}}{I_{B2}} = \frac{5.0156}{2.78432} = 1.8021 < \beta = 100$$

[correct]

$$\therefore 6 - V_{in} = 0.2$$

$$\therefore \boxed{V_{in} = 7.8 \text{ V}}$$

①

V_{out}

