BRAC University
Dept. of Computer Science and Engineering

Assessment: Assignment 4
Due: 11:59 PM 26 September, 2024
Full Marks: **40**

Semester: Summer 2024
Course Code: CSE251
Course Name: Electronic Devices and Circuits

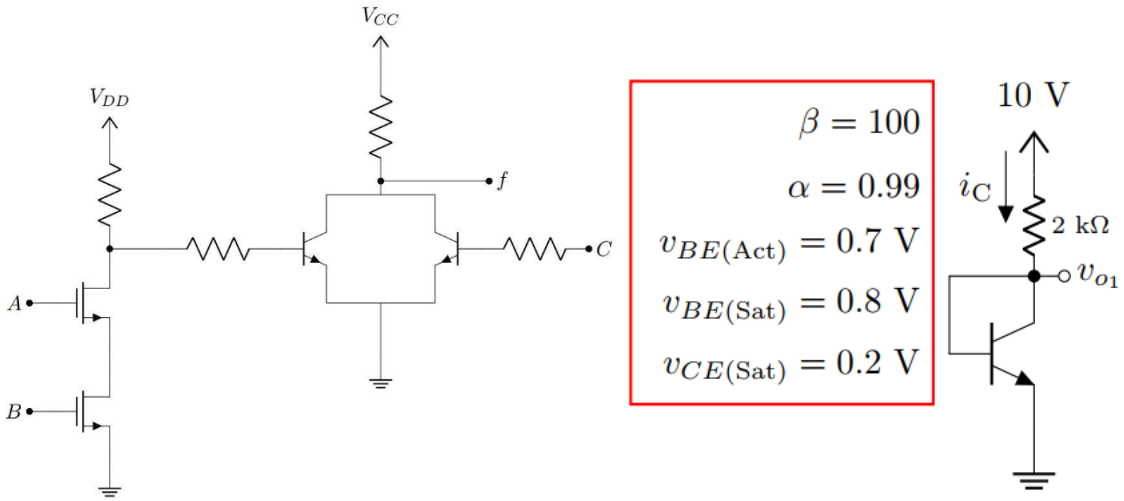
Name: _____

Student ID: _____

- ✓ Write down your student ID on the **top right corner of each of the pages**.
- ✓ Clearly write the solutions, along with the questions, on white paper with black ink (no need to use color pen, don't use pencils).
- ✓ Use **CamScanner**, or **Adobe Scan**, or **Microsoft Office Lens**, or any other software to scan the pages and make a **single PDF file**.
- ✓ After creating the PDF, make sure that **(a)** there are no pages missing, **(b)** all of the pages are legible, **(c)** your student ID on each page are visible.
- ✓ Please note, collaboration ≠ copying. You are allowed to discuss the questions and clear confusion you might have, but you have to write your solutions independently and be able to explain your answers during a random viva.
- ✓ **[Very Important]** Rename the PDF in the following format: **"A3_Section_StudentID_FullNameWithoutSpace.pdf"**. For example, if my student ID is 12345678 and my name is Shadman Shahid, the filename should be **"A3__S15_12345678_ShadmanShahid.pdf"**.
  - ✓ **Submission Link: https://forms.gle/wy8grQu7d4keTKKw9**

- For MOSFET $I_{DS(Sat)} = \frac{k}{2}(V_{GS} - V_T)^2$, $I_{DS(Triode)} = k\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}$, $k_n = \frac{k_n' W}{L}$, $R_{ON} = \frac{1}{k_n' \frac{W}{L} V_{OV}}$
- Consider $\beta = 100$, $V_{BE(Active)} = V_{BE(Sat)} = 0.7\ \text{V}$, $V_{CE(Sat)} = 0.2\ \text{V}$ if not provided.

Question 1: 8 Marks



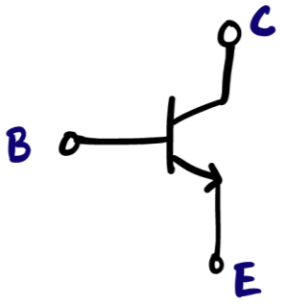
a) Analyze the circuit in the **left figure** above to find f in terms of boolean inputs A, B, C, and D. [CO2] 2

b) Design a circuit using MOSFET logic gates to implement logic function f found from **'a)'**. [CO3] 4

c) Analyze the **right figure** to find i_C and v_{o1} using the Method of Assumed State. Validate your assumptions. [CO2] 4

Question 2: **CO1** 8 Marks

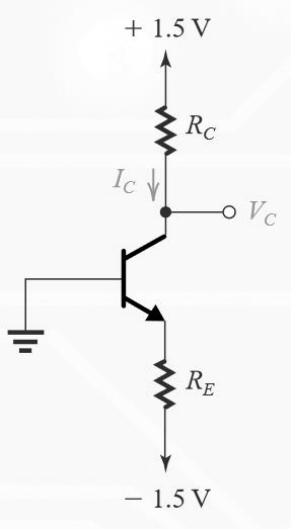
The terminal voltages of various npn transistors are measured during operation in their respective circuits with the following results. In this table, where the entries are in volts, 0 indicates the reference voltage. For each case, identify the mode of operation of the transistor.



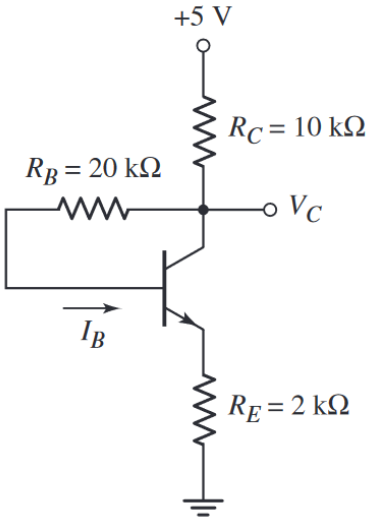
Case	E	B	C	Mode
1.	0	0.7	0.7	
2.	0	0.8	0.1	
3.	−0.7	0	0.7	
4.	−2.7	−2	0	

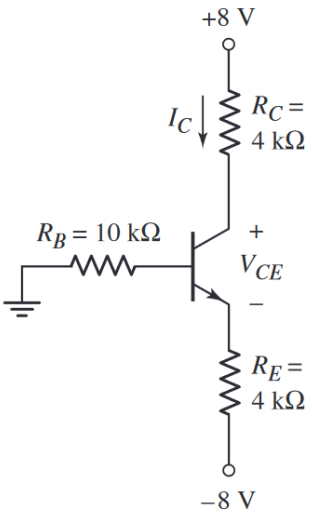
Question 3 — 12 Marks

a. Design the circuit, i.e., determine the Resistor values, to establish $I_C = 0.1\ \text{mA}$ and $V_C = 0.5\ \text{V}$. The transistor exhibits $v_{BE} = 0.8\ \text{V}$ at $i_c = 1\ \text{mA}$, and $\beta = 100$. [CO3] 4

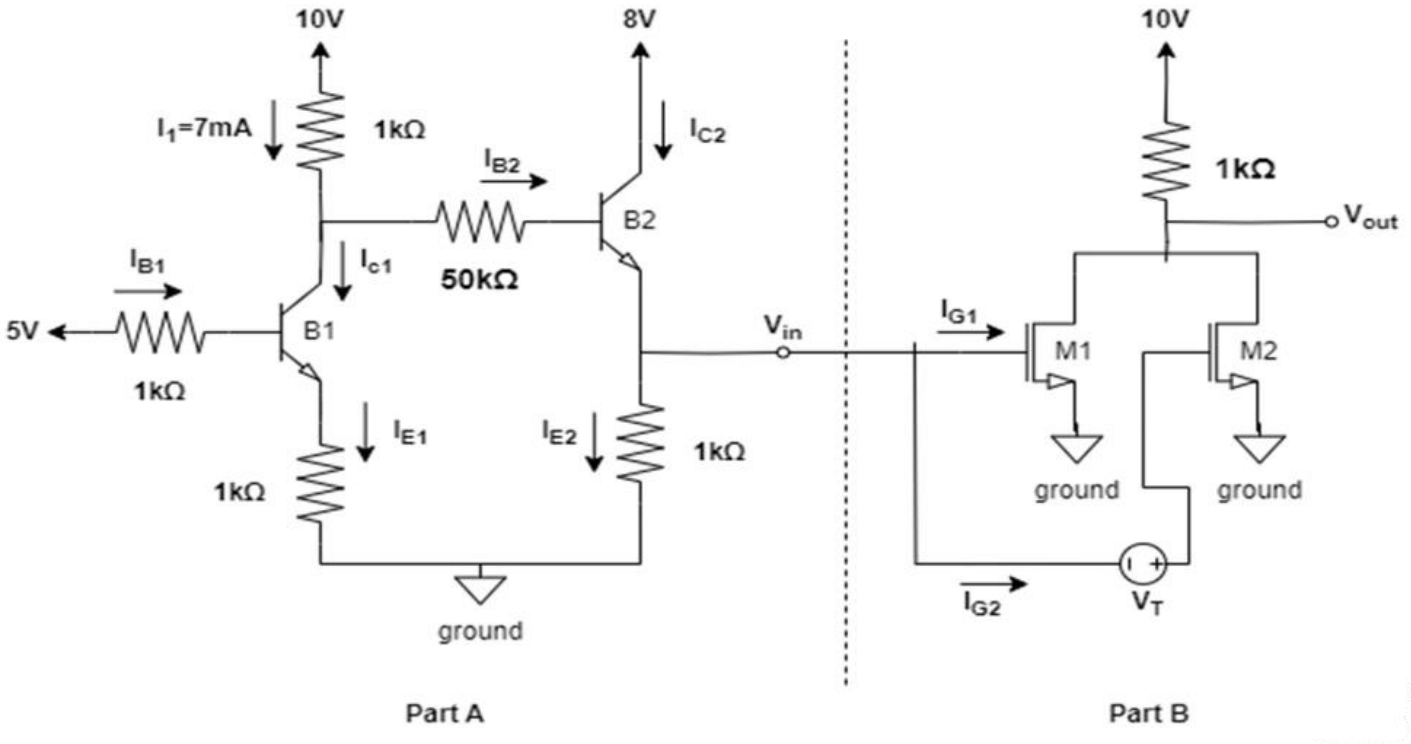


b. For the transistors in the adjacent figure, $\boldsymbol{\beta = 75}$. Find the labelled voltages and currents. [CO2] 8
(Assume $V_{BE_0} = 0.7\ \text{V}$, $V_{CE(\text{sat})} = 0.2\ \text{V}$)





Question 4: CO3 12 Marks



In the circuit above, the BJTs have the following specification: β=100, Forward Active Region: $V_{BE} = 0.7\,V$, $I_C = \beta I_B$, Saturation Region: $V_{BE} = 0.8\,V$, $V_{CE} = 0.2\,V$,or the MOSFETs: $V_T = Threshold\ Voltage\ of\ M1\ and\ M2$.

a) **Determine** i_{g1} and i_{g2}. **[1]**

b) The SR model of MOSFET is more efficient than the S model- Justify this statement. **[1]**

c) Assume, B1 and B2 are in the **Saturation region. Calculate i_{c2}.** **[2]**

d) Assume, B1 is in the **Forward Active region. Calculate Vin.** **[4]**

e) **Draw the VTC** of Part- B assuming, $V_T = 8\,V$. [Use S model of MOSFETs]. **[2]**