Cache FSM

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Legend:
Tag_in = Instr[15:11]
Index = Instr[10:3]
Offset = Instr[2:0]
Data_in = Data_in
Addr = Addr

Wait_Req

Check_Cache

Cache: Enable, Index, Tag_in, Offset, Comp
System: Stall = ~done
Dataout = (done) ? cacheout : 0,
done = hit & valid

Check_Miss 1

Memory: Rd, Addr
System: ~done, stall

Check_Miss 2

Memory: Rd, Addr
System: ~done, stall

Check_Miss 3

Memory: Rd, Addr
Cache: Enable, Write, offset = 0, tag_in,
data_in, ~valid_in
System: ~done, stall

Error
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err

Cache_Write

Cache: Enable, Index, Tag_in, Offset, Comp,
write, data_in
System: Stall = ~done
Dataout = (done) ? cacheout : 0,
done = hit & valid

Cache_Writeback_1

Memory: Wr, data_in, addr
Cache: Enable, Index, Offset = 0
System: stall, ~done

Cache_Writeback_6

System: Stall, ~done

Check_Miss 3

Memory: Rd, Addr
Cache: Enable, Write, offset = 1, tag_in,
data_in, ~valid_in
System: ~done, stall

Cache_Write

Cache: Enable, Write, valid_in, Index, Offset,
Tag_in, Data_in
System: Done, ~stall

Cache_Writeback_2

Memory: Wr, data_in, addr
Cache: Enable, Index, Offset = 1
System: stall, ~done

Cache_Writeback_5

System: Stall, ~done

Check_Miss 4

Cache: Enable, Write, offset = 2, tag_in,
data_in, ~valid_in
System: ~done, stall

Cache_Writeback_3

Memory: Wr, data_in, addr
Cache: Enable, Index, Offset = 2
System: stall, ~done

Cache_Writeback_5

System: Stall, ~done

Check_Miss 5

Cache: Enable, Write, offset = 3, tag_in,
data_in, valid_in
System: done = rd, stall = wr

Cache_Writeback_4

Memory: Wr, data_in, addr
Cache: Enable, Index, Offset = 3
System: stall, ~done

Transitions/labels:
- ~rd, ~wr
- rst
- rd, ~wr
- hit, valid
- rd, wr
- ~rd, wr
- ~valid | (valid & ~dirty)
- ~hit & valid & dirty
- hit & valid
- ~hit | (hit & ~valid)
- Rd
- Wr