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Colibri T20

Datasheet

Revision History

Date	Doc. Rev.	Colibri T20 Version	Changes
18-Nov-2010	Rev. 0.9	V1.0a	Initial Release: Preliminary version
23-Dec-2010	Rev. 0.91	V1.1a	-Add some information about the suspend mode -Remove programmable polarity form Memory Bus control signals - Add preliminary power consumption values - Add Bootstrap chapter - Add External Memory Map information
25-Jul-2011	Rev. 0.92	V1.1a	- Change name form Colibri Tegra 2 to Colibri T20 - Change Picture on front page - Correct spelling mistakes - Add reference to Iris - Add more information about the LCD interface - Add more I2C information - Add IDE Pin Description - Add missing Pins in Chapter 4.4 - Correct Mistake in Memory Bus Tables - Change name IDD_MAX -> IDD_HIGHCPU - Add new RAM / Flash Configuration
26-Jul-2011	Rev. 0.93	V1.1a	- Correct a lot of spelling mistakes - Fix Tegra Signal Names in Table 5-13 - Correct available SW - Add clarifications
09-Feb-2012	Rev 1.0	V1.2	- Fix mechanical drawing - Add Temperature Specification - Add ADC max values - Correct Pin number in Boostrap Table - Correct Table: USB Power Control Pins - Correct Table: Camera Interface Pins - Change recommended pull down value from 100 to 680 Ohm for boot strap pins - Add additional comment to HOTPLUG_DETECT pin.
25-July-2012	Rev 1.1	V1.2	- Add/Change Thermal Diode Max Temp - Corrected comment about RTC reset - Change Wiki links to Dev Center links - Correct Description in Table 5 17 - Update Typical Power Consumption - Remove comment about preinstalled license - Add drawings for pins 99 and 93 - Add a comment about reset states - Add Thermal Design Power
			- Add Clarifications in Chapter 3.2 - Correct description in Table 5-2 - Increase RGB resolution - Add missing multiplexed Pins in Table 3-1 - Add missing GPIO name in Table 3-1 - Add Voltage Range for VCC_BATT - Add clarify comments to VCC_BATT - Correct Spelling Mistakes
20-May-2014	Rev 1.2	V1.2	- Section 5.6.4 Memory Bus Signals Table 5-10: Updated compatible function details and description.

Date	Doc. Rev.	Colibri T20 Version	Changes
			- Section 10.2 Electrical Characteristics
			Table 10.2: Corrected descriptions
			- Section 3.2.1 SODIMM 200 / X1 and Section 5.9
			FFUART, BTUART, STDUART are renamed as UART_A, UART_B, UART_C respectively
02-Dec-2014	Rev 1.3	V1.2	- Section 10.6 renamed and updated
			- Signal name corrected in section 5.4.2
			- Update storage temperature in section 10.5
15-April-2015	Rev 1.4	V1.2	- Section 1.2.4, Interfaces
			Number of available GPIOs has been updated.
14-Feb-2017	Rev 1.5	V1.2	- Updated details and external web-links (Section 1.3)
			- Changed section heading to "Colibri Carrier Board Schematics" (Section 1.3.5)
			- Updated remarks in the Table 5-4 (Section 5.2.1)
			- Added tables containing UART interface pin details (Section 5.9)
			- Added tables containing SD/MMC interface pin details (Section 5.13)
			- Updated external web-links (Section 10.4.1)
17 April 2019	Rev 1.6	V1.2	- Added Remark to flash endurance (Section 1.2.3)
			- Updated web-links (Section 10.4.1)
			- Minor Changes

Contents

1. Introduction

1.1 Hardware

The Colibri T20 is a SODIMM sized computer module based on the NVIDIA© Tegra 2 embedded system-on-a-chip. The Cortex A9 dual core CPU runs at speeds up to 1 GHz. The module delivers very high CPU and graphic performance with minimum power consumption.

The integrated NVIDIA Graphics enables visually rich, smooth and fast user interfaces.

The module targets a wide range of applications, including: Digital Signage, Medical Devices, Navigation, Industrial Automation, HMIs, Avionics, Entertainment System, POS, Data Acquisition, Thin Clients, Robotics, Gaming and much more

It offers a wide range of interfaces from simple GPIOs, industry standard I2C and SPI buses through to high speed USB 2.0 interfaces and a high speed memory bus. The HDMI interface makes it very easy to connect large, full HD resolution displays.

Existing customers will benefit from an extremely easy migration path from the current Colibri PXAxxx module range to the Colibri T20 – all Colibri modules are electrically pin compatible. New customers will also appreciate the ability to select the Colibri module most suitable for their application to achieve the optimum price/performance balance without the need to support different carrier board designs.

1.2 Software

Toradex provides Windows CE 6.0, Windows Embedded Compact 7 and Linux.
Please check our Developer Center (http://developer.toradex.com) for more information about the current SW support.
Toradex works with partners in case you require another Operating System. For more information contact our Support.

1.2.1 Windows CE

The WinCE images contain drivers for the most common interfaces and are easily customizable through registry settings. The Windows CE image that is shipped as standard with all Colibri modules has been optimized for performance and stability and is used by thousands of customers worldwide over a diverse range of industries.
Toradex is highly experienced in Windows CE customization and application development and can ensure you benefit from this experience through our engineering support channels.

Main Features

1.2.2 CPU

- ✓ NVIDIA Tegra 2 dual-core Cortex-A9 MPcore
- ✓ Both CPUs have 32KB Instruction and 32KB Data Level 1 caches
- ✓ 1MB shared Level 2 cache
- ✓ VFPv3 Floating Point Unit

1.2.3 Memory

- ✓ 256 MB DDR2 (32 Bit) / 512MB DDR2 (32 Bit)
- ✓ 512MB NAND FLASH (8 Bit) / 1GByte NAND FLASH (8 Bit)

*Flash write endurance is limited. Extensive writing to the memory can wear out the memory cell. Software wear levelling makes sure the cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.2.4 Interfaces

- ✓ 16/32-Bit Data Bus
- ✓ LCD RGB (1920 x 1200 24bpp)
- ✓ HDMI 1.3 1080p (1920x1080)
- ✓ Analog Video (1600x1200)
- ✓ Touch Screen (4/5 wire)
- ✓ Audio I/O (16 Bit stereo)
- ✓ CMOS/CCD Image Sensor Interface (12MP)
- ✓ I2C
- ✓ 4x SPI
- ✓ 5x UART
- ✓ 2x SDCard up to 8Bit (SDIO, MMC)
- ✓ Up to 153 GPIOs
- ✓ USB 2.0 high speed hosts
- ✓ USB 2.0 high speed device
- ✓ 10/100 Mbit Ethernet
- ✓ One-Wire
- ✓ Keypad
- ✓ 4x PWM
- ✓ S/PDIF

1.2.5 HD Video Decode

- ✓ H.264
  - o Baseline Profile (B frames) — 1080p/20Mbps
  - o Main Profile (B Frames, CAVLC) — 1080p
  - o Main Profile (B Frames, CABAC, no weighted prediction) — 720p/6Mbps
  - o High Profile (B Frames, CABAC, no weighted prediction) — TBD

- ✓ WMV9 VC-1 (Simple, Main and Advanced Profiles) — 1080p/20Mbps
- ✓ MPEG-4 (Simple, B frames and ASP Profiles) — 1080p/8Mbps
- ✓ H.263 (Profile 0) — 720×576/4Mbps
- ✓ DiVX (DiVX 4/5) — 1080p/8Mbps
- ✓ XviD (XviD Home Theater) — 1080p/8Mbps
- ✓ MPEG-2 (Main Profile @ Main Level) — 720×576/10Mbps
- ✓ VP6 (simple and advanced profile) — 720p30/2Mbps
- ✓ Sorenson (simple and advanced profile) — 720×576/4Mbps
- ✓ JPEG up to 80 Mpixel per second

1.2.6 HD Video Encode

- ✓ H.264 (Baseline Profile) — 1080p/10Mbps

- ✓ MPEG-4 (Simple Profile) — 720p/4Mbps
- ✓ H.263 (Profile 0) — 720×576/4Mbps
- ✓ JPEG up to 80 MPixel per second

1.2.7 Ultra-low Power NVIDIA GeForce GPU

- ✓ OpenGL® ES 2.0
- ✓ Peak Triangle Rate: 71 million triangles per second
- ✓ Peak File Rate (with Z-reject): 1200 million pixels per second
- ✓ Programmable pixel shader
- ✓ Programmable vertex and lighting
- ✓ CSAA support (Coverage Sampling Antialiasing)
- ✓ 2K x 2K texture and 4K x 4K render resolutions supported
- ✓ Advanced 2D and vector engine

1.2.8 Digital Audio Decode

- ✓ AAC-LC, AAC+, eAAC+
- ✓ AMR-WB,AMR-NB
- ✓ WMA7, WMA8, WMA9, and WMA10
- ✓ MP3
- ✓ PCM/WAV
- ✓ SBC

1.2.9 Digital Audio Encode

- ✓ AAC-LC
- ✓ AMR-WB,AMR-NB
- ✓ PCM/WAV
- ✓ SBC

1.2.10 Timers

- ✓ 4 timers
- ✓ 1 Micro Second resolution
- ✓ Watchdog function

1.2.11 Supported Operating Systems

- ✓ Windows CE 6.0
- ✓ Windows Embedded Compact 7.0
- ✓ Linux
- ✓ Other operating systems are available through 3rd party companies

1.3 Reference Documents

1.3.1 Ethernet Controller

Colibri T20 uses the Asix AX88772B Ethernet chip
http://www.asix.com.tw

1.3.2 Audio Codec and Touch Screen Controller

Colibri T20 uses the Cirrus Logic / Wolfson WM9715L Audio Controller.
https://www.cirrus.com/products/wm9715/

1.3.3 Toradex Migration Guide

This document provides additional information about the pin usage and describes functional compatibility with the rest of the Colibri family. Please study this document in detail prior to starting your carrier board design.
http://docs.toradex.com/100188-colibri-migration-and-design-guide.pdf
http://developer.toradex.com/carrier-board-design

1.3.4 Toradex Developer Center

You can find a lot of additional information in the Developer Center which is updated with the latest product support information on a regular basis.
http://www.developer.toradex.com

1.3.5 Colibri Carrier Board Schematics

We provide the complete schematics and the Altium project file which includes library symbols and IPC-7351 compliant footprints for the Colibri Evaluation Board and other Carrier Boards free of charge. This is a great help when designing your own Carrier Board.
http://developer.toradex.com/carrier-board-design/reference-designs

2. Architecture Overview

2.1 Block Diagram
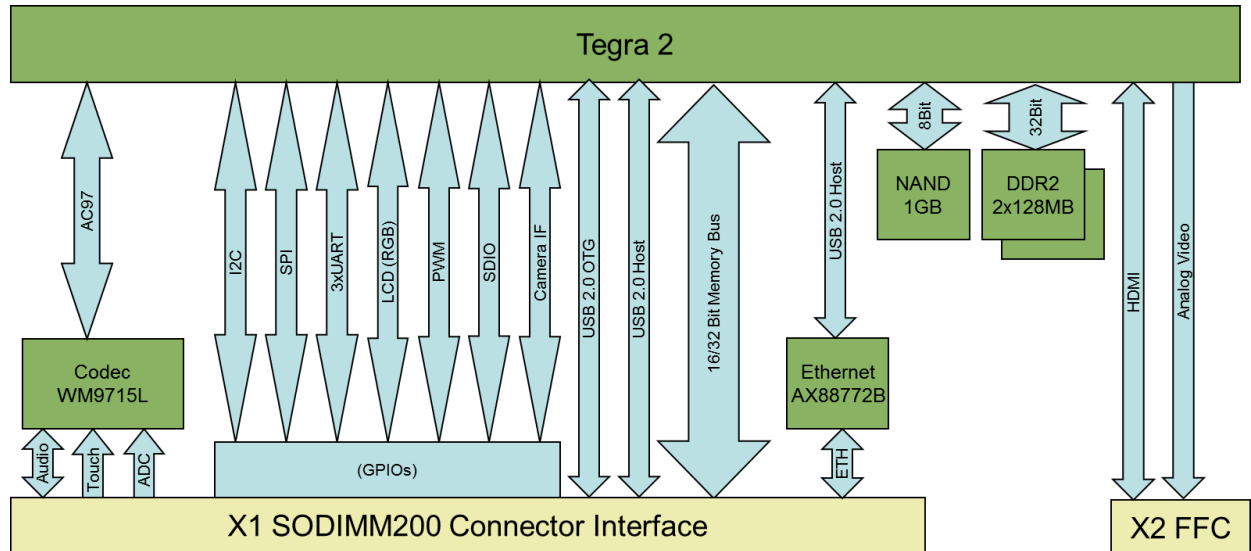
Figure 1 Colibri T20 Block Diagram

3. Colibri T20 Connectors

3.1 Physical Locations

The Colibri T20 is equipped with a 200 Pin SODIMM edge connector (X1) and an FCC connector (X2). The position of the connectors is shown in the figure below.
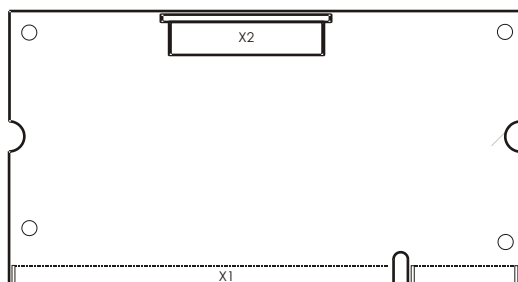
Figure 2 Location of the Colibri T20 connectors. (Bottom of the module)

3.2 Assignment

3.2.1 SODIMM 200 / X1

The following table describes the SODIMM 200 way connector pin out. It should be noted that some of the pins are multiplexed; this means there is more than one Tegra pin connected to one SODIMM or FFC pin. For example, SDIO3_CMD and VI_D6 GPIO99 GPIO113 are both assigned to SODIMM pin 67. Care should be taken to ensure that multiplexed Tegra pins are tri-stated when they are not being used (e.g., if Tegra pin A and pin B are tied to SODIMM pin 1, then if you are driving Tegra pin A, then pin B should be tri-stated). Additional information can be found in chapter 4.1: Function Multiplexing.

- X1 Pin: Pin number on the SODIMM connector (X1).
- Compatible function: The default function which is compatible with all Colibri modules.
                                IMPORTANT: There are some limitations. You can find more
                                information about pin compatibility in the "Colibri Migration Guide".
- Tegra 2 Pin Name: The name of the pin of the Tegra chip.
- GPIO Name: The name of the GPIO function which is available on this pin.

Table 3-1 X1 Connector

X1 Pin	Compatible Function	Tegra 2 Pin Name	GPIO Name	X1 Pin	Compatible Function	Tegra 2 Pin Name	GPIO Name
1	MIC_IN	WM9715 pin		2	AD3	WM9715 pin	
3	MIC_GND	WM9715 pin		4	AD2	WM9715 pin	
5	LINEIN_L	WM9715 pin		6	AD1	WM9715 pin	
7	LINEIN_R	WM9715 pin		8	AD0	WM9715 pin	
9	VSS_AUDIO	WM9715 pin		10	AVDD_AUDIO	WM9715 pin	
11	VSS_AUDIO	WM9715 pin		12	AVDD_AUDIO	WM9715 pin	
13	HEADPHONE_GND	WM9715 pin		14	TSPX	WM9715 pin	
15	HEADPHONE_L	WM9715 pin		16	TSMX	WM9715 pin	
17	HEADPHONE_R	WM9715 pin		18	TSPY	WM9715 pin	
19	UART_C_RXD	UART2_RXD	GPIO_C3	20	TSMY	WM9715 pin	
21	UART_C_TXD	UART2_TXD	GPIO_C2	22		VI_GP3	GPIO_BB4
23	UART_A_DTR	SDIO1_CLK	GPIO_Z0	24	BATT_FAULT	VI_GP4	GPIO_BB5
25	UART_A_CTS	SDIO1_CMD	GPIO_Z1	26	nRESET_EXT		

X1 Pin	Compatible Function	Tegra 2 Pin Name	GPIO Name	X1 Pin	Compatible Function	Tegra 2 Pin Name	GPIO Name
27	UART_A_RTS	SDIO1_DAT0	GPIO_Y7	28	PWM<B>	SDIO3_DAT2	GPIO_B5
29	UART_A_DSR	LCD_PWR1	GPIO_C1	30	PWM<C>	SDIO3_CLK	GPIO_A6
31	UART_A_DCD	LCD_PWR2	GPIO_C6	32	UART_B_CTS	GMI_AD18	GPIO_B1
33	UART_A_RXD	SDIO1_DAT2	GPIO_Y5	34	UART_B_RTS	GMI_AD19	GPIO_K7
35	UART_A_TXD	SDIO1_DAT3	GPIO_Y4	36	UART_B_RXD	GMI_AD17	GPIO_B0
37	UART_A_RI	SDIO1_DAT1	GPIO_Y6	38	UART_B_TXD	GMI_AD16	GPIO_J7
39	GND			40	VCC_BATT		
41	GND			42	3V3		
43	WAKEUP Source0, MM_CD	GMI_WP_N	GPIO_C7	44	L_BIAS	LCD_DE (LCD_M1)	GPIO_J1 (GPIO_W1)
45		GPIO_PV3	GPIO_V3	46	LDD<7>	LCD_D7	GPIO_E7
47	MM_CLK	GMI_CS5_N	GPIO_I2	48	LDD<9>	LCD_D9	GPIO_F1
49	MM_DAT<1>	GMI_AD21	GPIO_AA1	50	LDD<11>	LCD_D11	GPIO_F3
51	MM_DAT<2>	GMI_AD22	GPIO_AA2	52	LDD<12>	LCD_D12	GPIO_F4
53	MM_DAT<3>	GMI_AD23	GPIO_AA3	54	LDD<13>	LCD_D13	GPIO_F5
55	SDA1 (PS2 Mouse GPIO)	SDIO3_DAT1	GPIO_B6	56	L_PCLK_WR	LCD_PCLK	GPIO_B3
57	LDD<16>	LCD_D16	GPIO_M0	58	LDD<3>	LCD_D3	GPIO_E3
59	PWM<A>, CIF_DD<7>	SDIO3_DAT3 VI_D7	GPIO_B4 GPIO_L5	60	LDD<2>	LCD_D2	GPIO_E2
61	LDD<17>	LCD_D17	GPIO_M1	62	LDD<8>	LCD_D8	GPIO_F0
63	SCL1 (PS2 Mouse GPIO)	SDIO3_DAT0	GPIO_B7	64	LDD<15>	LCD_D15	GPIO_F7
65	CIF_DD<9>, SDA2 (PS2 Keyboard GPIO)	VI_D9	GPIO_L7	66	LDD<14>	LCD_D14	GPIO_F6
67	PWM<D>,CIF_DD<6>	SDIO3_CMD VI_D6	GPIO_A7 GPIO_L4	68	L_LCLK_A0	LCD_HSYNC	GPIO_J3
69	SCL2 (PS2 Keyboard GPIO)	VI_D10	GPIO_T2	70	LDD<1>	LCD_D1	GPIO_E1
71	CIF_DD<0>, BL_ON (LCD back-light GPIO)	VI_D0	GPIO_T4	72	LDD<5>	LCD_D5	GPIO_E5
73		VI_GP6	GPIO_A0	74	LDD<10>	LCD_D10	GPIO_F2
75	CIF_MCLK,	VI_MCLK	GPIO_T1	76	LDD<0>	LCD_D0	GPIO_E0
77		VI_D11	GPIO_T3	78	LDD<4>	LCD_D4	GPIO_E4
79	CIF_DD<4>	VI_D4	GPIO_L2	80	LDD<6>	LCD_D6	GPIO_E6
81	CIF_FV	VI_VSYNC	GPIO_D6	82	L_FCLK_RD	LCD_VSYNC	GPIO_J4
83	GND			84	3V3		
85	CIF_DD<8>,	VI_D8	GPIO_L6	86	SSPFRM	SDIO3_DAT6	GPIO_D3
87	nRESET_OUT	GMI_RST_N	GPIO_I4	88	SSPSCLK	SDIO3_DAT5	GPIO_D0
89	nWE	GMI_WR_N	GPIO_I0	90	SSPRXD	SDIO3_DAT4	GPIO_D1
91	nOE	GMI_OE_N	GPIO_I1	92	SSPTXD	SDIO3_DAT7	GPIO_D4
93	RDnWR	GMI_WR_N	GPIO_I0 GPIO_W0	94	CIF_LV	VI_HSYNC	GPIO_D7
95	RDY	GMI_WAIT GMI_IORDY	GPIO_I7 GPIO_I5	96	CIF_PCLK,	VI_PCLK	GPIO_T0

X1 Pin	Compatible Function	Tegra 2 Pin Name	GPIO Name	X1 Pin	Compatible Function	Tegra 2 Pin Name	GPIO Name
97	CIF_DD<5>	VI_D5	GPIO_L3	98	CIF_DD<1>	VI_D1	GPIO_D5
99		GMI_WR_N	GPIO_I0 GPIO_Z3	100		SPI1_SCK	GPIO_X5
101	CIF_DD<2>	VI_D2	GPIO_L0	102		SPI1_CS0_N	GPIO_X6
103	CIF_DD<3>	VI_D3	GPIO_L1	104		SPI1_MISO	GPIO_X7
105	nCSx	GMI_CS4_N	GPIO_K2	106	nCSx	GMI_CS3_N	GPIO_K4
107	nCSx	GMI_CS2_N	GPIO_K3	108	3V3		
109	GND			110	ADDRESS8	GPIO_PU2	GPIO_U2
111	ADDRESS0	UART2_RTS_N	GPIO_J6	112	ADDRESS9	GPIO_PU3	GPIO_U3
113	ADDRESS1	UART2_CTS_N	GPIO_J5	114	ADDRESS10	GPIO_PU4	GPIO_U4
115	ADDRESS2	UART3_TXD	GPIO_W6	116	ADDRESS11	GPIO_PU5	GPIO_U5
117	ADDRESS3	UART3_RXD	GPIO_W7	118		GPIO_PU6	GPIO_U6
119	ADDRESS4	UART3_RTS_N	GPIO_C0	120		DAP4_FS	GPIO_P4
121	ADDRESS5	UART3_CTS_N	GPIO_A1	122		DAP4_DIN	GPIO_P5
123	ADDRESS6	GPIO_PU0	GPIO_U0	124		DAP4_DOUT	GPIO_P6
125	ADDRESS7	GPIO_PU1	GPIO_U1	126		GMI_CS0_N	GPIO_J0
127		CAM_I2C_SDA	GPIO_BB3	128		GMI_CS1_N	GPIO_J2
129	USBH_PEN	SPI2_CS1_N	GPIO_W2	130		GMI_CS6_N	GPIO_I3
131	USBH_OC	SPI2_CS2_N	GPIO_W3	132		GMI_CS7_N	GPIO_I6
133		CAM_I2C_SCL	GPIO_BB2	134		SPI1_MOSI	GPIO_X4
135		ACC1_DETECT SPDIF_IN	- GPIO_K6	136		SPI2_CS0_N LCD_D18	GPIO_X3 GPIO_M2
137	USBC_DET (USB cable detect GPIO)	USB1_VBUS SPDIF_OUT	- GPIO_X3	138		SPI2_SCK LCD_D19	GPIO_X2 GPIO_M3
139	USBH_P	USB3_DP		140		SPI2_MISO LCD_D20	GPIO_X1 GPIO_M4
141	USBH_N	USB3_DN		142		SPI2_MOSI LCD_D21	GPIO_X0 GPIO_M5
143	USBC_P	USB1_DP		144		DAP2_DOUT LCD_D22	GPIO_A5 GPIO_M6
145	USBC_N	USB1_DN		146		DAP2_DIN LCD_D23	GPIO_A4 GPIO_M7
147	GND			148	3V3		
149	DATA0	GMI_AD0	GPIO_G0	150		GMI_ADV_N	GPIO_K0
151	DATA1	GMI_AD1	GPIO_G1	152		GMI_CLK	GPIO_K1
153	DATA2	GMI_AD2	GPIO_G2	154		LCD_PWR0	GPIO_B2
155	DATA3	GMI_AD3	GPIO_G3	156		LCD_SDIN	GPIO_Z2
157	DATA4	GMI_AD4	GPIO_G4	158		LCD_SDOUT	GPIO_N5
159	DATA5	GMI_AD5	GPIO_G5	160		LCD_CS0_N	GPIO_N4
161	DATA6	GMI_AD6	GPIO_G6	162		LCD_DC0	GPIO_N6
163	DATA7	GMI_AD7	GPIO_G7	164		LCD_SCK	GPIO_Z4
165	DATA8	GMI_AD8	GPIO_H0	166		GMI_AD24	GPIO_AA4
167	DATA9	GMI_AD9	GPIO_H1	168		GMI_AD25	GPIO_AA5
169	DATA10	GMI_AD10	GPIO_H2	170		GMI_AD26	GPIO_AA6
171	DATA11	GMI_AD11	GPIO_H3	172		GMI_AD27	GPIO_AA7

X1 Pin	Compatible Function	Tegra 2 Pin Name	GPIO Name	X1 Pin	Compatible Function	Tegra 2 Pin Name	GPIO Name
173	DATA12	GMI_AD12	GPIO_H4	174		DAP1_FS	GPIO_N0
175	DATA13	GMI_AD13	GPIO_H5	176		DAP1_DIN	GPIO_N1
177	DATA14	GMI_AD14	GPIO_H6	178		DAP1_DOUT	GPIO_N2
179	DATA15	GMI_AD15	GPIO_H7	180		DAP1_SCLK	GPIO_N3
181	GND			182	3V3		
183	LINK_AKT	AX88772B pin		184		DAP2_SCLK	GPIO_A3
185	SPEED100	AX88772B pin		186		DAP2_FS	GPIO_A2
187	TXO-	AX88772B pin		188		DAP4_SCLK	GPIO_P7
189	TXO+	AX88772B pin		190	MM_CMD	GMI_DPD	GPIO_T7
191	AGND_LAN	AX88772B pin		192	MM_DAT<0>	GMI_AD20	GPIO_AA0
193	RXI-	AX88772B pin		194	I2C_SDA	GEN1_I2C_SDA	GPIO_C5
195	RXI+	AX88772B pin		196	I2C_SCL	GEN1_I2C_SCL	GPIO_C4
197	GND			198	3V3		
199	GND			200	3V3		

3.2.2 HDMI / X2

This connector is not backward compatible with the Colibri PXAxxx family. Its primary purpose is to provide the signals for the HDMI/DVI and analog (VGA) display interface. The only pin on this connecter which provides a GPIO function is pin 14 (GPIO_N7).

Table 3-2 X2 Connector

Pin	Name	Description	Direction
1	GND (Shield)		
2	TMDS_CLK_P	Transmit Clock Positive	O
3	TMDS_CLK_N	Transmit Clock Negative	O
4	GND		
5	TMDS_DATA0_P	Data Lane 0 Positive	O
	TMDS_DATA0_N	Data Lane 0 Negative	O
7	GND		
8	TMDS_DATA1_P	Data Lane 1 Positive	O
9	TMDS_DATA1_N	Data Lane 1 Negative	O
10	GND		
11	TMDS_DATA2_P	Data Lane 2 Positive	O
12	TMDS_DATA2_N	Data Lane 2 Negative	O
13	3V3_DDC_OUT		O
14	HOTPLUG_DETECT (GPIO_N7)	Hot Plug Detection, 5V Tolerant, 100K Ohm pull down on Colibri. 1K Ohm Serie resistor on base board recommended	I
15	DDC_SCL	DDC Serial Clock used for HDMI and the VGA interface. Open Collector Output 5V tolerant. To communicate with an HDMI/VGA display you need to pull up this line to 5V.	O
16	DDC_SDA	Serial Data. See DDC_SCL description	I/O
17	GND		
18	VGA_RED	Red signal for Analog RGB and Component TV out connections. For TV S-Video Output, this carries the color (chrominance) information.*	O
19	GND		
20	VGA_GREEN	Green signal for Analog RGB and Component TV out connections. For TV S-Video Output, this carries the intensity (Luminance) information. Also used for Composite TV Output when this is the only TV Output interface.*	O
21	GND		
22	VGA_BLUE	Blue signal for Analog RGB and Composite TV out connections. Used for Composite TV out when VGA_RED and VGA_GREEN are used for S-Video out.*	O
23	VGA_VSYNC	Vertical Sync for Analog RGB (VGA) Interface. It is recommended to level shift this signal before going to the monitor. (Typically 5V)	O
24	VGA_HSYNC	Horizontal Sync for Analog RGB (VGA) Interface. It is recommended to level shift this signal before going to the monitor. (Typically 5V)	O

4. I/O Pins

4.1   Function Multiplexing

Most of the NVIDIA Tegra Processors I/O pins have up to four special functions. They can be used as "normal" GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O).
For example, the Tegra Pin on connector X1, pin 21, has the primary function UART2_TXD, but can also provide the following alternative functions: SPDIF_IN, UART1_RTS_N or SPI4_SCK.

The default setting for this pin is the primary function UART2_TXD. It is strongly recommended whenever possible to use a pin for a function which is compatible with all Colibri modules. This guarantees the best compatibility with the standard software and with the other modules in the Colibri family.

All of the pins in the Tegra family are organized into groups. It is only possible to change the alternative function of a complete group. The exception to this rule is when a pin is used as a GPIO; the GPIO function can be enabled/disabled on a per pin base.

Most of the alternative functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In a few cases, the available alternative functions of certain pins on the Tegra device were constrained; to allow maximum flexibility. Some of these pins are paired and share the same SODIMM pin. As previously mentioned, ensure that the unused pin in the pair is tri-stated to avoid undesired behavior and/or hardware damage.
The following X1 connector pins are connected to more than one Tegra:

Table 4-1 Colibri Multiplexed Pins

X1 Pin #	Tegra Pin 1	Tegra Pin 2	Remarks
44	L_BIAS	LCD_M1	
59	VI_D7	SDIO3_DAT3	
67	VI_D6	SDIO3_CMD	
93	GMI_WR_N	LCD_CS1_N	GMI_WR_N is connected via a 3-State buffer with LCD_CS1_N. To tristate the buffer set GEN2_I2C_SDA (GPIO_PT6) to high. (default state). For more information see the Figure 3.
95	GMI_IORDY	GMI_WAIT	
99	GMI_WR_N	LCD_WR_N	GMI_WR_N is connected via a 3-State buffer with LCD_WR_N. To tristate the buffer set GEN2_I2C_SCL (GPIO_PT5) to high. (default state). For more information see the Figure 4.
135	ACC1_DETECT	SPDIF_IN	
136	SPI2_CS0_N	LCD_D18	
137	USB1_VBUS	SPDIF_OUT	
138	SPI2_CLK	LCD_D19	
140	SPI2_MISO	LCD_D20	
142	SPI2_MOSI	LCD_D21	
144	DAP2_OUT	LCD_D22	
146	DAP2_DIN	LCD_D23	

In the table in chapter 4.4 you will find a list of all pins which have alternative functions. There you can see which alternative function is available for each individual pin.
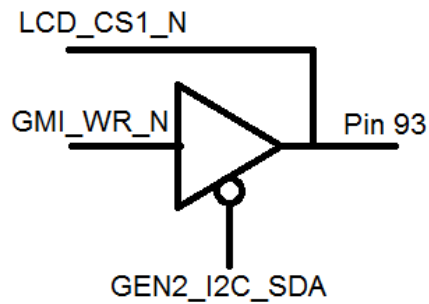

Figure 3
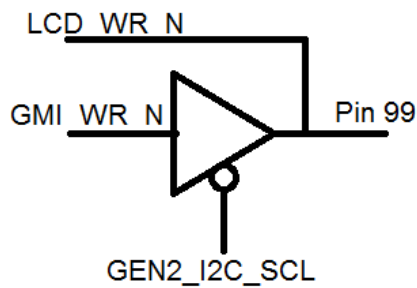
Figure 4

4.2 Pin Control

For all pins with a GPIO function, the following controls are available.
- Output Enable Control: Normal I/O or tri-state
- Pull-up/down Control: Normal, pull up or pull down (internal resistors between ~75KOhm to 150KOhm)
- Alternative Function Selection: Up to 4 special functions are available per pin.
- Drive Control: Output drive strength, Input Schmitt trigger enabled/disabled

These controls affect pins on a group level rather than individually (e.g. setting a pull up will pull up all pins in a group, rather than an individual pin). The table in chapter 4.4 explains pin grouping.

4.3 Pin Reset Status

After a reset the pins can be in different modes. Most of them are tri-stated, pulled up or pulled low. A few are driven low or high. Please check the table in chapter 4.4 for a list of reset states for each of the pins. Please note that software may change the state of these pins.

4.4 List Functions

Here you can find a list of all the Tegra pins which are available on the SODIMM connector X1. It shows what alternative functions are available for each pin. You will also find the Tegra GPIO name and the state of the pin immediately after reset (power on or software reset). Bootloader SW can change this state short after start. By default the Bootloader does change some states.

Reset Status Description
z: Tristate
pd: Pull Down (about 100kOhm)
pu: Pull Up (about 100kOhm)
pd+pu: Pulled Up and Pulled Down (due multiplexed pins)
0:          Drive Low
1:          Drive High

Function Short Forms
UART: Serial Ports (Universal Asynchronous Receiver/Transmitter)
VI: Video Interface (Camera Interface)
SPDIF: S/PDIF (Sony-Philips Digital Interface I/O)
SDIO: Secure Card I/O (SD, MMC, CE-ATA, eMMC)
HSMM: High Speed (SD, MMC, CE-ATA, eMMC)
SPI: Serial Peripheral Interface Bus
GMI: General Memory Interface
LCD: Parallel display interface
TWC: Three Wire Interface
OWR: One Wire Interface
DAP: Digital Audio Port (I2S and AC97)
IDE: Parallel ATA
PMFM: Pulse Wide Modulation

X1 Pin	Tegra Pin Name	Primary Function	Alt1	Alt2	Alt3	GPIO	Group	Reset
19	UART2_RXD	UART2_RXD	SPDIF_OUT	UART1_CTS_N	SPI4_MOSI	C3	uad	pu
21	UART2_TXD	UART2_TXD	SPDIF_IN	UART1_RTS_N	SPI4_SCK	C2	uad	pu
22	VI_GP3			VI_GP3	SPI1_SCK	BB4	dte	z
23	SDIO1_CLK	SDIO1_CLK			UART1_DTR_N	Z0	sdio1	pu
24	VI_GP4			VI_GP4	SPI1_CS0_N	BB5	dte	z
25	SDIO1_CMD	SDIO1_CMD			UART1_CTS_N	Z1	sdio1	pu
27	SDIO1_DAT0	SDIO1_DAT0		UART5_RTS_N	UART1_RTS_N	Y7	sdio1	pu
28	SDIO3_DAT2	PMFM_PWM1	TWC_CLK	SDIO3_DAT2	SPI3_CS0_N	B5	sdc	pu
29	LCD_PWR1	LCD1_PWR1	LCD2_PWR1			C1	lpw1	pu
30	SDIO3_CLK	UART1_TXD	PMFM_PWM2	SDIO3_CLK	SPI3_SCK	A6	sdd	pu
31	LCD_PWR2	LCD1_PWR2	LCD2_PWR2	SPI3_MISO		C6	lpw2	pu
32	GMI_AD18	UART4_CTS_N	SPI4_MISO	GMI_AD18	SFLASH_DIN	B1	gmc	z
33	SDIO1_DAT2	SDIO1_DAT2		UART5_RXD	UART1_RXD	Y5	sdio1	pu
34	GMI_AD19	UART4_RTS_N	SPI4_CS1_N	GMI_AD19		K7	gmc	z
35	SDIO1_DAT3	SDIO1_DAT3		UART5_TXD	UART1_TXD	Y4	sdio1	pu
36	GMI_AD17	UART4_RXD	SPI4_MOSI	GMI_AD17	SFLASH_DOUT	B0	gmc	z
37	SDIO1_DAT1	SDIO1_DAT1		UART5_CTS_N	UART1_RI_N	Y6	sdio1	pu
38	GMI_AD16	UART4_TXD	SPI4_SCK	GMI_AD16	GMI_INT2	J7	gmc	z
43	GMI_WP_N	IDE_HIRQ	NAND_CS5_N	GMI_WP_N	GMI_INT1	C7	gmb	0
44	LCD_M1	LCD1_LM1	LCD2_LM1			W1	lm1	pu
44	LCD_DE	LCD1_DE	LCD2_DE			J1	lspi	pu
45	GPIO_PV3	CLK12M_OUT				V3	uac	z
46	LCD_D7	LCD1_D7	LCD2_D7			E7	ld7	pd
47	GMI_CS5_N	IDE_DMARQ		GMI_CS5_N	HSMMC_CLK	I2	atb	1
48	LCD_D9	LCD1_D9	LCD2_D9			F1	ld9	pd
49	GMI_AD21	UART5_RXD	SPI3_MOSI	GMI_AD21	HSMMC_DAT1	AA1	gma	z
50	LCD_D11	LCD1_D11	LCD2_D11			F3	ld11	pd
51	GMI_AD22	UART5_CTS_N	SPI3_MISO	GMI_AD22	HSMMC_DAT2	AA2	gma	z
52	LCD_D12	LCD1_D12	LCD2_D12			F4	ld12	pd
53	GMI_AD23	UART5_RTS_N	SPI3_CS0_N	GMI_AD23	HSMMC_DAT3	AA3	gma	z
54	LCD_D13	LCD1_D13	LCD2_D13			F5	ld13	pd
55	SDIO3_DAT1		TWC_DIN	SDIO3_DAT1	SPI3_MOSI	B6	sdc	pu
56	LCD_PCLK	LCD1_PCLK	LCD2_PCLK			B3	lsc0	pu
57	LCD_D16	LCD1_D16	LCD2_D16			M0	ld16	pd
58	LCD_D3	LCD1_D3	LCD2_D3			E3	ld3	pd
59	VI_D7		SDIO2_DAT5	VI_D7		L5	dtd	pd+pu
59	SDIO3_DAT3	PMFM_PWM0	TWC_CS_N	SDIO3_DAT3	SPI3_CS1_N	B4	sdc	pd+pu
60	LCD_D2	LCD1_D2	LCD2_D2			E2	ld2	pd

X1 Pin	Tegra Pin Name	Primary Function	Alt1	Alt2	Alt3	GPIO	Group	Reset
61	LCD_D17	LCD1_D17	LCD2_D17			M1	ld17	pd
62	LCD_D8	LCD1_D8	LCD2_D8			F0	ld8	pd
63	SDIO3_DAT0		TWC_DO	SDIO3_DAT0	SPI3_MISO	B7	sdc	pu
64	LCD_D15	LCD1_D15	LCD2_D15			F7	ld15	pd
65	VI_D9		SDIO2_DAT7	VI_D9		L7	dtd	pd
66	LCD_D14	LCD1_D14	LCD2_D14			F6	ld14	pd
67	VI_D6		SDIO2_DAT4	VI_D6		L4	dtd	pd+pu
67	SDIO3_CMD	UART1_RXD	PMFM_PWM3	SDIO3_CMD	SPI2_SCK	A7	sdb	pd+pu
68	LCD_HSYNC	LCD1_HSYNC	LCD2_HSYNC			J3	lhs	pu
69	VI_D10			VI_D10	SPI1_MOSI	T2	dtb	pd
70	LCD_D1	LCD1_D1	LCD2_D1			E1	ld1	pd
71	VI_D0			VI_D0		T4	dta	pd
72	LCD_D5	LCD1_D5	LCD2_D5			E5	ld5	pd
73	VI_GP6			VI_GP6		A0	dte	z
74	LCD_D10	LCD1_D10	LCD2_D10			F2	ld10	pd
75	VI_MCLK	PLLC_OUT1	PLLP_OUT2	PLLP_OUT3	VI_SENSOR_CLK	T1	csus	pd
76	LCD_D0	LCD1_D0	LCD2_D0			E0	ld0	pd
77	VI_D11			VI_D11	SPI1_MISO	T3	dtb	pd
78	LCD_D4	LCD1_D4	LCD2_D4			E4	ld4	pd
79	VI_D4		SDIO2_DAT2	VI_D4		L2	dtd	pd
80	LCD_D6	LCD1_D6	LCD2_D6			E6	ld6	pd
81	VI_VSYNC			VI_VSYNC		D6	dtc	pd
82	LCD_VSYNC	LCD1_VSYNC	LCD2_VSYNC			J4	lvs	pu
85	VI_D8		SDIO2_DAT6	VI_D8		L6	dtd	pd
86	SDIO3_DAT6	SPDIF_IN	SPI4_CS0_N	SDIO3_DAT6	SPI2_CS0_N	D3	slxc	pu
87	GMI_RST_N	IDE_RESET	NAND_CLE	GMI_RST_N		I4	ata	0
88	SDIO3_DAT5		SPI4_SCK	SDIO3_DAT5	SPI2_MOSI	D0	slxk	pd
89	GMI_WR_N	IDE_WR_N	NAND_WE_N	GMI_WR_N		I0	atc	pu
90	SDIO3_DAT4		SPI4_MISO	SDIO3_DAT4	SPI2_MISO	D1	slxa	pu
91	GMI_OE_N	IDE_OE_N	NAND_RE_N	GMI_OE_N		I1	atc	pu[1]
92	SDIO3_DAT7	SPDIF_OUT	SPI4_MOSI	SDIO3_DAT7	SPI2_CS1_N	D4	slxd	pu
93	LCD_CS1_N	LCD2_CS1_N	SPI3_CS3_N			W0	lm0	pu[2]
93	GMI_WR_N	IDE_WR_N	NAND_WE_N	GMI_WR_N		I0	atc	pu[2]
94	VI_HSYNC			VI_HSYNC		D7	dtc	pd
95	GMI_IORDY	IDE_IRQ		GMI_IORDY		I5	atc	pu
95	GMI_WAIT	IDE_IORDY		GMI_WAIT	HSMMC_CMD	I7	atc	pu
96	VI_PCLK		SDIO2_SCLK	VI_CLK		T0	dtd	pd
97	VI_D5		SDIO2_DAT3	VI_D5		L3	dtd	pd
98	VI_D1		SDIO2_CMD	VI_D1		D5	dta	pd

X1 Pin	Tegra Pin Name	Primary Function	Alt1	Alt2	Alt3	GPIO	Group	Reset
99	LCD_WR_N	LCD1_WR_N	LCD2_WR_N	SPI3_SCK		Z3	lsc1	pu[2]
99	GMI_WR_N	IDE_WR_N	NAND_WE_N	GMI_WR_N		I0	atc	pu[2]
100	SPI1_SCK	SPI2_SCK	SPI1_SCK	SPI2_SCK	GMI_A26	X5	spie	pu
101	VI_D2		SDIO2_DAT0	VI_D2		L0	dtd	pd
102	SPI1_CS0_N	SPI2_CS0_N	SPI1_CS0_N	SPI2_CS1_N	GMI_A27	X6	spie	pu
103	VI_D3		SDIO2_DAT1	VI_D3		L1	dtd	pd
104	SPI1_MISO	SPI3_MISO	SPI1_MISO	SPI2_MISO		X7	spif	pd
105	GMI_CS4_N	IDE_A2		GMI_CS4_N		K2	atc	1
106	GMI_CS3_N	IDE_CS1		GMI_CS3_N		K4	atc	1
107	GMI_CS2_N	IDE_CS0		GMI_CS2_N		K3	atc	1
110	GPIO_PU2		UART1_CTS_N	GMI_A8		U2	gpu	z
111	UART2_RTS_N	UART1_TXD	UART2_RTS_N	GMI_A0	SPI4_MISO	J6	irrx	pu
112	GPIO_PU3	PMFM_PWM0	UART1_RTS_N	GMI_A9		U3	gpu	z
113	UART2_CTS_N	UART1_RXD	UART2_CTS_N	GMI_A1	SPI4_CS1_N	J5	irtx	pu
114	GPIO_PU4	PMFM_PWM1	UART1_DTR_N	GMI_A10		U4	gpu	z
115	UART3_TXD	UART3_TXD		GMI_A2		W6	uca	pu
116	GPIO_PU5	PMFM_PWM2	UART1_RI_N	GMI_A11		U5	gpu	z
117	UART3_RXD	UART3_RXD		GMI_A3		W7	uca	pu
118	GPIO_PU6	PMFM_PWM3	UART1_DSR_N	GMI_A12		U6	gpu	z
119	UART3_RTS_N	UART3_RTS_N	PMFM_PWM0	GMI_A4		C0	ucb	pu
120	DAP4_FS	DAP4_FS		GMI_A13		P4	dap4	pd
121	UART3_CTS_N	UART3_CTS_N		GMI_A5		A1	ucb	pu
122	DAP4_DIN	DAP4_DIN		GMI_A14		P5	dap4	pd
123	GPIO_PU0		UART1_TXD	GMI_A6		U0	gpu	z
124	DAP4_DOUT	DAP4_DOUT		GMI_A15		P6	dap4	pd
125	GPIO_PU1		UART1_RXD	GMI_A7		U1	gpu	z
126	GMI_CS0_N			GMI_CS0_N	SFLASH_CS0_N	J0	gmd	1
127	CAM_I2C_SDA	GEN3_I2C_SDA		VI_GP2		BB3	dtf	pu
128	GMI_CS1_N			GMI_CS1_N	SFLASH_CLK	J2	gmd	1
129	SPI2_CS1_N	SPI3_SCK	SPI2_CS1_N	SPI2_CS2_N	GEN1_I2C_SCL	W2	spig	pu
130	GMI_CS6_N			GMI_CS6_N		I3	ata	1
131	SPI2_CS2_N	SPI3_CS0_N	SPI2_CS2_N	SPI2_CS3_N	GEN1_I2C_SDA	W3	spih	pu
132	GMI_CS7_N			GMI_CS7_N		I6	ata	1
133	CAM_I2C_SCL	GEN3_I2C_SCL		VI_GP1		BB2	dtf	pu
134	SPI1_MOSI	SPI2_MOSI	SPI1_MOSI	SPI2_MOSI	GMI_A25	X4	spid	pd
135	SPDIF_IN	SPDIF_IN		GEN1_I2C_SDA	SDIO2_DAT3	K6	spdi	pu
135	ACC1_DETECT						usb	pu
136	SPI2_CS0_N	SPI1_CS0_N	SPI2_CS0_N	SPI3_CS1_N	GMI_A24	X3	spic	0
136	LCD_D18	LCD1_D18	LCD2_D18			M2	lhp1	0

X1 Pin	Tegra Pin Name	Primary Function	Alt1	Alt2	Alt3	GPIO	Group	Reset
137	SPDIF_OUT	SPDIF_OUT		GEN1_I2C_SCL	SDIO2_DAT2	K5	spdo	pu
137	USB1_VBUS						usb	pu
138	SPI2_SCK	SPI1_SCK	SPI2_SCK	SPI3_SCK	GMI_A23	X2	spic	0
138	LCD_D19	LCD1_D19	LCD2_D19			M3	lhp2	0
140	SPI2_MISO	SPI1_MISO	SPI2_MISO	SPI3_MISO	GMI_A22	X1	spib	pd
140	LCD_D20	LCD1_D20	LCD2_D20			M4	lvp1	pd
142	SPI2_MOSI	SPI1_MOSI	SPI2_MOSI	SPI3_MOSI	GMI_A21	X0	spia	pd
142	LCD_D21	LCD1_D21	LCD2_D21			M5	lhp0	pd
144	DAP2_DOUT	DAP2_DOUT	TWC_DO		GMI_A20	A5	dap2	pd
144	LCD_D22	LCD1_D22	LCD2_D22			M6	ldi	pd
146	DAP2_DIN	DAP2_DIN	TWC_DIN		GMI_A19	A4	dap2	pd
146	LCD_D23	LCD1_D23	LCD2_D23			M7	lpp	pd
149	GMI_AD0	IDE_D0		GMI_AD0	HSMMC_DAT1	G0	atc	pu
150	GMI_ADV_N	IDE_A0		GMI_ADV_N		K0	atc	pd
151	GMI_AD1	IDE_D1		GMI_AD1	HSMMC_DAT3	G1	atc	pu
152	OWR	OWR					owc	z
152	GMI_CLK	IDE_A1		GMI_CLK	HSMMC_CLK	K1	atc	pd
153	GMI_AD2	IDE_D2		GMI_AD2	HSMMC_DAT5	G2	atc	pu
154	LCD_PWR0	LCD1_PWR0	LCD2_PWR0	SPI3_MOSI		B2	lpw0	pu
155	GMI_AD3	IDE_D3		GMI_AD3	HSMMC_DAT7	G3	atc	pu
156	LCD_SDIN	LCD1_SDIN	LCD2_SDIN	SPI3_MISO		Z2	lsdi	pu
157	GMI_AD4	IDE_D4		GMI_AD4		G4	atc	pd
158	LCD_SDOUT	LCD1_SDOUT	LCD2_SDOUT	SPI3_MOSI		N5	lsda	pu
159	GMI_AD5	IDE_D5		GMI_AD5		G5	atc	pd
160	LCD_CS0_N	LCD1_CS0_N	LCD2_CS0_N	SPI3_CS2_N		N4	lcsn	pu
161	GMI_AD6	IDE_D6		GMI_AD6		G6	atc	pd
162	LCD_DC0	LCD1_DC0	LCD2_DC0			N6	ldc	pu
163	GMI_AD7	IDE_D7		GMI_AD7		G7	atc	pd
164	LCD_SCK	LCD1_SCK	LCD2_SCK	SPI3_SCK		Z4	lsck	pu
165	GMI_AD8	IDE_D8		GMI_AD8	HSMMC_DAT0	H0	atd	pu
166	GMI_AD24		DAP5_FS	GMI_AD24	HSMMC_DAT4	AA4	gme	z
167	GMI_AD9	IDE_D9		GMI_AD9	HSMMC_DAT2	H1	atd	pu
168	GMI_AD25		DAP5_DIN	GMI_AD25	HSMMC_DAT5	AA5	gme	z
169	GMI_AD10	IDE_D10		GMI_AD10	HSMMC_DAT4	H2	atd	pu
170	GMI_AD26		DAP5_DOUT	GMI_AD26	HSMMC_DAT6	AA6	gme	z
171	GMI_AD11	IDE_D11		GMI_AD11	HSMMC_DAT6	H3	atd	pu
172	GMI_AD27		DAP5_SCLK	GMI_AD27	HSMMC_DAT7	AA7	gme	z
173	GMI_AD12	IDE_D12		GMI_AD12		H4	ate	pu
174	DAP1_FS	DAP1_FS		GMI_D28	SDIO2_CMD	N0	dap1	pd

X1 Pin	Tegra Pin Name	Primary Function	Alt1	Alt2	Alt3	GPIO	Group	Reset
175	GMI_AD13	IDE_D13		GMI_AD13		H5	ate	pu
176	DAP1_DIN	DAP1_DIN		GMI_D29	SDIO2_DAT0	N1	dap1	pd
177	GMI_AD14	IDE_D14		GMI_AD14		H6	ate	pu
178	DAP1_DOUT	DAP1_DOUT		GMI_D30	SDIO2_DAT1	N2	dap1	pd
179	GMI_AD15	IDE_D15		GMI_AD15		H7	ate	pu
180	DAP1_SCLK	DAP1_SCLK		GMI_D31	SDIO2_SCLK	N3	dap1	pd
184	DAP2_SCLK	DAP2_SCLK	TWC_CLK		GMI_A18	A3	dap2	pd
186	DAP2_FS	DAP2_FS	TWC_CS_N		GMI_A17	A2	dap2	pd
188	DAP4_SCLK	DAP4_SCLK		GMI_A16		P7	dap4	pd
190	GMI_DPD	IDE_HDMACK	NAND_CLE	GMI_DPD	HSMMC_CMD	T7	atb	0
192	GMI_AD20	UART5_TXD	SPI3_SCK	GMI_AD20	HSMMC_DAT0	AA0	gma	z
194	GEN1_I2C_SDA	GEN1_I2C_SDA				C5	rm	pu
196	GEN1_I2C_SCL	GEN1_I2C_SCL				C4	rm	pu

This list is available as an Excel file.

1) This pin is pulled up (200kOhm). For more information about this pin see also the chapter "Recovery Mode"
2) These pins are multiplexed; please check "table 4-1 Colibri Multiplexed Pins"
3) These pins are strong pulled up (3.3kOhm). This pins can be used to change the boot device, see chapter "Bootstrap Options"

5. Interface Description

5.1 Power Signals

5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Signal Name	I/O	Description	Remarks
42, 84,108, 148,182,198, 200	3V3	I	3.3V main power supply	Use decouples capacities on all pins.
39, 41, 83, 109,147, 181, 197, 199	GND	I	Digital Ground	
40	VCC_BATT	I/O	RTC Power supply. Can be connected to a backup battery. If you use an external RTC, make sure this pin is not connected when the module is off.	This pin needs to be powered when the module is on, even if you do not use a RTC.

5.1.2 Analog Supply

Table 5-2 Analog Supply Pins

X1 Pin #	Signal Name	I/O	Description	Remarks
10, 12	AVDD_AUDIO	I	3.3V analog supply	Connect this pin in any case to a 3.3V supply. For better Audio, Touch and ADC accuracy we recommend filtering this supply separately from the digital supply.
9, 11	VSS_AUDIO	I	Analog Ground	Connect this pin in any case to GND. For better Audio, Touch and ADC accuracy we recommend filtering this supply separate from the digital supply.

5.1.3 Reset

Table 5-3 Reset Pins

X1 Pin #	Signal Name	I/O	Description	Remarks
26	nRESET_EXT	I	Reset Input	This pin is low active and resets the Colibri module. This pin is connected to the power manger IC. You need to apply the reset signal at least for 16us.
87	nRESET_OUT	O	Reset Output	This pin is low active.

5.2 GPIOs

Most of the pins have a GPIO (General Purpose Input/Output) function. All GPIO pins can be used as interrupt source.

5.2.1 Wakeup Source

Certain pins can be used to wake up the Colibri from a suspended state. There is on-chip deglitch logic, which can be de-activated if required. A signal pulse of at least 46us is recommended to wake up the system. It is possible to choose the wakeup level.

Table 5-4 Wakeup Pins

X1 Pin#	Wakeup Source	Remarks
37	WAKE13	
38	WAKE15	
43	WAKE8	Preferred Wakeup Source
45	WAKE1	Preferred Wakeup Source
49	WAKE10	
55	WAKE3	
73	WAKE5	
103	WAKE2	
116	WAKE6	
118	WAKE7	
129	WAKE12	
131	WAKE11	
135	WAKE21	
178	WAKE30	

5.3 Ethernet

The Colibri Module features a 10/100 Mbit Ethernet interface. The MAC/PHY are already on the Colibri, so you only need the magnetics on your base board.
Please check the datasheet of the Asix AX88772B Ethernet chip to learn more about the Ethernet pins.

5.4 USB

The Colibri T20 provides a USB 2.0 High Speed (480 Mbit/s) port and a USB 2.0 High Speed OTG port. The shared USB Host/Client port can also be used for the USB recovery mode, see the chapter "Recovery Mode" for more information.

5.4.1 USB Data Signal

Table 5-5 USB Data Pins

X1 Pin#	Signal Name	I/O	Description
139	USBH_P	I/O	Positive Differential Signal for USB Host port
141	USBH_N	I/O	Negative Differential Signal for USB Host port
143	USBC_P	I/O	Positive Differential Signal for the shared USB Host / Client port
145	USBC_N	I/O	Negative Differential Signal for the shared USB Host / Client port

5.4.2 USB Control Signals

Table 5-6 USB OTG Pins

X1 Pin#	Signal Name	I/O	Description
135	USB_ID	I	Use this pin to detect the ID pin if you use USB OTG
137	USBC_DET	I	Use this pin to detect if VBUS is present (5V USB supply). Please note that this pin is only 3.3V tolerant

If you use the USB Host function you need to generate the 5V USB supply voltage on your base board. The Colibri T20 provides two optional signals for the USB supply. We recommend using the following pins to guarantee the best possible compatibility, however - you can use other GPIOs or not use the signals at all.

Table 5-7 USB Power Control Pins

X1 Pin#	Signal Name	I/O	Description
131	USBH_OC	I	USB overcurrent, this pin can signal an over current condition in the USB supply
129	USBH_PEN	O	This pin enables the external USB voltage supply.

5.5 Display

The Colibri T20 has two independent display controllers. Each of the two display controllers shares access to the various output ports. There is only one instance of the parallel LCD, HDMI and TV outputs. Only one display controller can access one of these outputs at any given time. If you are using a smart display (displays with an internal frame-buffer) it is possible to use both display controllers on the parallel display interface.

Features of each display controller
- Three display windows (main frame buffer and 2 overlays)
- Hardware surface blending
- Hardware cursor
- Fully programmable display timing and resolution

5.5.1 Parallel RGB LCD interface

The Colibri T20 provides a parallel LCD interface on the SODIMM connector. It supports up to 24 bit colors per pixel.
The first 18bits are backward compatible with the existing Colibri PXAxxx family. It is also possible to use this interface for a smart display. If you use 18bit or less you can use the other bits for a smart display. However there are only a few special cases where it makes sense to use such a smart display.

Features
- Up to WSXGA+ (1680 x1050) resolution
- Up to 24 bit color
- Supports parallel TTL displays and smart displays
- Max pixel clock 120MHz

The following list details the most common color configurations.

Table 5-8 Color Configuration

X1 Pin #	Tegra Pin Name	24 bit RGB	18 bit RGB	16 bit RGB
146	LCD_D23	R1		
144	LCD_D22	R0		
142	LCD_D21	G1		
140	LCD_D20	G0		
138	LCD_D19	B1		
136	LCD_D18	B0		
61	LCD_D17	R7	R5	R4
57	LCD_D16	R6	R4	R3
64	LCD_D15	R5	R3	R2
66	LCD_D14	R4	R2	R1
54	LCD_D13	R3	R1	R0
52	LCD_D12	R2	R0	
50	LCD_D11	G7	G5	G5
74	LCD_D10	G6	G4	G4
48	LCD_D9	G5	G3	G3
62	LCD_D8	G4	G2	G2
46	LCD_D7	G3	G1	G1
80	LCD_D6	G2	G0	G0
72	LCD_D5	B7	B5	B4
78	LCD_D4	B6	B4	B3
58	LCD_D3	B5	B3	B2
60	LCD_D2	B4	B2	B1
70	LCD_D1	B3	B1	B0
76	LCD_D0	B2	B0	

Table 5-9 Additional Display

X1 Pin#	Signal Name	I/O	Description
44	LCD_DE / LCD_M1	O	Data Enable (other names: Output Enable) For Passive Displays you can use this pin as Bias/Modulation pin
56	LCD_PCLK	O	Pixel Clock (other names: Dot Clock, L_PCLK_WR)
68	LCD_HSYNC	O	Horizontal Sync (other names: Line Clock, L_LCKL_A0)
82	LCD_VSYNC	O	Vertical Sync (other names: Frame Clock, L_FCLK)

Typically you will also require some signals to control the Backlight and/or the Display Enable Signal. You can use any free GPIO for this function but we recommend using the same than we did on our standard base boards, this minimizes the required SW configurations. If would you like to use a PWM signal to control the backlight use a pin with PWM function for the Backlight Control, see also chapter 5.11.

5.5.2 HDMI

The HDMI interface is available on the X2 FFC connector on the back of the Colibri T20 module. This interface is not backwards compatible with older Colibri PXAxxx modules.

HDMI provides a unified method of transferring both video and audio data over a TMDS compatible physical link to an audio/visual display device.
Please note that the signals HDMI (TMDS) cannot be used as GPIOs.

Features
- HDMI 1.3 up to 1080p
- Supports digital sound

5.5.3 Analog VGA

The analog VGA interface is also available on the X2 FFC connector on the back of the Colibri T20 module. It supports analog VGA (analog RGB) and component TV out.

Features
- Supports NTSC, PAL or SECAM color standards.
- Supports standard definition and high definition standard.
- Supports interlaced and progressive scan standard (480i, 576i, 480p, 576p, 1080i , 720p).
- Closed Captioning
- Teletext

5.5.4 DDC (Display Data Channel)

The Colibri T20 can automatically detect the connected display over the DDC. The DDC port is 5V compatible. DDC is realized with the I2C Port 2 controller.

5.5.5 LVDS

The Colibri does not have direct a LVDS interface. However, it is very easy to use the parallel LCD port with an LVDS transmitter. Contact Toradex if you have any questions on how to connect a LVDS transmitter.

5.6 External Memory Bus

The Colibri T20 features an external memory bus. This memory bus is exclusively for your devices, there are no internal chips connected to this bus. This means you can adjust all the settings to optimize the access to your devices.
The bus can be configured as a 32 or 16bit bus. Due to compatibility reasons with our other Colibri modules we recommend using the 16bit mode. You will also lose some of the default functions if you are using the 32bit bus. The memory controller supports the programmed IO mode (PIO) or DMA transfers.

Features
- Supports 16 or 32bit bus width
- Up to 28 address bits
- Up to 8 chip selects
- Data ready signal support
- Synchronous and asynchronous access supported
- Muxed and Demux address/data mode

The memory bus is typically used to connect high speed devices like FPGAs, DSPs, additional Ethernet controllers, Wifi chips etc.

5.6.1 Non-Multiplexed Mode

In this mode the address and data signals use different pins. This mode is compatible with all our Colibri modules.

5.6.2 Multiplexed Mode

In the multiplexed mode the data signals are also used to transmit the addresses. This reduces the required number of lines to connect a device. You can use GMI_ADV_N (X1 pin 150) to separate data and addresses. If you use the 16bit mode it is only possible to transfer the lower 16 address bits over the data bus. The upper address lines are on the non-multiplexed address pins. This mode is not compatible with our Colibri PXA270 modules.

5.6.3 External Memory Map

The Colibri Tegra has two memory controllers. Both are able to address 256MB. It is possible to use any of the 8 chip selects for both memory controllers.

On the Colibri T20 the mapping of the address bit is different than on the Colibri PXAs.
In 16bit mode the external address pin A[0] correlates to the internal memory address bit 1, external address pin A[1] to internal memory address bit 2, and so on.
In 32 bit mode the external address pin A[0] correlates with the internal memory address bit 2, external address pin A[1] with internal memory address bit 3, and so on.

5.6.4 Memory Bus Signals

Table 5-10 Address and Data Pins

X1 Pin #	Compatible Function	Tegra Memory Bus Function	I/O	Description
116,114,112,110, 125,123,121,119, 117,115,113,111	Address[11:0]	GMI_A[11:0]	O	Non-Multiplexed address bits 0 to 11. They are compatible with all Colibri modules.
134,136,138,140, 142,144,146,184, 186,188,124,122, 120,118	Address[25:12] Colibri PXA270, T20, and T30 only	GMI_A[25:12]	O	Non-Multiplexed address bits 12 to 25. This pin functions are not with all Colibri Modules compatible. See the Toradex Colibri Migration Guide for more information Multiplexed Mode: In the 16bit mode the bits 16:25 are the non-multiplexed address bits.
102, 100	-	GMI_A[27:26]	O	Non- Multiplexed Address bits 26 and 27. This pin functions are not available on the Colibri PXAxx family. Multiplexed Mode: In the 16bit mode the bits 26 and 27 are the non-multiplexed address bits.
179,177,175,173, 171,169,167,165, 163,161,159,157, 155,153,151,149	Data[15:0]	GMI_AD[15:0]	I/O	Non- Multiplexed Mode: Data bits 0 to 15 Multiplexed Mode: Data/Address bits 0 to 15 The Non-Multiplexed Function is compatible with all modules GMI_AD[7:4] are with 100kOhm pulled down. GMI_AD[15:12] are with 100kOhm pulled up.
172,170,168,166, 53,51,49,192,34, 32,36,38	-	GMI_AD[27:16]	I/O	Non- Multiplexed Mode: Data bits 16 to 27 Multiplexed Mode: Data/Address bits 16 to 27 This pin functions are not compatible with the Colibri PXAxx family.
180, 178,176,174	Data[31:28]	GMI_D[31:28]	I/O	Non- Multiplexed Mode: Data bits 28 to 31 Multiplexed Mode: Data/Address bits 28 to 31

Note: Please see the table in chapter 4.4 for more information

Table 5-11 Bus Control Signals

X1 Pin #	Compatible Function	Tegra Memory Bus Function	I/O	Description
89	nWE	GMI_WR_N	O	Write Enable
91	nOW	GMI_OE_N	O	Output Enable Pulled up on the Colibri with 200 kOhm. This pin is also used for the Recovery Mode. For more information see the "Recovery Mode" chapter.
93	RDnWR	GMI_WR_N	O	The Tegra chip does not provide an RDnWR function. We routed GMI_WR_N to this pin (through a buffer). (GMI_WR_N is also available on X1 pin 89) . The GMI_WR_N provides a similar function than the RDnWR function, however the timing is a little different This pin is multiplexed with another pin, please chapter 4.1 for more information
95	RDY	GMI_WAIT GMI_IORDY	I	Wait (or Ready): Level configurable input. When asserted, WAIT (RDY) indicates the read data is invalid (Wait) or Valid (Ready). Typically used for variable latency IOs. This pin is multiplexed, please check chapter 4.1 for more information.
99	nWE	GMI_WR_N	O	Write Enable This is the same signal than on pin 89. Except that the signal passes a buffer. Use Pin 89 as tristate if backwards compatibility with the Colibri PXA270 is not required.
47,105, 106, 107, 126, 128, 130, 132	nCS and others	GMI_CSx_N	O	Chip Select Signals We recommend to use the CS signals on the pins X1 105, 106, 107 due to compatibility with our other Colibri modules. Please see the Colibri Migration Guide for more information
150	-	GMI_ADV_N	O	Address Valid This signal is used for muxed operations For synchronous read operations, the address is typically latched either on the edge active -> inactive of ADV_N or on the first rising edge of CLK after ADV_N goes active (slow devices <= 108MHz) or on the last rising edge of CLK after ADV_V goes active (faster devices >= 108MHz) For asynchronous reads, the address is latched on the edge active -> inactive of ADV_N. For writes, ADV_N is held active and the address is valid throughout the cycle for non-muxed operation. In the non-muxed case the address will be valid for the duration of the entire access. Only in the muxed modes is it valid during the ADV_N (minimum 2 cycles) This signal is with 100kOhm pulled down.
152	-	GMI_CLK	O	Clock, used to synchronize the Colibri and the device during Synchronized accesses. Rising edge active. This signal is with 100kOhm pulled down.

Note: Please see the table in chapter 4.4 for more information

5.7 IDE

The Colibri T20 supports an IDE interface. The interface shares the pins with the external memory interface.

Features:
- ATA/ATAPI-5 compliant
- PIO mode 0, 1, 2, 3, 4
- Multiword DMA mode 0, 1, 2
- Ultra DMA mode 0, 1,2,3,4
- Peak throughput of 66 MB/Sec ¡n UDMA Mode 4
- AHB Master Capability for DMA modes
- Separate timing select per drive
- Interface polarity control
- Maximum frequency of device clock is 100 MHz

The IDE interface can be used to connect a PATA hard drive.

Table 5-12 IDE Signals

X1 Pin #	Compatible Function	Tegra Memory IDE Function	I/O	Description
87	nRESET_OUT	IDE_RESET	O	Reset
47	MM_CLK	IDE_DMARQ	I	DMA Request
190	MM_CMD	IDE_HDMACK	O	DMA Acknowledge
95	RDY	IDE_IRQ	I	Drive interrupt. Cannot be used if IDE_IORDY is used.
95	RDY	IDE_IORDY	I	Input/Output Ready. Cannot be used if IDE_IRQ is used.
150		IDE_A0	O	IDE Address Bus Bit 0
152		IDE_A1	O	IDE Address Bus Bit 1
105	nCSx	IDE_A2	O	ID Address Bus Bit 2
107	nCSx	IDE_CS0	O	IDE Chip Select 0
106	nCSx	IDE_CS1	O	IDE Chip Select 1
89 /93/ 99	nWE	IDE_WR_N	O	Write strobe signal.
91	nOE	IDE_OE_N	O	Read strobe signal
179,177,175,173, 171,169,167,165, 163,161,159,157, 155,153,151,149	Data[15:0]	IDE_D[15:0]	I/O	IDE Data Lines

Note: Please see the table in chapter 4.4 for more information

5.8 I2C

The Colibri T20 offers three I2C controllers. They implement the I2C 2.1 specification. All can be used as master or slave. Port 2 is typically used for DDC and is only available on the extension connector X2 form more information see Table 3-2

Features:
- Supports standard and fast mode of operation (0-400KHz) as well as high speed mode (3.4 MHz). Note: The high speed mode of operation is not I2C 2.1 specification-compliant (requires a current source pull up to be implemented).
- Independent Master Controller and Slave Controller
- Master supports clock stretching by the slave
- Supports one to eight-byte burst data transfers
- 7-bit or 10-bit addressing
- Fully programmable 7-bit or 10-bit address for the slave
- Supports general call addressing
- Supports Recognition and Transfer of data to peripherals that do not send an acknowledge

There are a lot of low speed devices which use I2C interfaces RTCs or sensors but it is also used to configure other devices like cameras or displays.

Table 5-13 I2C Signals

X1 Pin #	Compatible Function	Tegra Pin Name	I2C Port	Description
194	I2C_SDA	GEN1_I2C_SDA	1	Tegra I2C port 1 Data (Recommended Pin for I2C)
196	I2C_SCL	GEN1_I2C_SCL	1	Tegra I2C port 1 Clock (Recommended Pin for I2C)
135		SPDIF_IN	1	Tegra I2C port 1 Data Alternative Pin Please note that this pin in multiplexed see Table 4-1 for more information
137	USBC_DET	SPDIF_OUT	1	Tegra I2C port 1 Clock Alternative Pin Please note that this pin in multiplexed see Table 4-1 for more information
131	USB_OC	SPI2_CS2_N	1	Tegra I2C port 1 Data Alternative Pin
129	USBH_PEN	SPI2_CS1_N	1	Tegra I2C port 1 Clock Alternative Pin
127		CAM_I2C_SDA	3	Tegra I2C port 3 Data
133		CAM_I2C_SCL	3	Tegra I2C port 3 Clock

5.9 UART

The Colibri Tegra provides up to five serial UART interfaces. Three of them are backward compatible with the Colibri PXAxxx modules. UART2 (provided by default on the UART_C pins) can be used as VFIR (Very Fast Infra-Red) interface.

UART Features
- Support 16450 and 16550 compatible modes
- 16 byte FIFO
- Up 4.5 Mbaud
- Word length 5 to 8 bit, optional parity, one or two stop bits
- Auto sense baud detection

VFIR Features
- Supports up to IrDA version 1.4 with 16Mbit/s
- 32bit x 16 deep FIFO

Table 5-14 UART Signals (Colibri family compatible interfaces)

X1 Pin#	Colibri Signal Name	Tegra 2 Signal Name	Tegra UART Function Name	I/O	Description
33	UART_A_RXD	SDIO1_DAT2	UART1_RXD	I	Receive Data UART_A
35	UART_A_TXD	SDIO1_DAT2	UART1_TXD	O	Transmit Data UART_A
27	UART_A_RTS	SDIO1_DAT0	UART1_RTS_N	O	Request to send UART_A
25	UART_A_CTS	SDIO1_CMD	UART1_CTS_N	I	Clear to send UART_A
23	UART_A_DTR	SDIO1_CLK	UART1_DTR_N	O	Data Terminal Ready UART_A
29	UART_A_DSR	LCD_PWR1		I	Data Set Ready UART_A
31	UART_A_DCD	LCD_PWR2		I	Carrier Detect UART_A
37	UART_A_RI	SDIO1_DAT1	UART1_RI_N	I	Ring Indicator UART_A
36	UART_B_RXD	GMI_AD17	UART4_RXD	I	Receive Data UART_B
38	UART_B_TXD	GMI_AD16	UART4_TXD	O	Transmit Data UART_B
34	UART_B_RTS	GMI_AD19	UART4_RTS_N	O	Request to send UART_B
32	UART_B_CTS	GMI_AD18	UART4_CTS_N	I	Clear to send UART_B
19	UART_C_RXD	UART2_RXD	UART2_RXD	I	Receive Data UART_C
21	UART_C_TXD	UART2_TXD	UART2_TXD	O	Transmit Data UART_C

Table 5-15 UART Signals (additional, not compatible with other modules)

X1 Pin#	Colibri Signal Name	Tegra 2 Signal Name	Tegra UART Function Name	I/O	Description
110	ADDRESS8	GPIO0_PU2	UART1_CTS_N	I	Alternate Pin: Clear to send UART_A
19	UART_C_RXD	UART2_RXD			
114	ADDRESS10	GPIO0_PU4	UART1_DTR_N	O	Alternate Pin: Data Terminal Ready UART_A
116	ADDRESS11	GPIO0_PU5	UART1_RI_N	I	Alternate Pin: Ring Indicator UART_A
112	ADDRESS9	GPIO0_PU3	UART1_RTS_N	O	Alternate Pin: Request to send UART_A
21	UART_C_TXD	UART2_TXD			
113	ADDRESS1	UART2_CTS_N	UART1_RXD	I	Alternate Pin: Receive Data UART_A
125	ADDRESS7	GPIO0_PU1			
111	ADDRESS0	UART2_RTS_N	UART1_TXD	O	Alternate Pin: Transmit Data UART_A
123	ADDRESS6	GPIO_PU0			
30	PWM<C>	SDIO3_CLK			

X1 Pin#	Colibri Signal Name	Tegra 2 Signal Name	Tegra UART Function Name	I/O	Description
113	ADDRESS1	UART2_CTS_N	UART2_CTS_N	I	Alternate. Pin: Clear to send UART_C
111	ADDRESS0	UART2_RTS_N	UART2_RTS_N	O	Alternate. Pin: Request to send UART_C
121	ADDRESS5	UART3_CTS_N	UART3_CTS_N	I	Clear to send UART_D
119	ADDRESS4	UART3_RTS_N	UART3_RTS_N	O	Request to send UART_D
117	ADDRESS3	UART3_RXD	UART3_RXD	I	Receive Data UART_D
115	ADDRESS2	UART3_TXD	UART3_TXD	O	Transmit Data UART_D
37	UART_A_RI	SDIO1_DAT1	UART5_CTS	I	Clear to send UART_E
51	MM_DAT<2>	GMI_AD22			
27	UART_A_RTS	SDIO1_DAT0	UART5_RTS	O	Request to send UART_E
53	MM_DAT<3>	GMI_AD23			
33	UART_A_RXD	SDIO1_DAT2	UART5_RXD	I	Receive Data UART_E
49	MM_DAT<1>	GMI_AD21			
192	MM_DAT<0>	GMI_AD20	UART5_TXD	O	Transmit Data UART_E
35	UART_A_TXD	SDIO1_DAT3			

5.10 SPI

The four SPI controllers operate at up to 50 Mbps. They provide full duplex, synchronous, serial communication between the Colibri module and external peripheral devices. Each SPI channel consists of four signals; clock, chip select (frame), data in and data out.

Features:
- Up to 50 Mbps
- 32bit x 32 deep FIFO
- Packet size 1-32 bit
- Packed mode with 8 or 16bit packet size
- Receive compare mode where the controller checks for a particular pattern in the incoming data stream before transferring the data to the FIFO
- Simultaneous receive and transmit

Each SPI channel supports four different modes of the SPI protocol:

Table 5-16 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	Clock is positive polarity and the data is latched on the positive edge of SCK
1	0	1	Clock is positive polarity and the data is latched on the negative edge of SCK
2	1	0	Clock is negative polarity and the data is latched on the positive edge of SCK
4	1	1	Clock is negative polarity and the data is latched on the negative edge of SCK

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some LCD displays are required to be configured over SPI prior to being driven via the RGB or LVDS interface.

Table 5-17 Backwards Compatible SPI Signals

X1 Pin #	Compatible Function	Tegra Memory SPI Function	I/O	Description
86	SSPFRM	SPI4_CS0_N	I/O	SPI Chip Select/ SPI Frame/ SPI Enable Signal
88	SSPSCLK	SPI4_SCK	I/O	SPI Clock
90	SSPRXD	SPI4_MISO	I/O	SPI Master Input / Slave Output

X1 Pin #	Compatible Function	Tegra Memory SPI Function	I/O	Description
92	SSPTXD	SPI4_MOSI	I/O	SPI Master Output / Slave Input

For a list with more SODIMM pins with SPI functions have a look at the table in chapter 4.4

5.10.1 SPI Serial Flash Controller

There is an additional SPI controller which is specifically intended for interfacing with serial EEPROM and flash memories and similar devices. For a general SPI connectivity, it is recommended that one of the four SPI controllers is used.

Features:
- Up to 50 Mbps
- 32bits x 4 deep FIFO
- Packet size 1-32 bit
- Packed mode with 8 or 16bit packet size
- Receive compare mode where the controller checks for a particular pattern in the incoming data stream before transferring the data to the FIFO
- Simultaneous receive and transmit

5.10.2 Digital Television Interface (DTV, Serial TS)

The SPI Serial Flash Interface can also be used by the DTV controller. The DTV controller converts an incoming Serial Transport Stream (Serial TS) to parallel data and stores it in the memory where you can access it via SW.

Features:
- 0-20MHz frequency of operation
- Capture of Reed-Solomon data
- SLAVE support for serial TS interface
- Minimum packet size needs to be 4 bytes

5.10.3 TWC (Three Wire Interface)

The Colibri has a three wire interface, however at this moment we recommend to use one of the four standard SPI interface instead.

5.11 PWM (Pulse Width Modulation)

The Colibri T20 features a four channel Pulse Width Modulator (PWM). The duty cycle has an 8 bit resolution (that is, it can be set to a value of between 0 and 255 in steps of 1/256). The maximum frequency output is 187.5 kHz. A 13bit divider can be used to configure the unit to run at slower frequencies.

The PWM interface can be used as an easy way to emulate a DAC and generate a variable DC voltage if used with a suitable RC circuit. Other uses include control of LED brightness, display backlights or servo motors.

The display unit and camera interface support their own PWM signals, however, these functions are not compatible with the Colibri PXAxxx family.

5.12 OWR (One Wire)

The One Wire Controller (OWR) implements a device communications bus system that provides low-speed data, signaling and power over a single signal. The OWR uses two signals for this - one for ground, and the other for power and data.
On the Colibri T20 the one wire protocol is primarily intended for communication with battery controller chips.

Features
- FIFO depth of 32 x 32 bits
- Hard-wired implementation of one wire protocol to eliminate need for external bridge chip
- 1 MHz device clock required
- Supports de-glitch
- Supports Byte transfer or 1 Bit transfer
- Supports the following commands: Read Rom, Skip Rom, Read Mem, Read Status, Read Data/Generate 8 bit CRC, Write Memory, Write Status
- Supports CRC 8/16 bit implementation
- Supports different battery devices, up to a memory size of 256KB in byte transfer

5.13 SD/MMC

The Colibri T20 has 4 SD/MMC controllers, which are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards and eMMC devices. The controllers can act as both master and slave simultaneously.
Three interfaces provide up to 8 data signals, with a fourth providing up to 4 data signals.
It is also possible to use the SD card interface as a boot device.

Features
- Supports MMC Specification Version 4.3
- Supports SD Memory Card Specification 2.0
- Supports SDIO Card Specification Version 2.0
- Supports MMC Plus, MMC Mobile and Dual-Voltage MMC Cards.
- Support of 8-bit data interlace for MMC cards
- Support SPI mode
- Up to 200Mbits per second data rate using 4 parallel data lines (SD 4-bit mode) at 50MHz
- Up to 100Mbits per second data rate using 4 parallel data lines (SDIO 4-bit mode) at 25 MHz
- Up to 4I6Mbits per second data rate using 8 bit parallel data lines (MMC 8-bit mode) at 52MHz.
- Up to 52Mbits per second data rate using 1 bit SPI mode at 52MHz.
- Supports the boot mode feature of MMC Specification 4.3 version.

T20 SDIO interface	Max Bus Width	Description
HSMMC	4bit (8bit)	Colibri Standard SD/MMC interface, additional data bits for 8bit interface available as alternate function
SDIO2	8bit	Available as alternate function, not compatible with Colibri standard
SDIO3	8bit	
SDIO0	4bit	

Table 5-18 Colibri SD/MMC Signal Pins

X1 Pin#	Colibri Signal Name	Tegra 2 Signal Name	Tegra SD/MMC Function Name	I/O	Description
190	MMC_CMD	GMI_DPD	HSMMC_CMD	I/O	Command
192	MMC_DAT0	GMI_AD20	HSMMC_DAT0	I/O	Serial Data 0
49	MMC_DAT1	GMI_AD21	HSMMC_DAT1	I/O	Serial Data 1
51	MMC_DAT2	GMI_AD22	HSMMC_DAT2	I/O	Serial Data 2
53	MMC_DAT3	GMI_AD23	HSMMC_DAT3	I/O	Serial Data 3
47	MMC_CLK	GMI_CS5_N	HSMMC_CLK	O	Serial Clock
43	WAKEUP Source-0,MMC_CD	GMI_WP_N		I	Card Detect

Table 5-19 Additional SD/MMC Signals (not compatible with other modules)

X1 Pin#	Colibri Signal Name	Tegra 2 Signal Name	Tegra SD/MMC Function Name	I/O	Description
166		GMI_AD24	HSMMC_DAT4	I/O	Serial Data 4 (only for 8bit MMC)
169	DATA10	GMI_AD10			
153	DATA2	GMI_AD2	HSMMC_DAT5	I/O	Serial Data 5 (only for 8bit MMC)
168		GMI_AD25			
170		GMI_AD26	HSMMC_DAT6	I/O	Serial Data 6 (only for 8bit MMC)
171	DATA11	GMI_AD11			
155	DATA3	GMI_AD3	HSMMC_DAT7	I/O	Serial Data 7 (only for 8bit MMC)
172		GMI_AD27			

The additional SD/MMC signals allow the SD/MMC interface to be used as an 8bit interface. The pins are not compatible with other Colibri modules, as it is not part of the Colibri module specification.

Table 5-20 Additional SD/MMC interfaces (not compatible with other modules)

X1 Pin#	Colibri Signal Name	Tegra 2 Signal Name	Tegra SD/MMC Function Name	I/O	Description
180		DAP1_SCLK	SDIO2_SCLK	O	SDIO2: Serial Clock
96	CIF_PCLK	VI_PCLK			
174		DAP1_FS	SDIO2_CMD	I/O	SDIO2: Command
98	CIF_DD<1>	VI_D1			
101	CIF_DD<2>	VI_D2	SDIO2_DAT0	I/O	SDIO2: Serial Data 0
176		DAP1_DIN			
103	CIF_DD<3>	VI_D3	SDIO2_DAT1	I/O	SDIO2: Serial Data 1
178		DAP1_DOUT			
137	USBC_DET (USB cable detect GPIO)	USB1_VBUS, SPDIF_OUT	SDIO2_DAT2	I/O	SDIO2: Serial Data 2
79	CIF_DD<4>	VI_D4			
135		ACC1_DETECT, SPDIF_IN	SDIO2_DAT3	I/O	SDIO2: Serial Data 3 (Hardware multiplexed pin)
97	CIF_DD<5>	VI_D5			
67	PWM<D>, CIF_DD<6>	SDIO3_CMD, VI_D6	SDIO2_DAT4	I/O	SDIO2: Serial Data 4 (Hardware multiplexed pin)
59	PWM<A>, CIF_DD<7>	SDIO3_DATA3, VI_D7	SDIO2_DAT5	I/O	SDIO2: Serial Data 5
85	CIF_DD<8>	VI_D8	SDIO2_DAT6	I/O	SDIO2: Serial Data 6

X1 Pin#	Colibri Signal Name	Tegra 2 Signal Name	Tegra SD/MMC Function Name	I/O	Description
65	CIF_DD<9>, SDA2 (PS2 Mouse GPIO)	VI_D9	SDIO2_DAT7	I/O	SDIO2: Serial Data 7
30	PWM<C>	SDIO3_CLK	SDIO3_CLK	O	SDIO3: Serial Clock
67	PWM<D>, CIF_DD<6>	SDIO3_CMD, VI_D6	SDIO3_CMD	I/O	SDIO3: Command
63	SCL1 (PS2 Mouse GPIO)	SDIO3_DAT0	SDIO3_DAT0	I/O	SDIO3: Serial Data 0
55	SDA1 (PS2 Mouse GPIO)	SDIO3_DAT1	SDIO3_DAT1	I/O	SDIO3: Serial Data 1
28	PWM<B>	SDIO3_DAT2	SDIO3_DAT2	I/O	SDIO3: Serial Data 2
59	PWM<A>, CIF_DD<7>	SDIO3_DATA3, VI_D7	SDIO3_DAT3	I/O	SDIO3: Serial Data 3 (Hardware multiplexed pin)
90	SSPRXD	SDIO3_DAT4	SDIO3_DAT4	I/O	SDIO3: Serial Data 4
88	SSPSCLK	SDIO3_DAT5	SDIO3_DAT5	I/O	SDIO3: Serial Data 5
86	SSPFRM	SDIO3_DAT6	SDIO3_DAT6	I/O	SDIO3: Serial Data 6
92	SSPTXD	SDIO3_DAT7	SDIO3_DAT7	I/O	SDIO3: Serial Data 7
23	UART_A_DTR	SDIO1_CLK	SDIO1_CLK	O	SDIO0: Serial Clock
25	UART_A_CTS	SDIO1_CMD	SDIO1_CMD	I/O	SDIO0: Command
27	UART_A_RTS	SDIO1_DAT0	SDIO1_DAT0	I/O	SDIO0: Serial Data 0
37	UART_A_RI	SDIO1_DAT1	SDIO1_DAT1	I/O	SDIO0: Serial Data 1
33	UART_A_RXD	SDIO1_DAT2	SDIO1_DAT2	I/O	SDIO0: Serial Data 2
35	UART_A_TXD	SDIO1_DAT3	SDIO1_DAT3	I/O	SDIO0: Serial Data 3

5.14 Analog Audio

On the Colibri T20 is a Wolfson WM9715 chip which handles the audio interface. You can consult the Wolfson WM9715 datasheet for more information.

Table 5-21 Audio Interface Pins

X1 Pin #	Signal Name	I/O	Description	Pin on the WM9715
1	MIC_IN	Analogue Input	Microphone input	21
3	MIC_GND	Analogue Input	Microphone pseudo-ground	(28)
5	LINEIN_L	Analogue Input	Left Line Input	23
7	LINEIN_R	Analogue Input	Right Line Input	24
13	HEADPHONE_GND	Analogue Output	Headphone pseudo-ground	37
15	HEADPHONE_L	Analogue Output	Headphone Left Output	39
17	HEADPHONE_R	Analogue Output	Headphone Right Output	41

5.16 Touch Panel Interface

The Wolfson WM9715 IC provides the touch interface. Please consult the Wolfson WM9715 documentation for more information.

Table 5-22 Touch Interface Pins

X1 Pin #	Signal Name	I/O	Description	Pin on the WM9715
14	TSPX	Analogue Input	X+ (4-wire) / Bottom right (5-wire)	14
16	TSMX	Analogue Input	X- (4-wire) / Top left (5-wire)	16
18	TSPY	Analogue Input	Y+ (4-wire) / Top right (5-wire)	15
20	TSMY	Analogue Input	Y- (4-wire) / Bottom left (5-wire)	17
2	AD3	Analogue Input	Wiper (5-wire) also used as ADC input. (See Analog Inputs)	12

5.17 Analog Inputs

The Wolfson WM9715 IC provides the 4 analogue input channels. Please consult the Wolfson WM9715 documentation for more information.

Table 5-23 Analog Inputs Pins

X1 Pin #	Signal Name	I/O	Description	Pin on the WM9715
2	AD3	Analogue Input	ADC input (3.3V max). This pin is also used in the 5-wire interface, see Touch Panel interface.	12
4	AD2	Analogue Input	ADC input (5V max)	31
6	AD1	Analogue Input	ADC input (3.3V max)	30
8	AD0	Analogue Input	ADC input (3.3V max)	29

5.18 Camera Interface

The Video Capture and Imaging Subsystem (VI) can receive data from TV decoder chips, CMOS sensors and other devices. It supports advanced processing features with its multi-stage pipeline, from lens correction through to color space conversion.
Among other functions, this subsystem removes common artifacts of digital CMOS image sensors and lenses from the raw data, and interpolates alternating, one-color-per-pixel Bayer-formatted data into full RGB color signals.

Features
- Raw (Bayer), RGB, YUV input up to 12 Megapixels
- 8/10/12bit parallel video interface
- ITU-R 8bit
- Max pixel clock input 120 MHz
- Max Master clock output (Camera input clock) 80MHz

Table 5-24 Camera Interface Pins

X1 Pin #	Compatible Function	Tegra Pin Name	I/O	Description
75	CIF_MCLK	VI_MCLK	O	Master Clock: Connect to Reference clock input on camera(s)
96	CIF_PCLK	VI_PCLK	I	Pixel Clock: Connect to Pixel CLK output on camera(s)
81	CIF_FV	VI_VSYNC	I	Vertical Sync: Connect to Vsync on camera(s)
94	CIF_LV	VI_HSYNC	I	Horizontal Sync: Connect to Hsync on camera(s)
	CIF_DD[9:0]	VI_D[9:0]	I	Pixel Data bits 0 -9: Connect to Data pins on camera(s).
69	SCL2 (PS2 Keyboard GPIO)	VI_D10	I	Pixel Data bit 10: Connect to a Data pin on camera(s). This data bit is NOT compatible with the complete Colibri family
77	-	VI_D11	I	Pixel Data bit 11: Connect to a Data pin on camera(s). This data bit is NOT compatible with the complete Colibri family

Table 5-25 Camera to Colibri Pin Mapping

Format	Camera Pins	Colibri Pin
YUV	D[7:0]	CIF_DD[9:2]
Bayer 8-bit	D[7:0]	CIF_DD[9:2], connect CIF_DD[1:0] with GND
Bayer 10-bit	D[9:0]	CIF_DD[9:0]

5.19 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of the serial audio digital interface format. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard. This controller is also used for the audio HDMI output.

Features
- Supports 5 data formats
        - 16-bit
        - 20-bit
        - 24-bit
        - Raw
        - 16-bit packed

- Supports "autolock" mode to automatically detect "spdifin" sample rate and lock onto the data stream.
- Supports override mode to provide a manual control to sample "spdifin" data stream.
- Maximum device clock of 50 MHz

5.20 AC97/I2S

The NVIDIA Tegra chip has 3 Audio Controllers (two I2S and a single AC97). On the Colibri T20, 4 of the 5 audio ports (DAP) are available. One (DAP3) is used internally for the onboard AC97 codec. With the Digital Audio Switch it is possible to connect the internal Audio Controllers (DAC) with the DAPs in many different configurations.
The audio interface is a new feature and is not backwards compatible with the PXAxxx based Colibri modules.

5.20.1 AC97

This Audio Controller is normally used for the onboard AC97 codec. However, it is possible to connect it via the Digital Audio Switch with one of the alternative audio ports.

Features
- AC97 V2.3 compliant
- Supports double Data Rate playback

5.20.2 I2S

The I2S can be used to connect an additional external audio codec.

Features
- PCM, Network and TDM mode Support
- Master or Slave
- Supports I2S, RJM, LJM and DSP mode data formats
- Maximum device clock of 24 MHz

5.21 Clock Output

The Colibri T20 provides an external Clock on SODIMM (X1) Pin 75.
It can be selected to run in either PLL P or PLL C mode.
PLLP_OUT2: 48MHz
PLLP_OUT3: 72MHz
PLLC_OUT1: general purpose PLL frequency lower or equal 600 MHz

Care must be taken when changing PLL frequencies; these PLLs are also used internally in the Tegra processor.

5.22 Keypad

You can use any free GPIOs to realise a Matrix keypad interface.

5.23 JTAG

There is a JTAG interface available.

6. Recovery Mode

The shared USB Client/Host port can be used to download new software. This is normally only required if the Bootloader does not boot anymore.

To enter the recovery mode, either connect the recovery mode pads on the front of the module together (see picture below) or pull SODIMM pin 91 to GND with a 10KOhm resistor while booting.
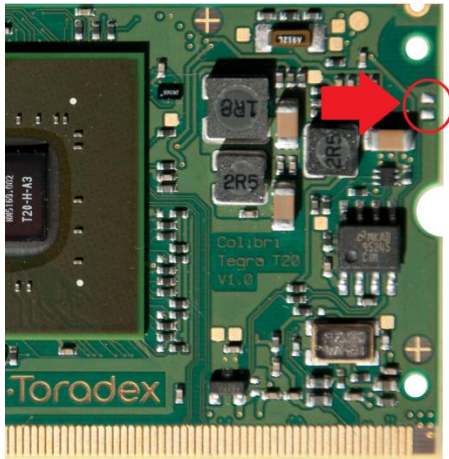

Figure 5 Force Recovery Pins Colibri T20 V1.0a

When the module is in recovery mode, the NVFlash tool can be used to re-program the module.

You find additional information in our Developer Center: http://www.developer.toradex.com

7. Bootstrap Options

By default the Colibri T20 will boot from the internal Flash Memory.
You have the option to change this setting and boot directly from an SD card. For example this could be useful if the system doesn't boot anymore from the internal Flash Memory. You need to format the SD Card with a special tool to use it as a boot device.

To change the boot device you need to use the following boot strap pins. If you like to minimize power consumption you can activate the pull down resistors only at boot time.

Table 7-1 Bootstrap Options

X1 Pin #	Status	Boot Device	Comment
173, 175, 177, 179	All open or pulled high	Internal Flash	This pins are internally pulled up with 3.3kOhm
173, 175, 177, 179	All pulled low with 680 Ohm	MMC/SD Card	This pins are internally pulled up with 3.3kOhm

8. Suspend

In the suspend state the CPU is powered off but the RAM is still powered. It is very fast to wake up form this state.
You can use several pins as Wakeup Sources, see chapter 5.2.1 for more information about possible wakeup sources.

The GPIO pins have keeper circuits that maintain the output level of the pads during Suspend.
If a specific level is needed during suspend state other than what the pad is already driving, the pad can be configured as a GPIO to drive out the desired level. This includes setting the outputs to drive high/low or Tristate.

The internal pull up/down control is deactivated in the suspend state except for the following pins:

X1 Pin#	Remarks
23	
25	
27	
28	
30	
33	
35	
37	
55	
59	Multiplexed pin
63	
67	Multiplexed pin
86	
88	
90	
92	
137	Multiplexed pin

9. Known Issues

TBD

10. Technical Specifications

10.1 Absolute Maximum Rating

Table 10-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_VCC_BATT	RTC Supply	−0.3	3.6	V
Vmax_IO	Most pins with GPIO functions	-0.5	3.63	V
Vmax_3V3	Digital Supply	-0.3	3.63	V
Vmax_AVDD	Analog Supply	-0.3	3.63	V
Vmax_USB	USB Voltage	-0.5	6.0	V

10.2 Electrical Characteristics

Table 10-2 Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
V_VDD	Power Supply Operating Voltage	3.135	3.3	3.465	V
V_AVDD	Analog Power Supply	3.0	3.3	3.60	V
VIH_DDC	HDMI and DDC Input High Voltage	0.75 * V_VDD		5.3	V
VIL_DDC	HDMI and DDC Input Low Voltage	-0.5		0.25*V_VDD	V
VIH_OWR	One Wire Input High Voltage	1.35		0.5+V_VDD	V
VIL_OWR	One Wire Input Low Voltage	-0.5		0.45	V
VIH_IO	Digital Input High Voltage	0.75 * V_VDD		0.5+V_VDD	V
VIL_IO	Digital Input Low Voltage	-0.5		0.25*V_VDD	V
VOH_IO	Digital Output High Voltage	0.85*V_VDD			V
VOL_IO	Digital Output Low Voltage			0.15*VDD	V
IIN_IO	Input Leakage Current if no pull-up or pull-down are active.	-1		1	uA
VIL_nRESET_EXT	Reset In Low Voltage (min. 16uS low)			0.4	V
VCC_BATT	RTC Supply	1.7	3.3	3.6	V

Table 10-3 Typical Power Consumption

Symbol	Description (VCC=3.3V, Colibri T20 V1.2a , HDMI + LCD active)	Typ	Unit
IDD_IDL256	CPU Idle (res 640x480, Colibri T20 256MB)	332	mA
IDD_IDL512	CPU Idle (res 640x480, Colibri T20 512MB)	414	mA
IDD_HIGHCPU256	High Load (1080p, 2 core 100%, 3D demo, 1080p movie form USB 2.0)	812	mA
IDD_HIGHCPU512	High Load (1080p, 2 core 100%, 3D demo, 1080p movie form USB 2.0)	822	mA
IDD_HD256	Full HD Video from USB 2.0 Memory Stick	377	mA
IDD_SUSPEND256	Module in Suspend State	TBD	mA
IDD_SUSPEND512	Module in Suspend State	TBD	mA

10.3 Power Up Ramp Time Requirements

TBD

10.4 Mechanical Characteristics

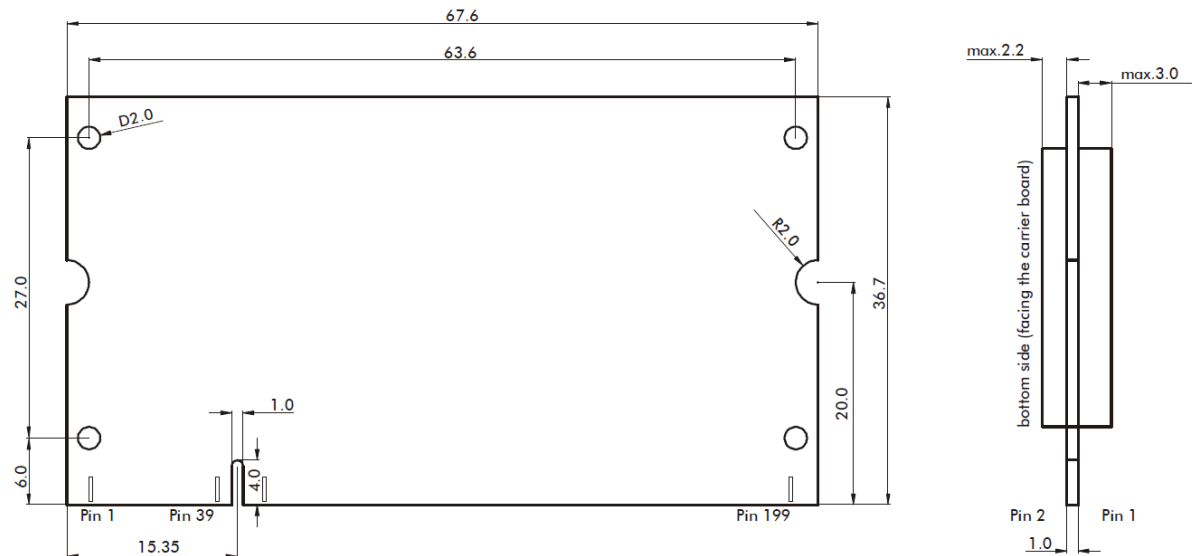Figure 6 Mechanical dimensions of the Colibri modules
Tolerance for all measures: +/- 0.1mm

10.4.1 Sockets for the Colibri Modules

The Colibri modules fit into a regular 2.5V (DDR1) SODIMM200 memory socket.
A choice of SODIMM200 socket manufacturers is given below:

AUK Connectors:	http://www.aukconnector.com/
CONCRAFT:	http://www.concraft.com.tw/connector_products.html
Morethanall Co Ltd.:	http://www.morethanall.com/
Tyco Electronics (AMP):	http://www.te.com/usa-en/home.html
NEXUS COMPONENTS GmbH	https://www.nexus-de.com/en

10.5 Thermal Specification

The Colibri T20 is available in 2 temperature ranges, consumer and industrial temperature range (IT).

Table 10-4 1.1 Thermal Specification

Module	Description	Min	Typ	Max	Unit
Colibri T20	Operating temperature range (ambient)	0		70	°C
Colibri T20 IT	Operating temperature range (ambient)	-40		85	°C
Colibri T20/ Colibri T20 IT	Storage Temperature	-40		85	°C
Colibri T20	Operation temperature as sensed form Thermal Diode (CPU)			90	°C
Colibri T20 IT	Operation temperature as sensed form Thermal Diode (CPU)			105	°C
Colibri T20	Thermal Design Power at max Temperature Tegra Chip and DDR RAM only[2]		3.0		W
Colibri T20/ Colibri T20 IT	Thermal Resistance Junction-to-Ambient, Tegra Chip only. (Theta-JA) [1]		18.7		°C/W
Colibri T20/ Colibri T20 IT	Thermal Resistance Junction-to-Case, Tegra Chip only. (Theta-JC) [1]		3.21		°C/W
Colibri T20/ Colibri T20 IT	Thermal Resistance Junction-to-Top of Package, Tegra Chip only, (Psi-JT) [1]		2.2		°C/W

[1] A High K JEDEC Board as defined by JEDEC Standard JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements, was used for thermal modeling to determine thermal performance.
[2] Thermal Design Power is the power dissipation for use in thermal design considering high-compute applications. Thermal Design Power is not the theoretical maximum power the device can generate

10.6 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at: http://www.toradex.com/support/product-compliance

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