Wasca memory maps v. 0.2

This is a short document describing wasca cartridge memory and registers map from both SH-2 and in-FPGA Nios II soft cpu perspective.

Part 1. SH-2 memory map

All the addresses in this part of the document are in SH-2 cache-through address space unless otherwise specified.
Table 1 describes differencies between SH-2's chipselect spaces and A-bus (SMPC's chipselects). Further chipselect references will be using A-Bus ranges.

Address range	Size	SH-2 chipselects	A-Bus Chipselects	wasca usage
0x22000000 - 0x23FFFFFF	32 MB	CS0	CS0	Yes
0x24000000 - 0x24FFFFFF	16 MB	CS1	CS1	Yes
0x25000000 - 0x257FFFFF	8 MB		Dummy	No
0x25800000 - 0x258FFFFF	1 MB		CS2	Not yet

Table 1-1. SH-2 and A-bus chipselect ranges.

Table 2 shows a detailed map for CS0 and CS1:

Address range	Size	CS	Power memory usage	RAM cart usage	ROM usage	wasca usage	
0x22000000 - 0x221FFFFF	2 MB	CS0			Data	First stage boot loader	ROM / BootROM emulation
0x22000000 - 0x223FFFFF	2 MB						
0x22400000 - 0x225FFFFF	2 MB			Lower data		RAM emulation	
0x22600000 - 0x227FFFFF	2 MB			Upper data			
0x22800000 - 0x23FEFFFF	11.94 MB						
0x23FF0000 – 0x23FF0FFF	4KB					SD card interface	
0x23FF1000 – 0x23FFEFFF	56KB					Reserved	
0x23FFF000 – 0x23FFFFFF	4KB					wasca system area	

0x24000000 – 0x24FEFFFF	15.999 9 MB	CS1	Data			Power memory emulation	
0x24FFFFFC	4B		ID	ID	ID	ID	

Table 1-2. Detailed CS0 and CS1 memory maps.

SD card interface registers are shown in the table 3.

Address range	Size	R/W	Name	Description
0x23FF0000 – 0x23FF01FF	512B	R/W	SD card buffer	Data buffer for incoming and outgoing data
0x23FF0200 – 0x23FF020F	16B	R	CID	Card Identification Number Register
0x23FF0210 – 0x23FF021F	16B	R	CSD	Card Specific Data Register
0x23FF0220	4B	R	OCR	Operation Condition Register
0x23FF0224	4B	R	SR	SD Card Status Register
0x23FF0228	2B	R	RC	Relative Card Address Register
0x23FF022C	4B	R/W	CMD_ARG	Command Argument Register
0x23FF0230	2B	R/W	CMD	Command Register
0x23FF0234	2B	R	ASR	Auxiliary Status Register
0x23FF0238	2B	R	RR1	Response R1
0x23FF0FFE	2B	R/W	WSSCR	wasca Specific SD Control Register

Table 1-3. SD card interface registers.

Table 4 holds the same for wasca system area. System wasca registers are 16-bit-wide and should be accessed with 16-bit accesses and 16-bit address align. Other access sizes and/or unaligned addresses will lead to unpredictable behavior.

Address range	Size	R/W	Name	Description
0x23FFF000 - 0x23FFFFEF	4080B		Reserved	
0x23FFFFF0	2B	R	PCNTR	Wasca Prepare counter. Reset value is 0, after writing a valid value to MODE, this counter shows value (in percents) of the prepare progress. When this register has value of 0x0064, wasca is ready to emulate specified cart. Higher values should not appear normally.
0x23FFFFF2	2B	R	STATUS	Wasca Status register. Error and flag bits appears here. Bit 0 – SD card error when 1 Bit 1 – SDRAM test failed when 1

				Bit 2 – USB transfer error when 1 Other bits are reserved
0x23FFFFF4	2B	R/W	MODE	wasca Mode Register Divided into 4 octets, non-zero octet selects cart type, octet value selects card subtype. See table 5 for additional description. Setting values not provided in table 5 results in unpredictable behavior.
0x23FFFFF6	2B	R	HWVER	wasca hardware version, major and minor 0x050C = v5.12
0x23FFFFF8	2B	R	SWVER	wasca embedded software version, major and minor (same format as HWVER) This register is zero at reset, and is written by Nios soft CPU right after boot. If by the time SH-2 is running the bootcode this value is still zero, it means Nios fault. SH-2 cannot alter this register.
0x23FFFFFA- 0x23FFFFFF	6B	R	SIGNATURE	Signature: “wasca “ in ASCII (0x7761 0x7363 0x6120)

Table 1-4. Wasca system area registers.

Okay, and now the promised wasca modes table:

MODE value	Description
0x0000	INIT
0x0001	Power memory, 0.5 MB
0x0002	Power memory, 1 MB
0x0003	Power memory, 2 MB
0x0004	Power memory, 4 MB
0x0010	RAM expansion, 1 MB
0x0020	RAM expansion, 4 MB
0x0100	ROM, KoF95.bin
0x0200	ROM, Ultraman.bin
Other values	Unpredictable

Table 1-5. Valid wasca MODE register values.

Part 2. Nios II memory map

Nios II address range is FPGA-dependent (will be different for different FPGA parts) and is still work in progress, so it might change occasionally. Please check the last wasca FPGA project from repository for the valid memory map. Table 2-1 shows a memory map for Nios II soft cpu.

Address range	Size	Description
0x00000000 - 0x0002AFFF	172 KB	On-chip flash. It stores both Nios II software and SH-2 bootcode (compiled into Nios II software as binary).
0x00040000 — 0x0040001F	32 B	UART registers
0x00041000 — 0x000417FF	2 KB	Debug RAM
0x00042000 — 0x0004200F	16 B	PLL setup
0x00043000 — 0x000433FF	1 KB	SD card interface
0x00044000 — 0x0004400F	16 B	Reserved
0x00045000 — 0x000451FF	512 B	wasca system registers
0x00080000 — 0x000827FF	10K	RAM

Table 2-1. Nios II memory map.

The scope of this document does not cover Nios II peripheral description, but it is well covered in Altera docs. The only custom core in Nios II memory map is wasca system registers interface, and its content is shown in table 2-2.

Address range	Size	R/W	Name	Description
0x00045000 - 0x00045FEF	4080B		Reserved	
0x00045FF0	2B	R/W	PCNTR	Wasca Prepare counter. After sensing a non-zero value in MODE register Nios should start the preparement process, and write the progress periodically into this value (in percents).
0x00045FF2	2B	R/W	STATUS	Wasca Status register. Nios should write status here. See corresponding register in SH-2 memory map.
0x00045FF4	2B	R	MODE	wasca Mode Register Nios should scan this register while in INIT mode, and switch to corresponding mode when it changes. See corresponding register in SH-2 memory map.

0x00045FF6	2B	R	HWVER	wasca hardware version, major and minor 0x050C = v5.12
0x00045FF8	2B	R/W	SWVER	This register is zero at reset, and is written by Nios soft CPU right after boot. See corresponding register in SH-2 memory map.
0x00045FFA- 0x00045FFF	6B		Reserved	

Table 2-2. wasca system area from Nios II perspective.