Electrical-, protocol- and application layer validation of MIPI D-PHY and M-PHY designs

Roland Scherzinger

MIPI Application Expert
Digital Test Division
Agilent Technologies

Agenda

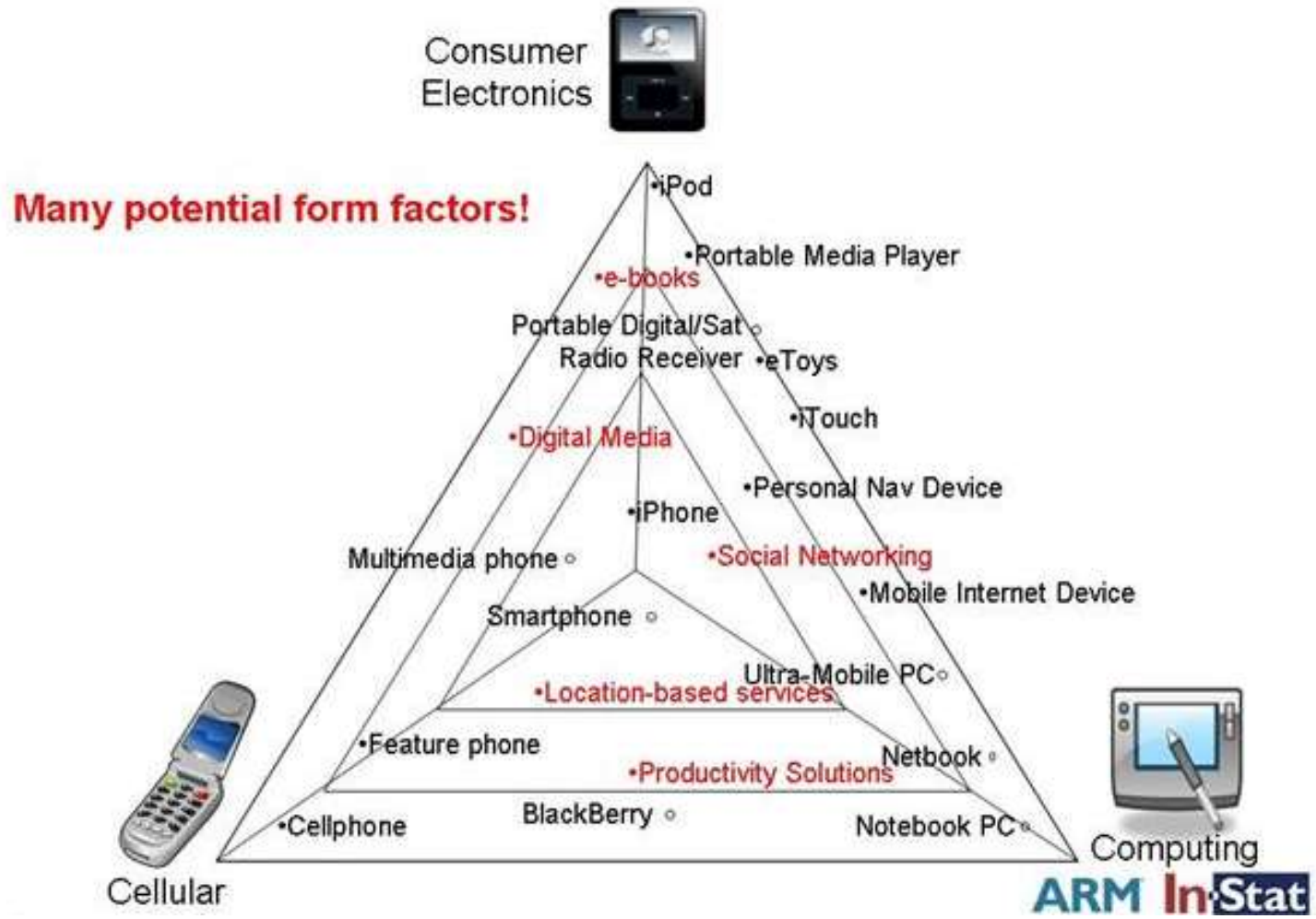
Introduction, Smart Device Overview

MIPI Interfaces in Smart Devices

Validating MIPI Interfaces

Outlook

Smart Devices Overview



Features of Smart Devices

Internet, eMail, Organizer, Phone

- Wireless (WLAN, UMTS, LTE, ...)

Imaging, Photo, Video, Movies

- High resolution Camera and Display

Audio, Music

- MP3, WMA, AAC, …

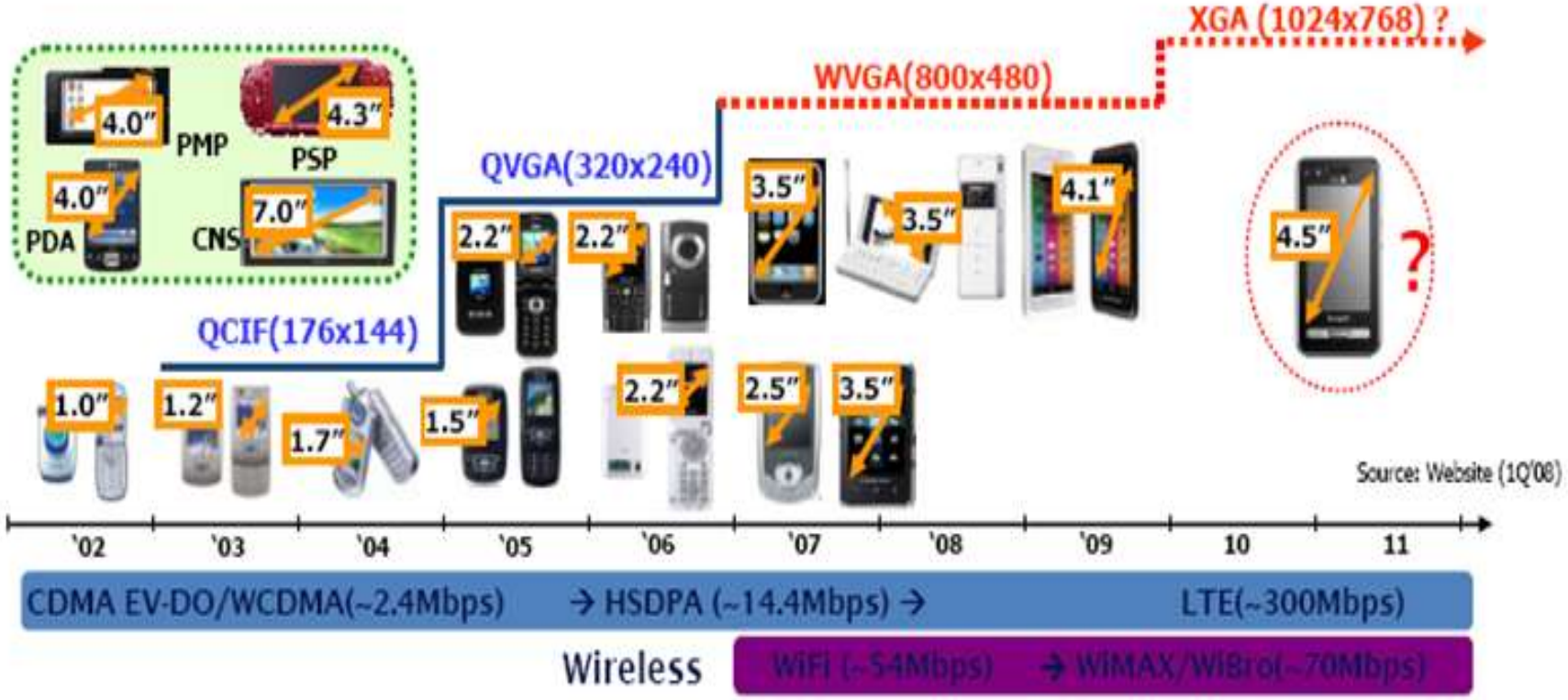
Maps

- GPS, aGPS

Book Reading

Gaming

Mobile (Smart) Device Evolution



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- **MIPI Overview**
- D-PHY Overview
- M-PHY Overview

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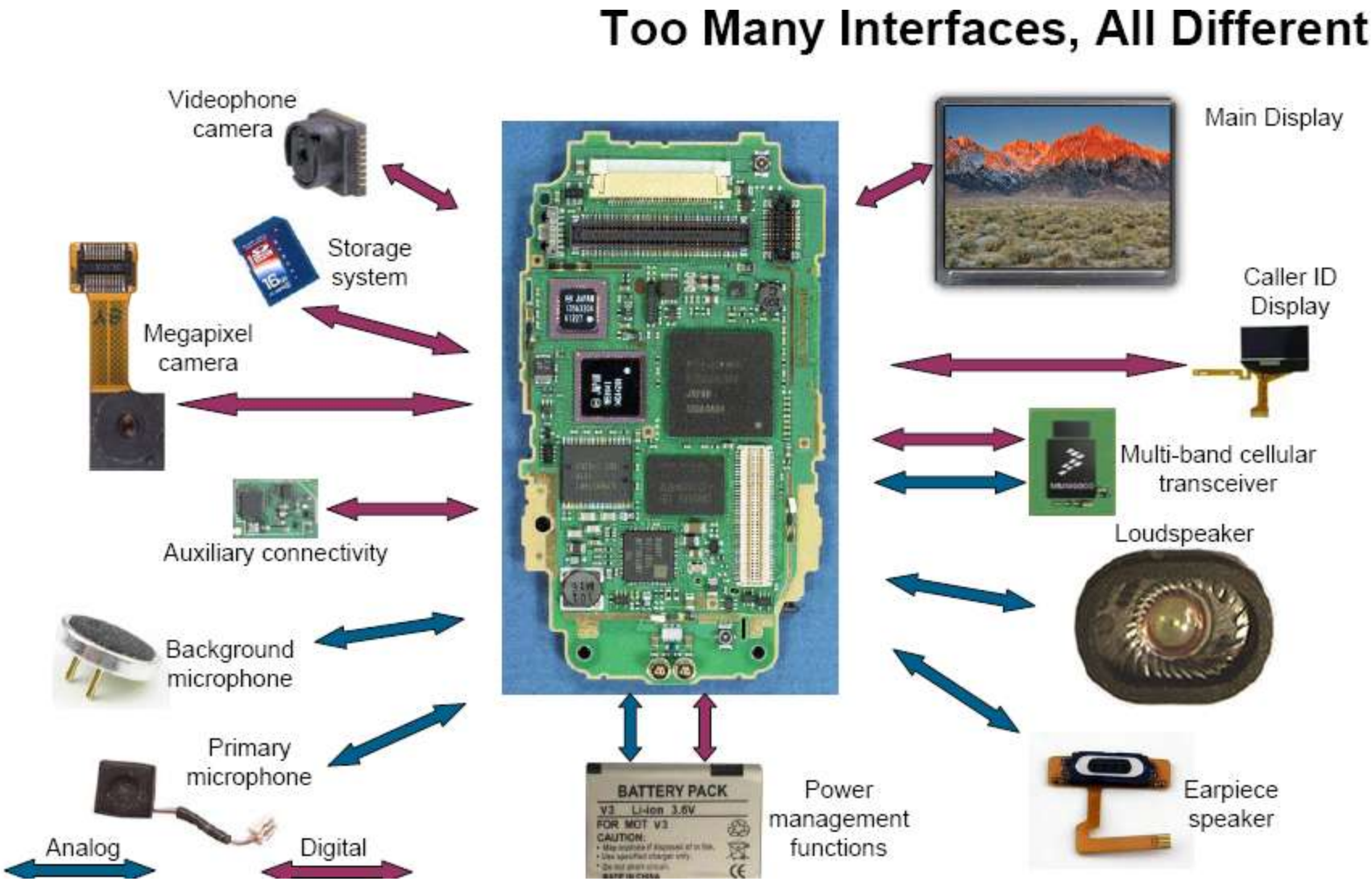
Technology Challenges in Mobile Computing



MIPI Interfaces in a Mobile Platform

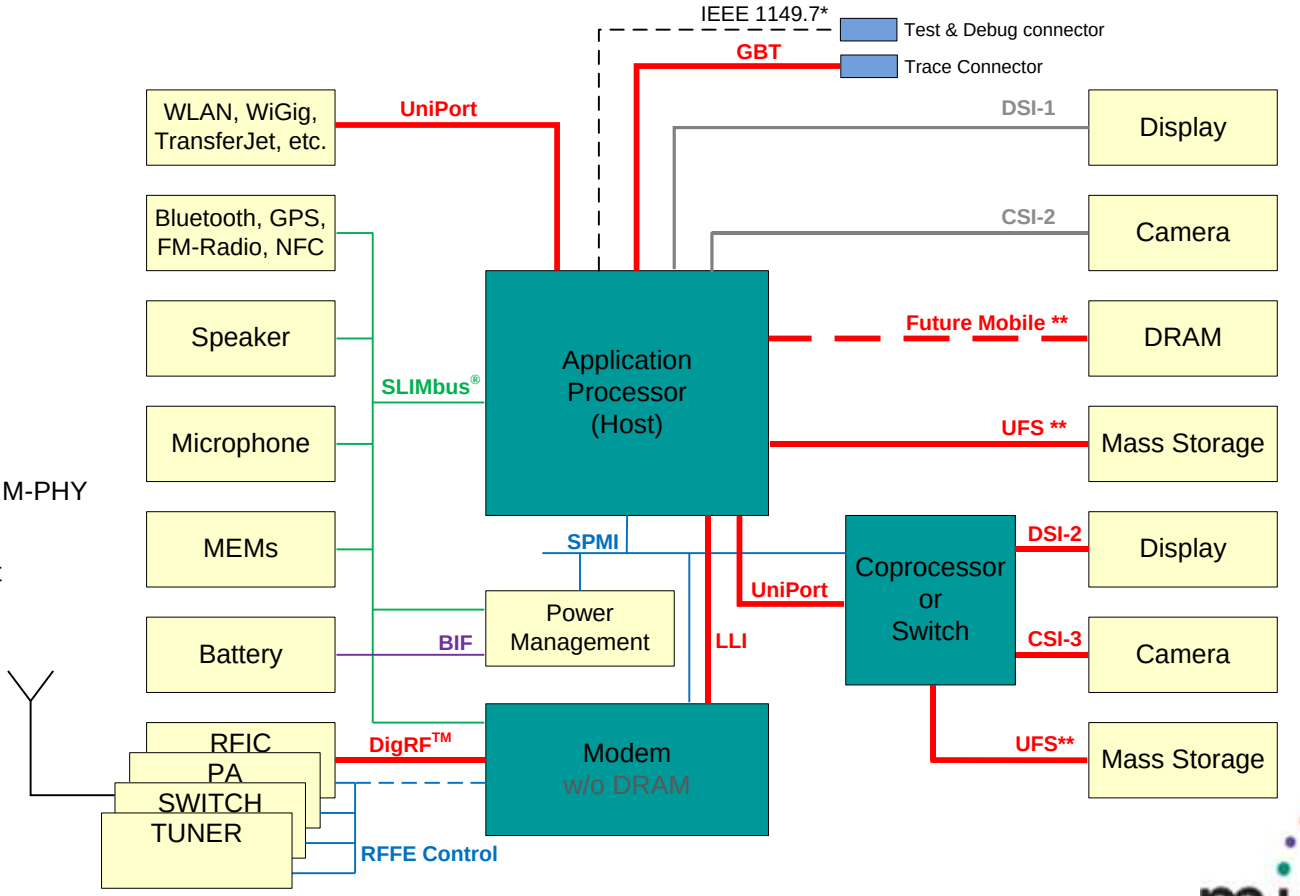
This picture is only an illustrative example for several ways of integration with the purpose of demonstrating MIPI diversity on interfaces

- D-PHY based
- M-PHY based
- SLIMbus
- SPMI/RFFE

UniPort : UniPro™ + D-PHY or M-PHY

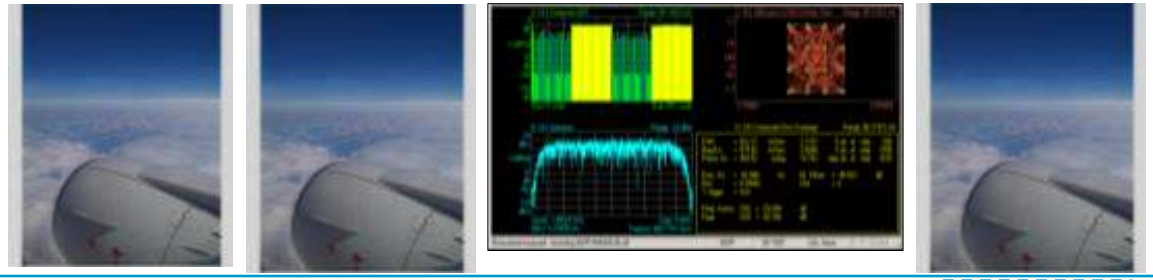
UniPro based IF technology are:
UFS, CSI-3, DSI-2, GBT, UniPort

(*) Transferred to IEEE
(**) Liaison with JEDEC



Physical / Protocol / Application Support

MIPI
Mobile industry
processor Interface



Application

Protocol Standard

CSI camera Interface

DSI Display Interface

DigRF v3

DigRF v4

Next Gen CSI / DSI

UFS

Unipro

LLI

Physical Standard

D-PHY

M-PHY

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- **D-PHY Overview**
- M-PHY Overview

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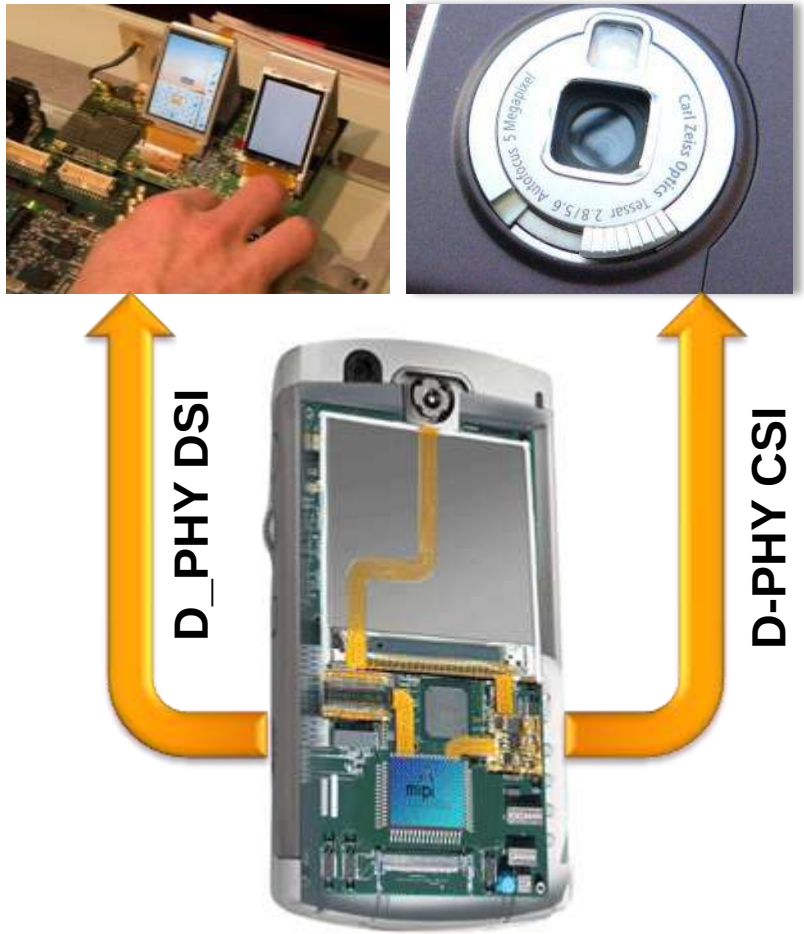
What is MIPI D-PHY ?

MIPI D-PHY is a Serial Bus

- Mobile Display
- Mobile Camera
- Mobile Controller



Why use MIPI D-PHY ?

Standard Bus: Facilitates Integration and Interoperability

Performance: up to 4Gbs for high resolution camera and displays

Low power and high Scalability: Multilane architecture

MIPI D-PHY Characteristics

Data Lanes

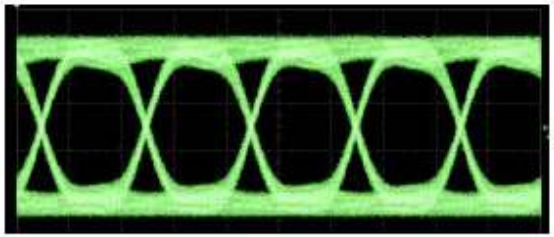
- High Speed Mode 80Mbps -1Gbps
- May go up to 1.5 Gbps in the future
- Low Power Mode < 10Mbps
- Bidirectional

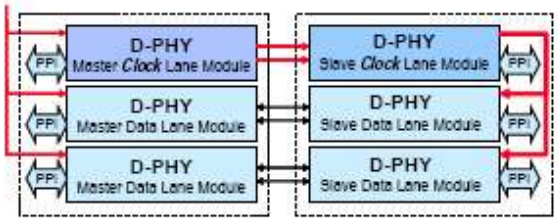
Lane Scalability

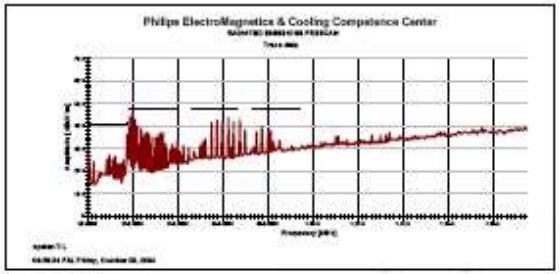
- Up to 4 Lanes + 1 clock lane

Power

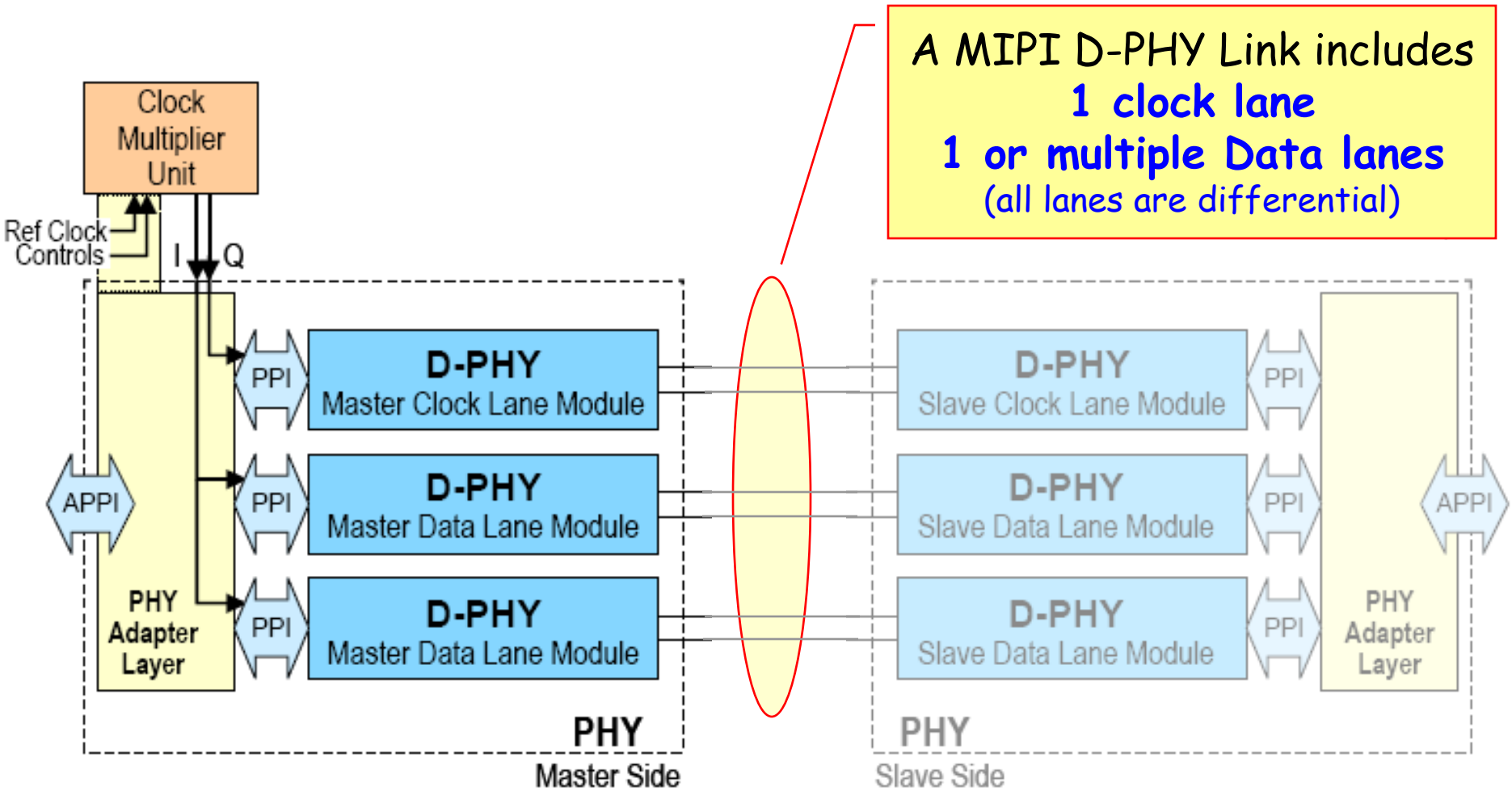
- Low Operational power
- Very Low Standby power







Anatomy of a MIPI D-PHY link



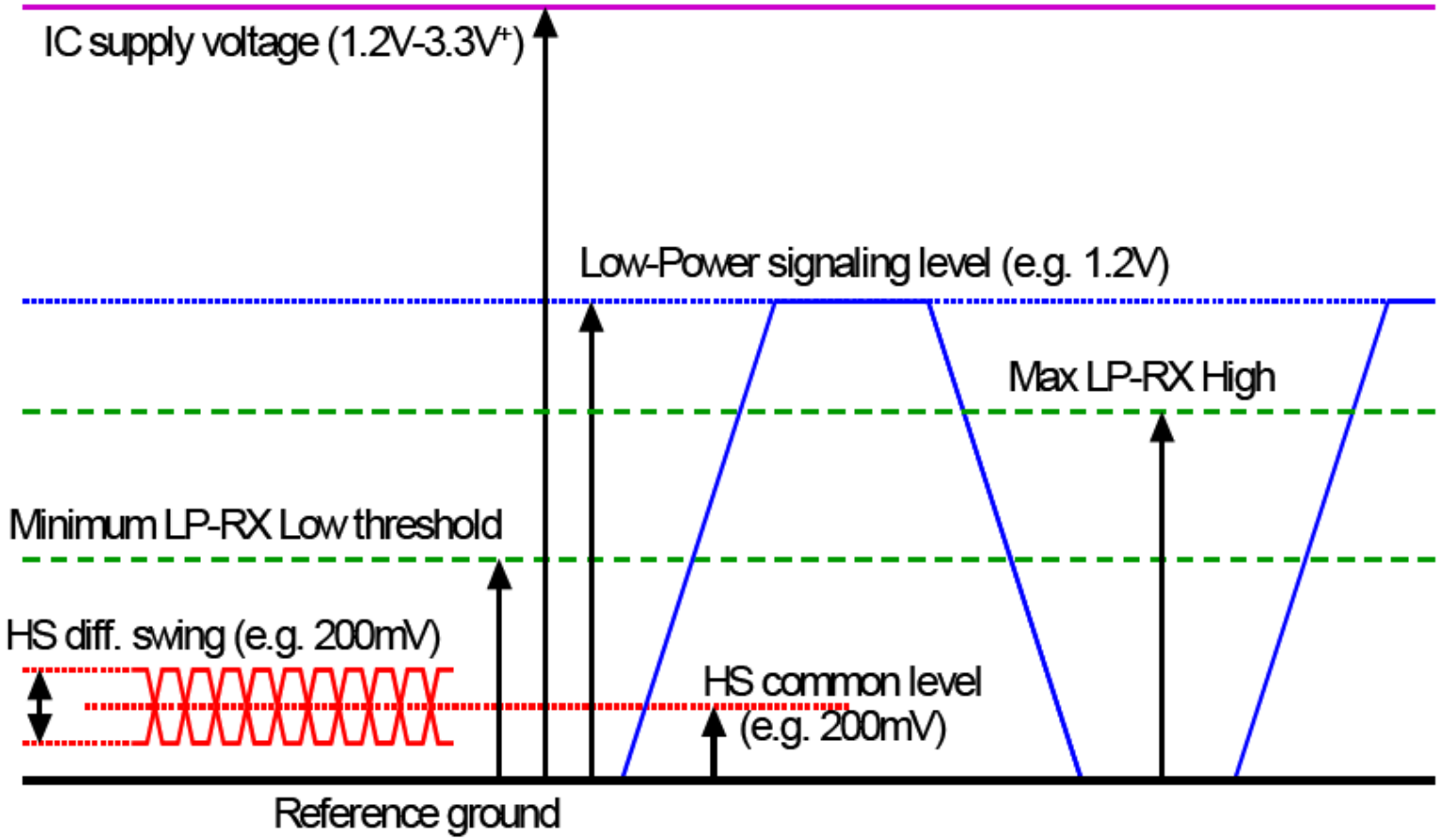
2 data lanes MIPI D-PHY Link Example

Master drives the clock

MIPI D-PHY at the Physical Layer

Dual Signaling for high speed and low power transmission

Dynamic termination



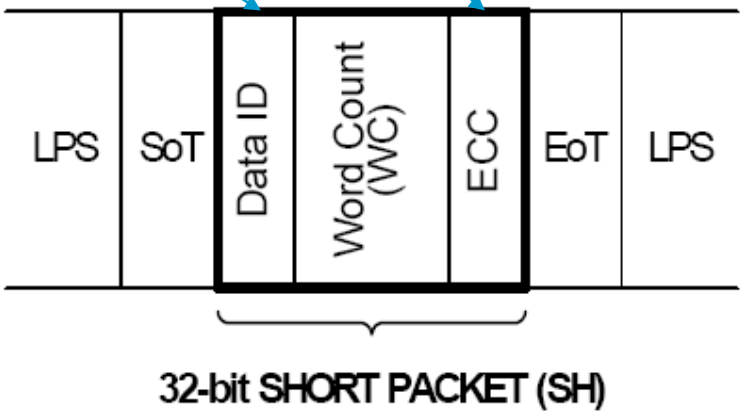
MIPI D-PHY Signals

MIPI DPhy DSI/CSI-2 Short Packet Structure

Note: The packet structure is identical for DSI and CSI-2. The difference is the interpretation of the Data ID field.

Data Identifier: Contains the Data Type Information (Short vs. Long) denotes the format/content of the Payload Data.

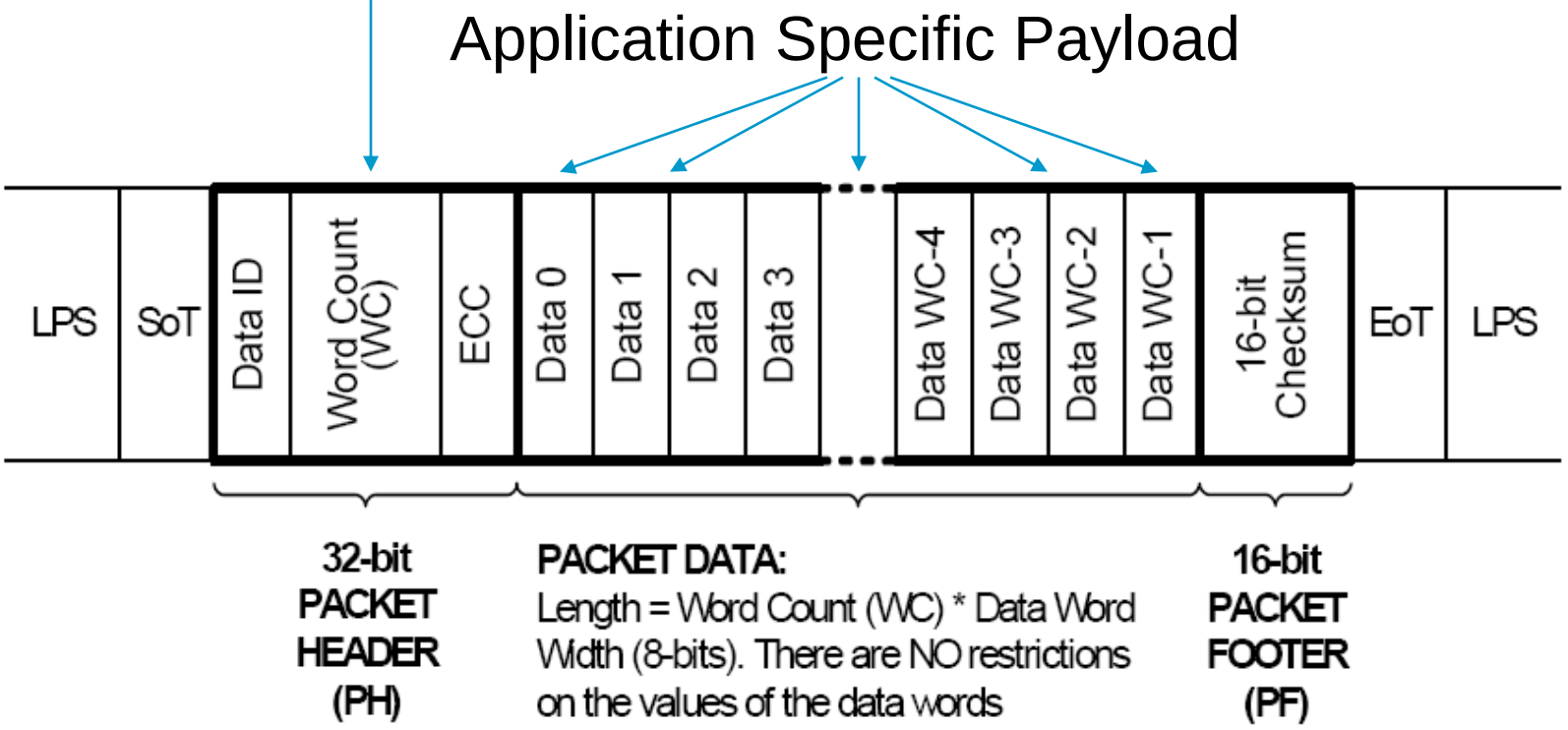
8-bit Correction Code: 8-bit ECC code for the Packet Header. Allows 1-bit error correction and 2-bit error detection.



MIPI DSI/CSI-2 Long Packet Structure

16-bit Word Count(WC):

The receiver reads the next WC data words independent of value. The receiver uses the WC value to determine the End of Packet.



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MIPI Interfaces in Smart Devices

- MIPI Overview
- D-PHY Overview
- **M-PHY Overview**

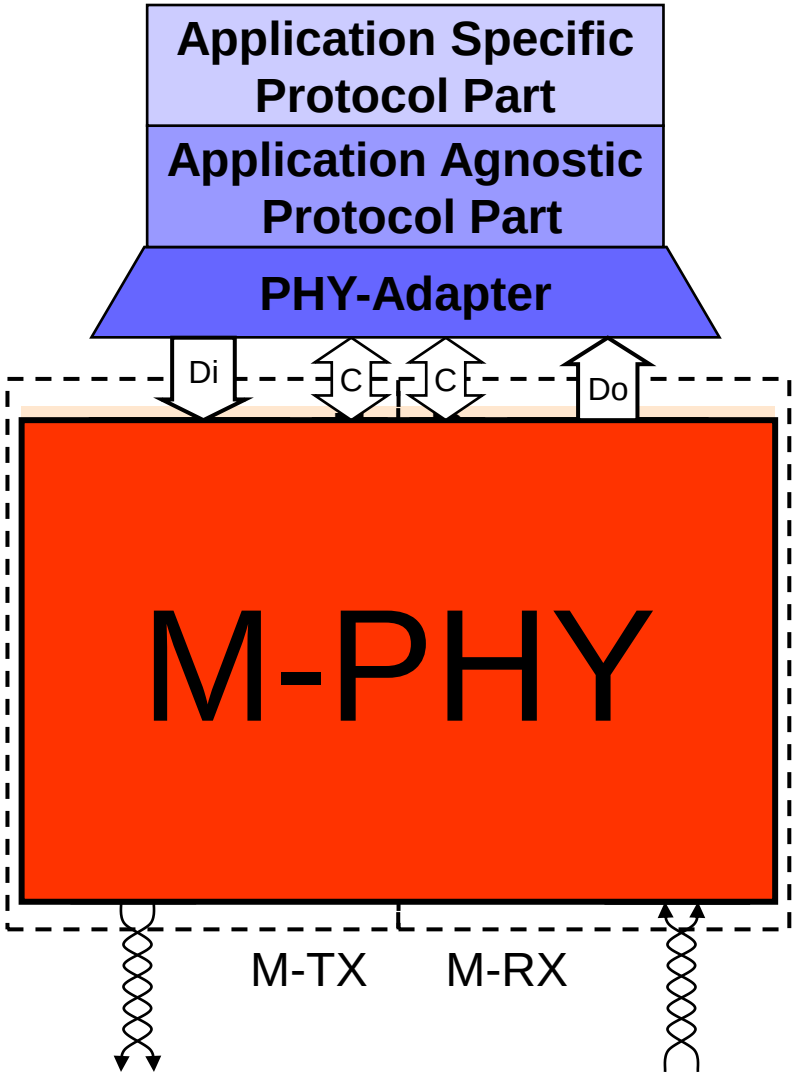
Validating MIPI Interfaces

Outlook

Main properties of M-PHY

Main LANE characteristics		2 pins/wires, differential, unidirectional
Minimum composition		Dual-simplex (4 wires)
Media		0-30 cm PCB, micro coax <1.2 m cable optical waveguides
Clocking method	HS LS	Embedded clock (8b10b) with or without shared RefClk PWM: Self-clocking SYS: Synchronous to RefClk
Raw bitrates (8b10b coded)	HS LS	1¼ & 1½, 2½ & 3 , 5 & 6 Gb/s PWM: 10 kb/s-600 Mb/s SYS: RefClk rate
RefClk frequencies		19.2 / 26 / 38.4 / 52 MHz
Data BURST encoding		8b10b
Power efficiency (overall)		<10pJ per payload-bit
CDR at receive side		Yes for HS, No for LS(-only)
TX pre-emphasis / RX equalization		No / Not specified
Signal levels (supply independent!)		0 - 200mV$_{RT}$ - 400mV$_{NT}$ (large drive) 0 - 100mV$_{RT}$ - 200mV$_{NT}$ (small drive)
Configuration		Using protocol & PHY mechanisms

Layered Interface Standards

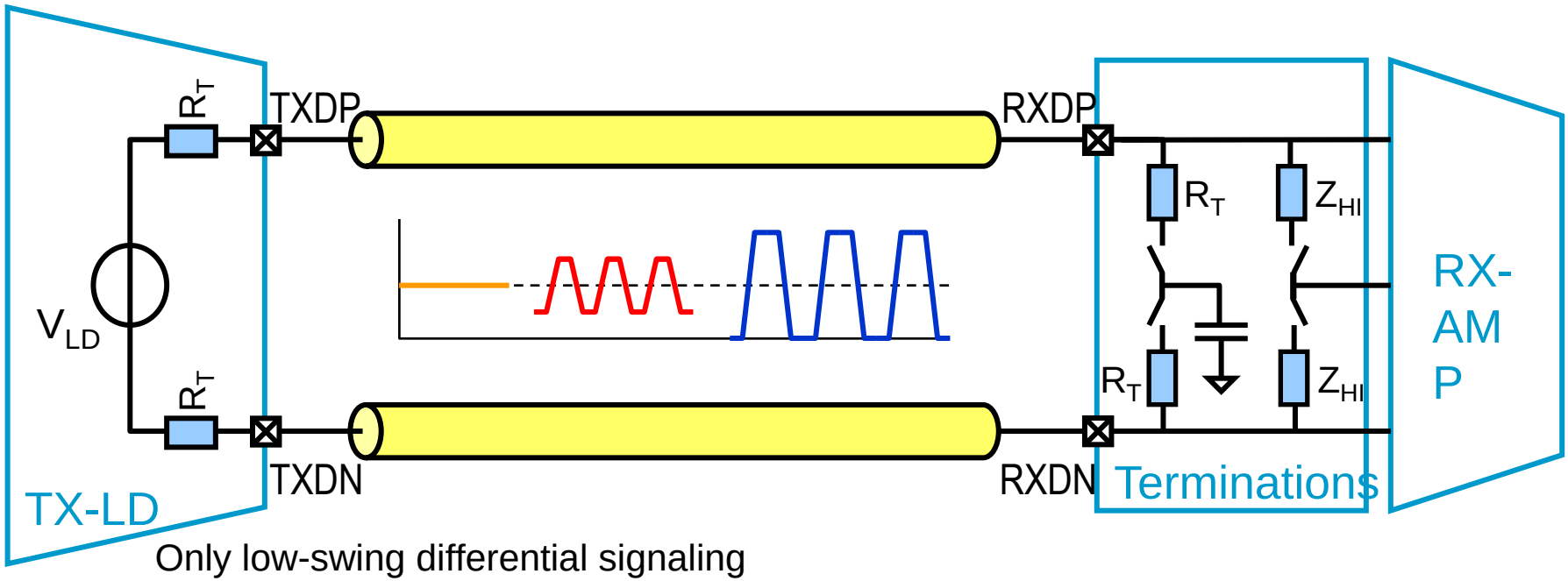


Applications:

- DigRF v4
- UniPRO
  - CSI / DSI / UFS / GBT
- LLI

M-PHY Scope

Electrical signal characteristics



Only low-swing differential signaling

TX always provides LINE termination

Switchable RX line termination: operation with or without termination

RX can hold undriven LINE at ‘differential-zero’ with Z_{HI} impedances

Two different TX drive strengths: Large & Small (=Large/2)

Optional Slew-Rate Control for EMI reduction

mipi℠ mobile industry processor interface

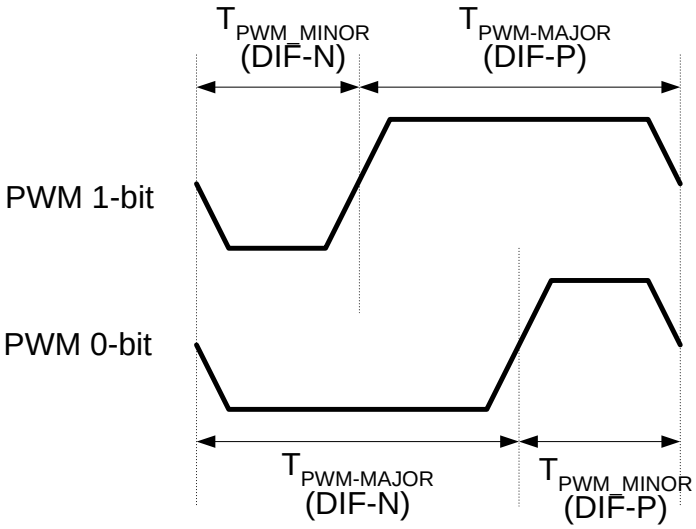
Bit signaling schemes

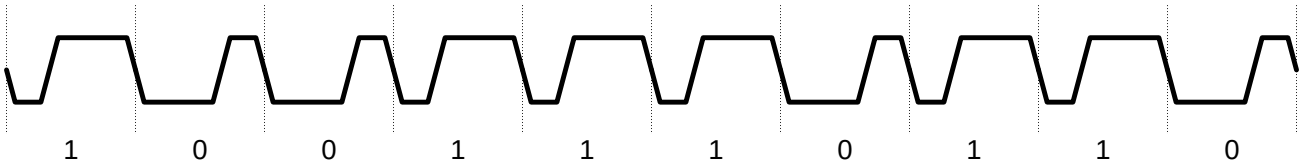
NRZ

- Non-Return-to-Zero (Trivial)

PWM

- Pulse-Width-Modulation
- Self-Clocking





mipi SM
mobile industry processor interface

Comparison of D-PHY with M-PHY

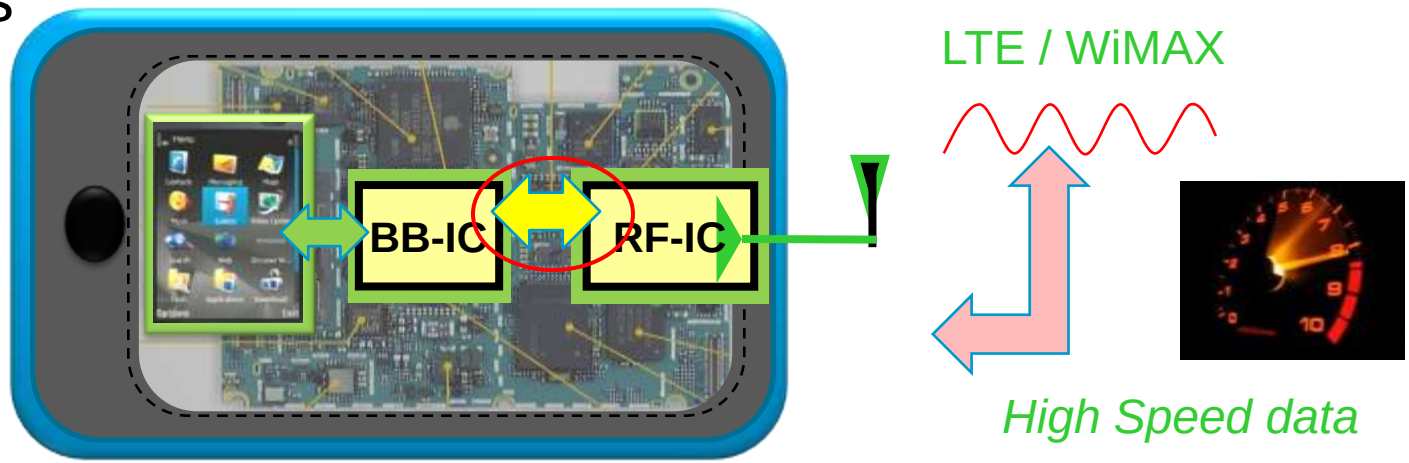
Min. number of pins per direction		4	2
Minimum configuration		4 only unidir or half-duplex	4 dual-simplex=full-duplex
Minimal UniPRO configuration		8	4
Medium		<30 cm PCB, flex, micro coax	< 30 cm PCB, flex, micro coax, <1.2 m cable, optical
Data rate per lane	HS	>80 Mb/s (Practical limit <1Gb/s)	~ 1¼ , 2½ , 5 Gb/s ~ 1½ , 3 , 6 Gb/s
	LP	< 10 Mb/s	10k-600Mb/s
Electrical signaling	HS	SLVS-200	SLVS-200
	LP	LVCMOS1.2V	SLVS-200 w/o RX-R_T
HS Clocking method		DDR Source-Sync Clk	Embedded Clk
HS Line coding		None or 8b9b	8b10b
Power – Energy/bit		Low	Lower
Receiver CDR required		No	Yes
Suited for optical transmission		No	Yes
LP only PHY's		Disallowed	Allowed

DigRF V4 Overview

DigRF v4 is the next generation link between the BB-IC and RF-IC in a mobile device, enabling LTE and WiMAX data rates

Bus between BB-IC and RF-IC must support high traffic flows

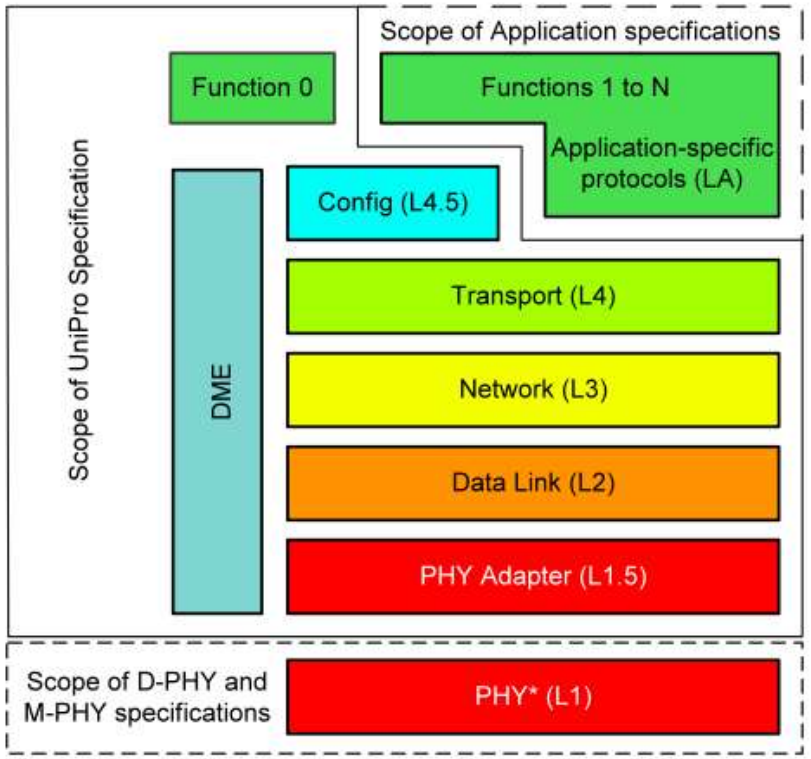
4G standards (LTE, WiMAX) enable downlink speed of over 300 MBit/s



DigRF V4 is an enabling technology for LTE and WiMAX Applications

UniPro Overview

- D-PHY and M-PHY
- High Scalable Bandwidth with low pin-count
- Low power consumption
- Reliable packet based, latency-aware Traffic Classes
- Network architecture
- Connection management
- Device discovery
- Remote configuration
- Security



Layered Model of UniPro v1.5

*MIPI D-PHY or MIPI M-PHY

Low Latency Interface (LLI) Overview

The LLI interface allows sharing a DRAM memory between 2 chips for data and program. The main motivation for LLI is cost reduction.

The LLI specification defines several logical layers to help to make the specification more understandable:

- Transaction layer: exchanges memory mapped read/write transactions and signals between 2 chips.
- Data link layer: provides several independent virtual channels between the 2 chips.
- PHY adapter layer: provides an interface to the physical media. Focus first on serial MIPI M-PHY. Ensure reliability as necessary.
- Power management. Interface control for optimal power consumption; definition of the power states.
- Boot and reset
- Test

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Validating MIPI Interfaces

- **Testing Overview**
- D-PHY Testing
- M-Phy Testing

Outlook

Test Applications

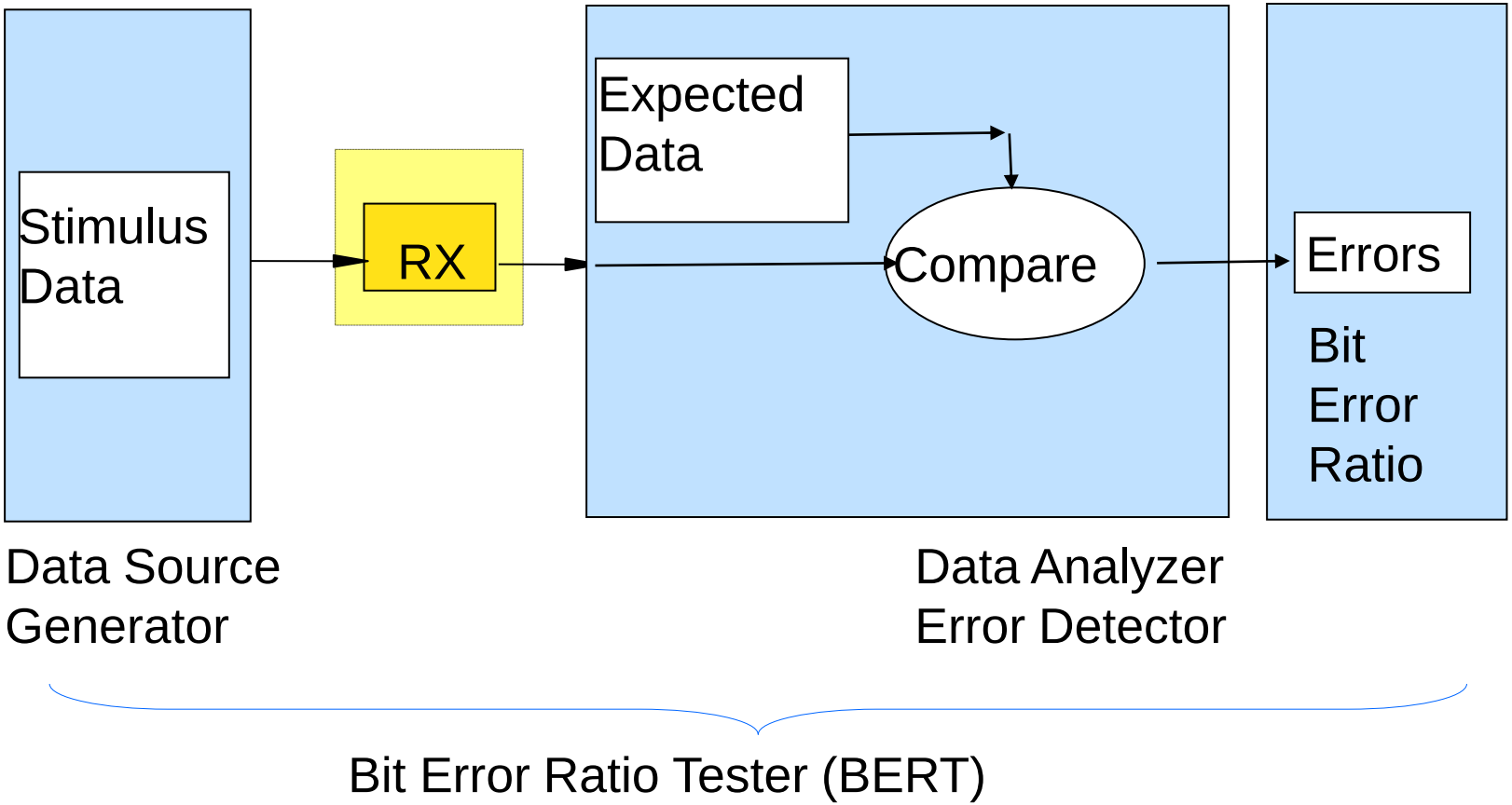
Electrical Layer

- TX & RX Compliance (Scope & Generator (BERT))
- BringUp & Debug (Scope)

Protocol & Application Layer

- Protocol Compliance (Protocol Exerciser / Analyzer)
- BringUp & Debug (Protocol analyzer or Scope)
- Device Emulation (Protocol Exerciser)
- Performance Validation (Protocol Exerciser)
- Application testing (Software Add-ons for Protocol exerciser)

How to electrically test an RX
Bit Error Ratio Test Principle



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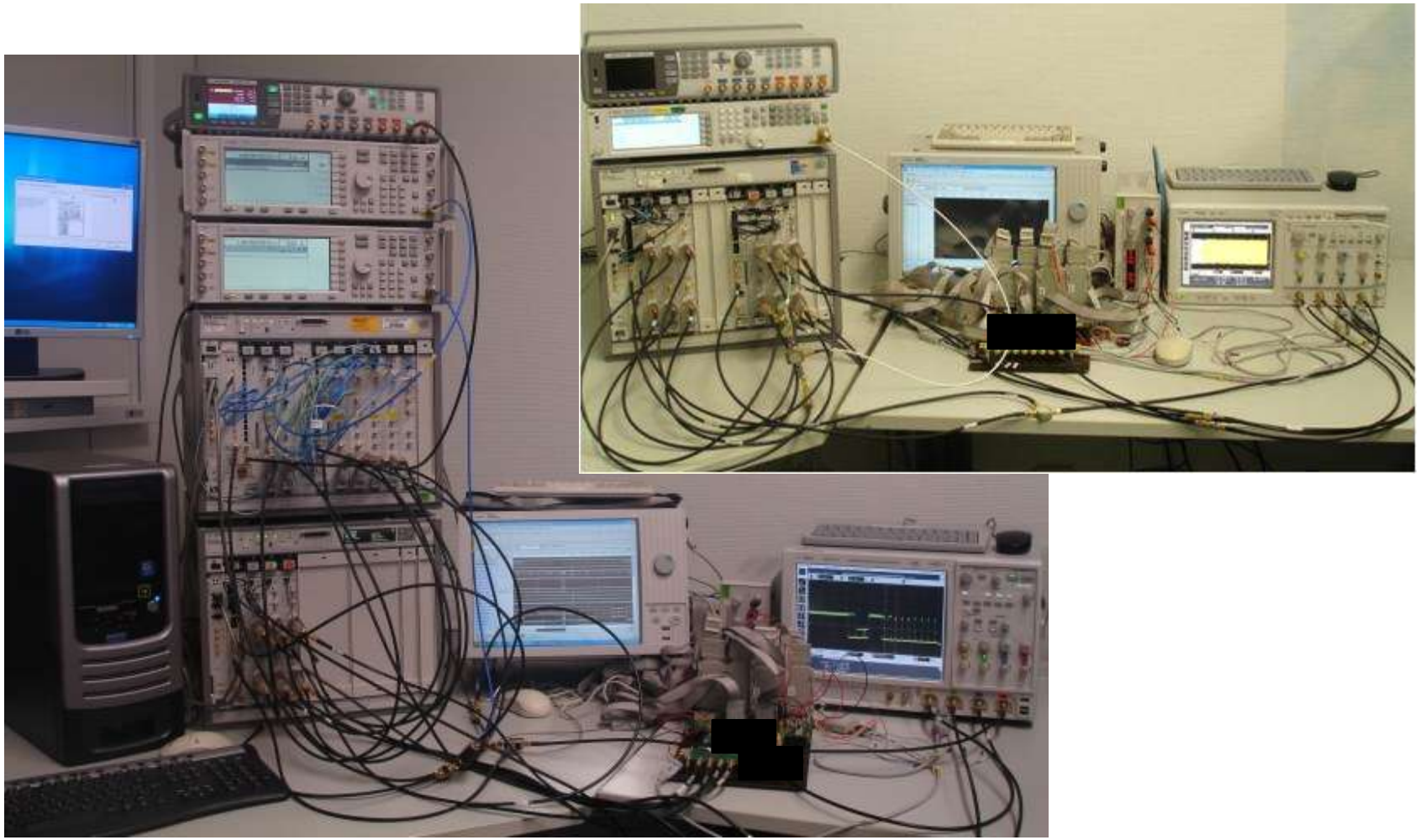
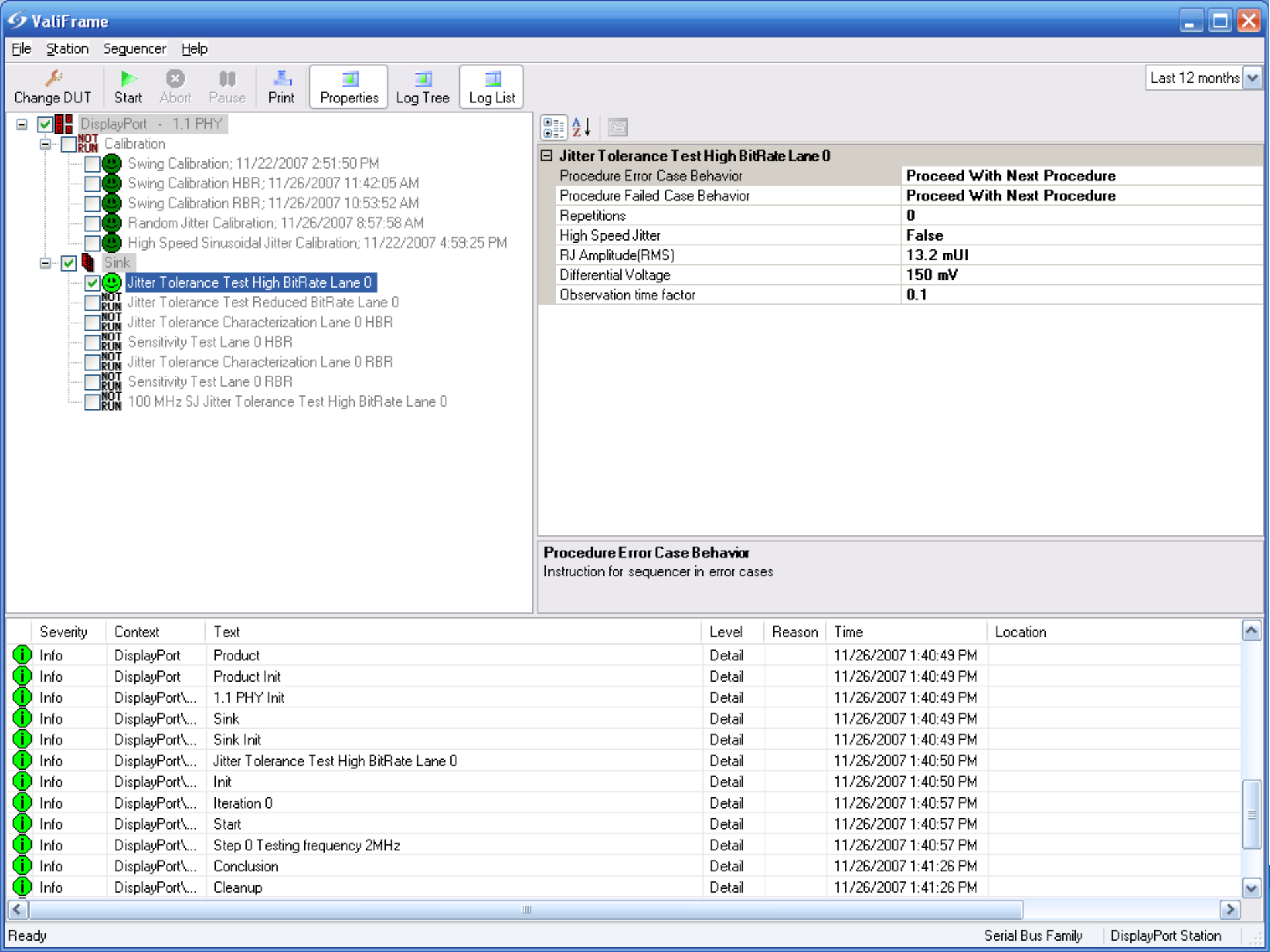
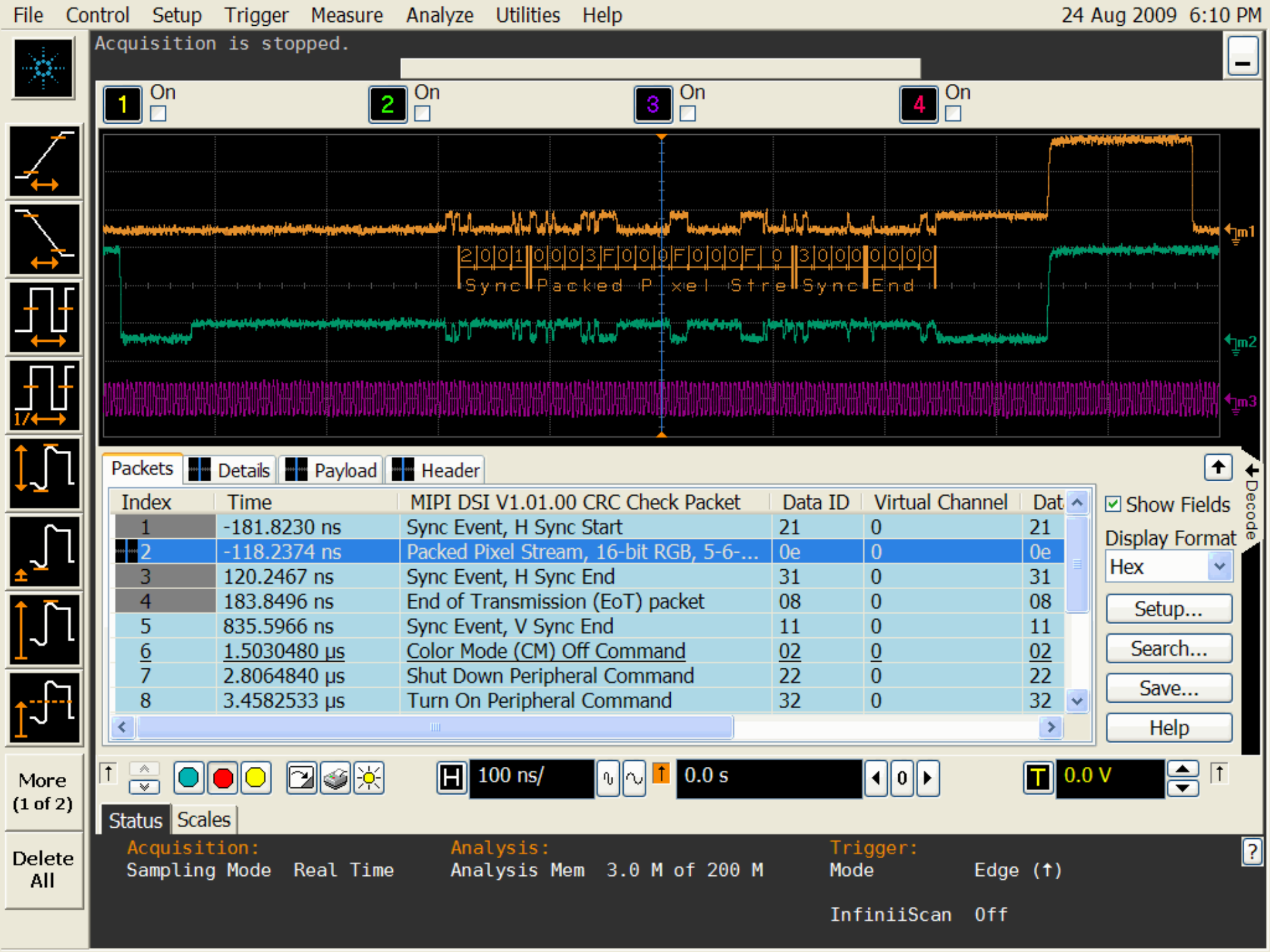
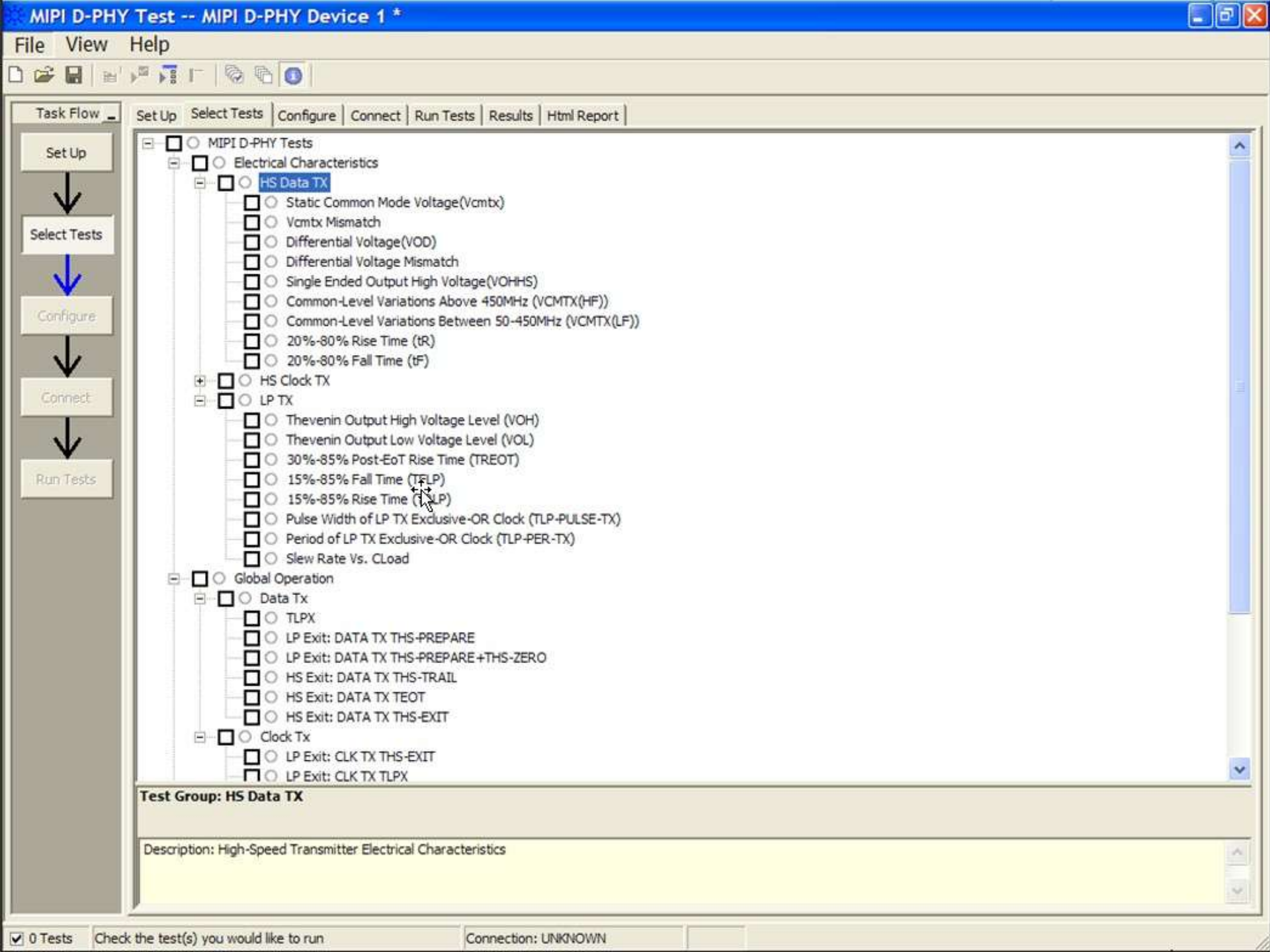
Agilent D-PHY Physical Layer Test Solution
Integrated Rx and Tx Test Setups




ValiFrame
File
Station
Sequencer
Help
Change DUT
Start
Abort
Pause
Print
Properties
Log Tree
Log List
Last 12 months
DisplayPort - 1.1 PHY
Calibration
Swing Calibration; 11/22/2007 2:51:50 PM
Swing Calibration HBR; 11/26/2007 11:42:05 AM
Swing Calibration RBR; 11/26/2007 10:53:52 AM
Random Jitter Calibration; 11/26/2007 8:57:58 AM
High Speed Sinusoidal Jitter Calibration; 11/22/2007 4:59:25 PM
Sink
Jitter Tolerance Test High BitRate Lane 0
Jitter Tolerance Test Reduced BitRate Lane 0
Jitter Tolerance Characterization Lane 0 HBR
Sensitivity Test Lane 0 HBR
Jitter Tolerance Characterization Lane 0 RBR
Sensitivity Test Lane 0 RBR
100 MHz SJ Jitter Tolerance Test High BitRate Lane 0
Jitter Tolerance Test High BitRate Lane 0
Procedure Error Case Behavior
Proceed With Next Procedure
Procedure Failed Case Behavior
Proceed With Next Procedure
Repetitions
0
High Speed Jitter
False
RJ Amplitude(RMS)
13.2 mUI
Differential Voltage
150 mV
Observation time factor
0.1
Procedure Error Case Behavior
Instruction for sequencer in error cases
Severity
Context
Text
Level
Reason
Time
Location
Info DisplayPort Product Detail 11/26/2007 1:40:49 PM
Info DisplayPort Product Init Detail 11/26/2007 1:40:49 PM
Info DisplayPort\... 1.1 PHY Init Detail 11/26/2007 1:40:49 PM
Info DisplayPort\... Sink Detail 11/26/2007 1:40:49 PM
Info DisplayPort\... Sink Init Detail 11/26/2007 1:40:49 PM
Info DisplayPort\... Jitter Tolerance Test High BitRate Lane 0 Detail 11/26/2007 1:40:50 PM
Info DisplayPort\... Init Detail 11/26/2007 1:40:50 PM
Info DisplayPort\... Iteration 0 Detail 11/26/2007 1:40:57 PM
Info DisplayPort\... Start Detail 11/26/2007 1:40:57 PM
Info DisplayPort\... Step 0 Testing frequency 2MHz Detail 11/26/2007 1:40:57 PM
Info DisplayPort\... Conclusion Detail 11/26/2007 1:41:26 PM
Info DisplayPort\... Cleanup Detail 11/26/2007 1:41:26 PM
Ready
Serial Bus Family
DisplayPort Station

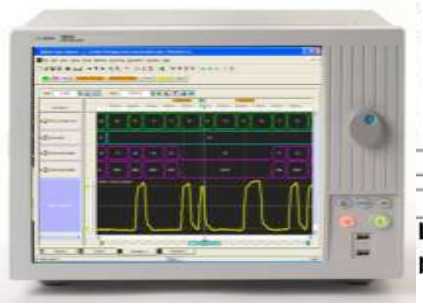

File Control Setup Trigger Measure Analyze Utilities Help
24 Aug 2009 6:10 PM
Acquisition is stopped.
1 On
2 On
3 On
4 On
2 0 0 1 0 0 0 3 F 0 0 0 F 0 0 0 F 0 3 0 0 0 0 0 0
Sync Packed P xel Stre Sync End
m1
m2
m3
Packets
Details
Payload
Header
Index
Time
MIPI DSI V1.01.00 CRC Check Packet
Data ID
Virtual Channel
Dat
1 -181.8230 ns Sync Event, H Sync Start 21 0 21
2 -118.2374 ns Packed Pixel Stream, 16-bit RGB, 5-6-... 0e 0 0e
3 120.2467 ns Sync Event, H Sync End 31 0 31
4 183.8496 ns End of Transmission (EoT) packet 08 0 08
5 835.5966 ns Sync Event, V Sync End 11 0 11
6 1.5030480 µs Color Mode (CM) Off Command 02 0 02
7 2.8064840 µs Shut Down Peripheral Command 22 0 22
8 3.4582533 µs Turn On Peripheral Command 32 0 32
Show Fields
Display Format
Hex
Setup...
Search...
Save...
Help
Decode
More (1 of 2)
Delete All
H 100 ns/ 0.0 s 0
T 0.0 V
Status
Scales
Acquisition:
Sampling Mode Real Time
Analysis:
Analysis Mem 3.0 M of 200 M
Trigger:
Mode Edge (↑)
InfiniiScan Off


MIPI D-PHY Test -- MIPI D-PHY Device 1 *
File View Help
Task Flow
Set Up
Select Tests
Configure
Connect
Run Tests
Set Up
Select Tests
Configure
Connect
Run Tests
Results
Html Report
MIPI D-PHY Tests
Electrical Characteristics
HS Data TX
Static Common Mode Voltage(Vcmtx)
Vcmtx Mismatch
Differential Voltage(VOD)
Differential Voltage Mismatch
Single Ended Output High Voltage(VOHHS)
Common-Level Variations Above 450MHz (VCMTX(HF))
Common-Level Variations Between 50-450MHz (VCMTX(LF))
20%-80% Rise Time (tR)
20%-80% Fall Time (tF)
HS Clock TX
LP TX
Thevenin Output High Voltage Level (VOH)
Thevenin Output Low Voltage Level (VOL)
30%-85% Post-EoT Rise Time (TREOT)
15%-85% Fall Time (TFLP)
15%-85% Rise Time (TRLP)
Pulse Width of LP TX Exclusive-OR Clock (TLP-PULSE-TX)
Period of LP TX Exclusive-OR Clock (TLP-PER-TX)
Slew Rate Vs. CLoad
Global Operation
Data Tx
TLPX
LP Exit: DATA TX THS-PREPARE
LP Exit: DATA TX THS-PREPARE+THS-ZERO
HS Exit: DATA TX THS-TRAIL
HS Exit: DATA TX TEOT
HS Exit: DATA TX THS-EXIT
Clock Tx
LP Exit: CLK TX THS-EXIT
LP Exit: CLK TX TLPX
Test Group: HS Data TX
Description: High-Speed Transmitter Electrical Characteristics
0 Tests
Check the test(s) you would like to run
Connection: UNKNOWN

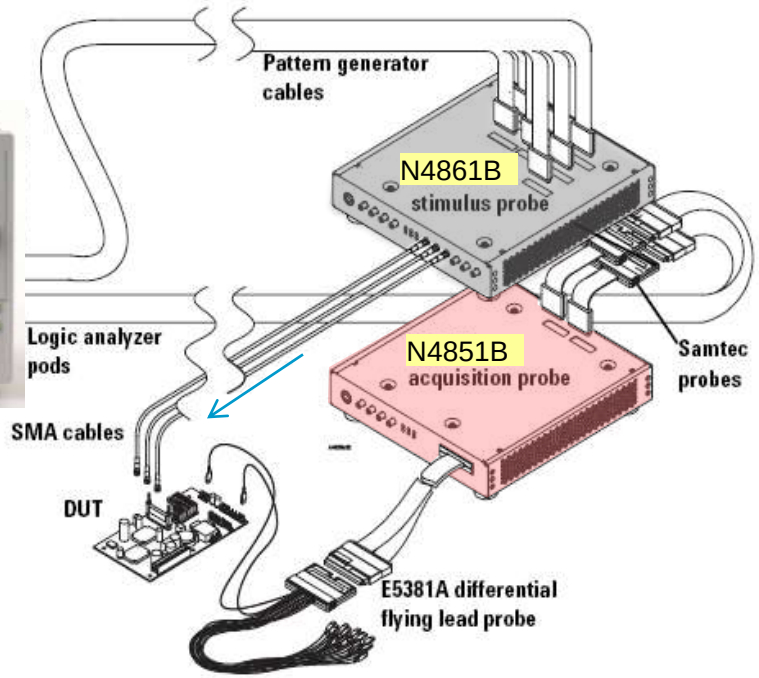
MIPI D-PHY Protocol Test System configuration

Protocol Stimulus and Analysis

16720A pattern
Generator module



All LA modules
Except 16962A



N4861B Stimulus Probe

- Speed : 1Gbps per lane
- 3 lanes support
- CSI & DSI stimulus generation
- Error injection
- Voltage control
- Timing control
- High Speed and Low power mode

N4851B Analysis Probe

- Speed : up to 1Gbps per lane
- 4 lanes support
- Flying leads or soft touch
- Full Protocol Triggering
- Real time error detection
- CSI & DSI packet viewer
- High Speed and Low power mode

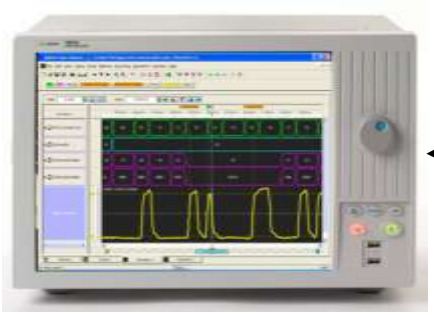
Notes :

- Loopback board orderable N4850-66402 for around $750.
- Dynamic termination board available from UNH-IOL.

Test Model #1 : Camera Sensor Test

Functional Analysis

CSI Protocol Trigger and Display



Logic Analyzer

Real-time capture

N4851B

MIPI
D-PHY
CSI
4 lanes
940Mbps

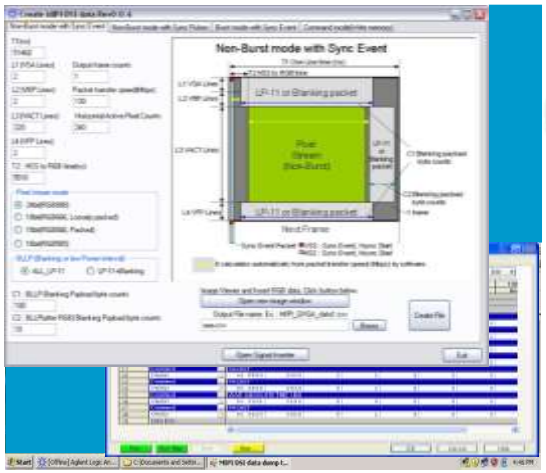
Camera

- Capture Traffic in real-time
- Protocol Level Trigger and Display
- Real time Errors detection
- Compliance test

Notes :
- Analyzer operates in high impedance mode
- Dynamic Termination required on target System
- Camera= bus Master

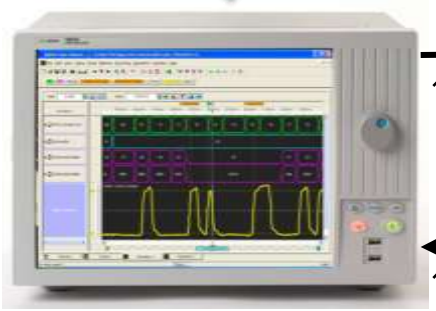
Test Model #2 : Display Module Evaluation
Functional Stimulus and Analysis

Initialization Commands
Data File



DSI Packet & Image Generation

Send Stimulus to Display Device



N4861B

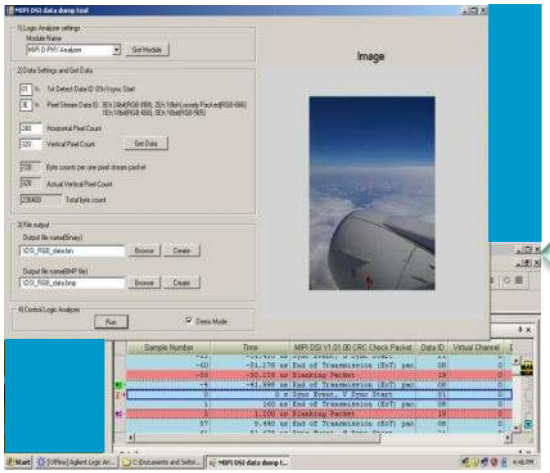
N4851B

MIPI
D-PHY
DSI

Display

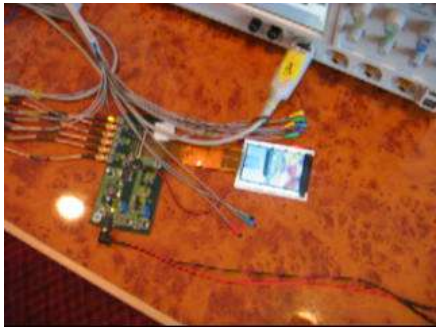
Logic
Analyzer

Real-time capture of Bus activity



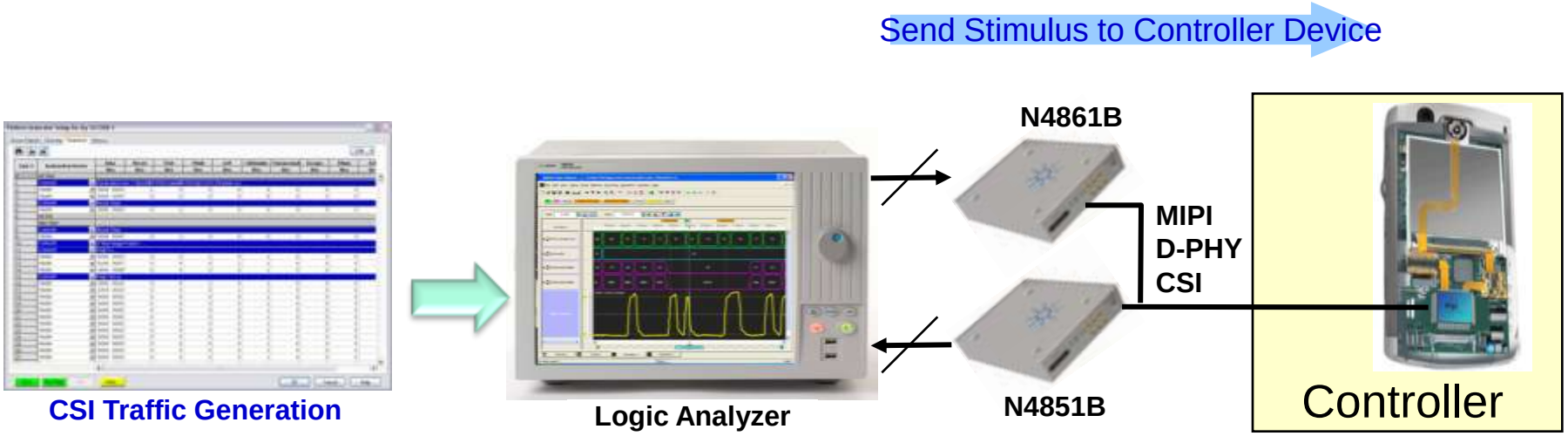
DSI Packet & Image View

Notes :
- Dynamic Impedance required on target system if bus-turn around



Test model #3 : Camera Emulation

Functional Analysis



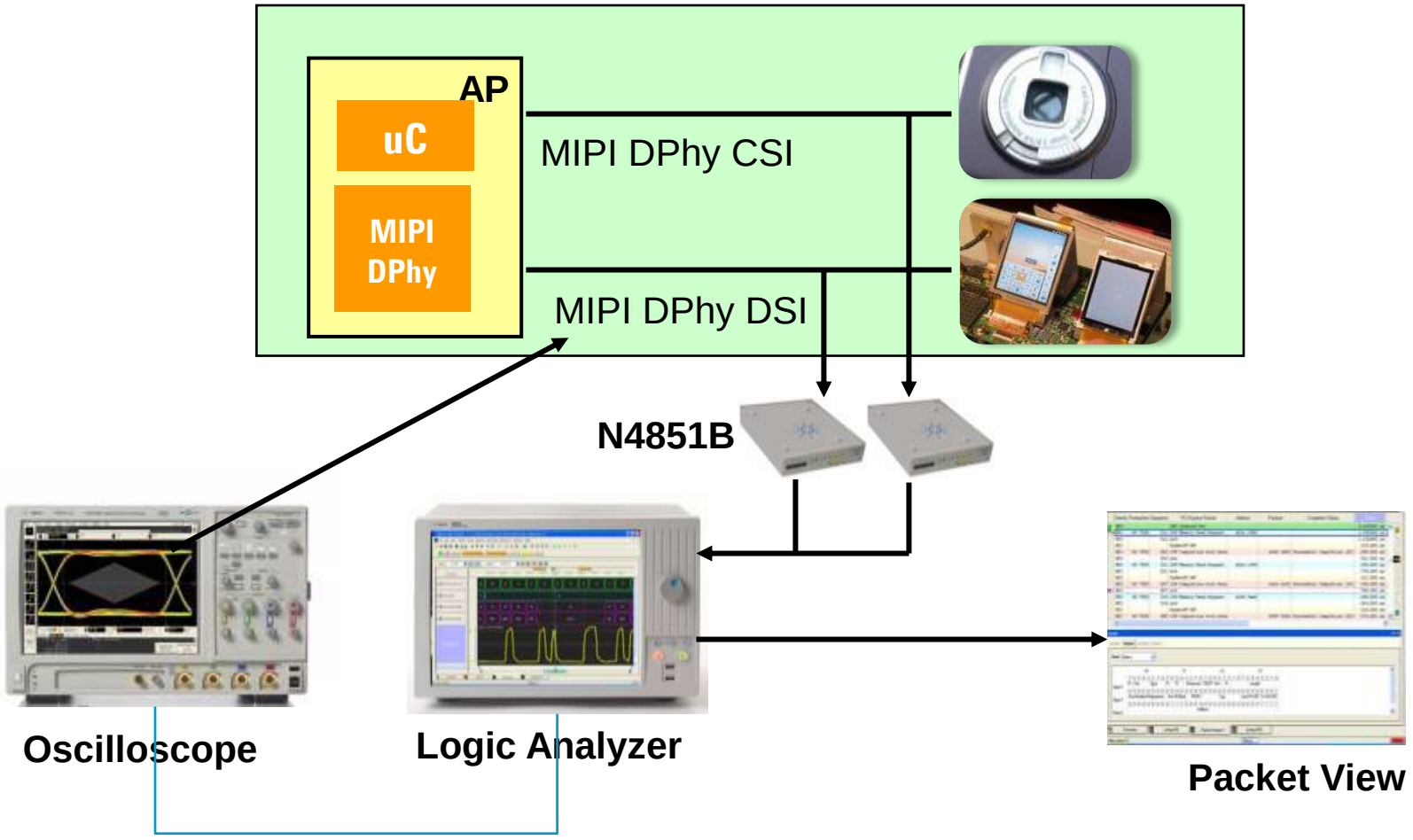
Challenge : simulating various CSI devices

Generate Real-time CSI traffic

1Gbps on 3 lanes

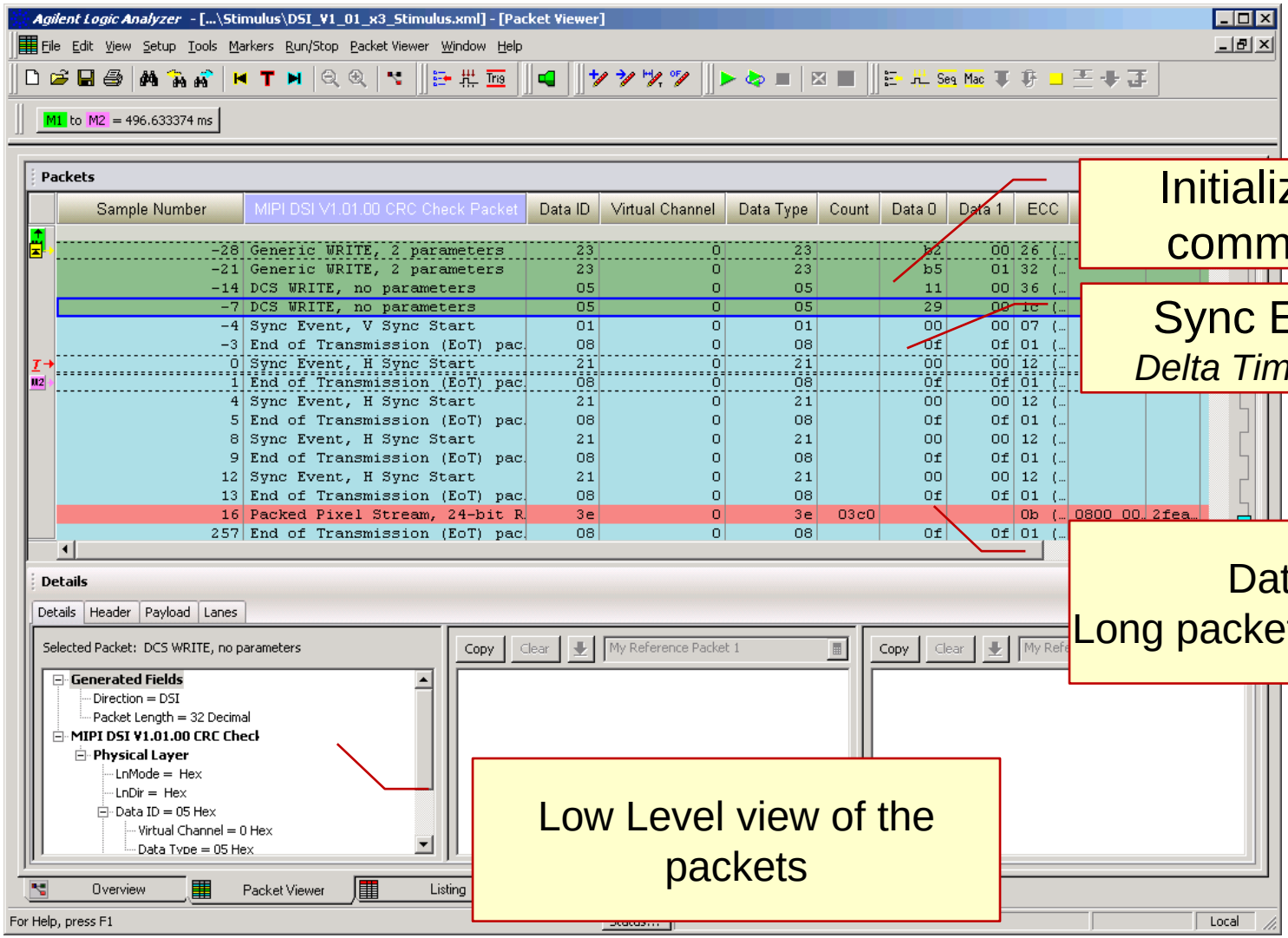
Capture and replay

Test model #4 : Controller, Display & Camera Integration



ViewScope for cross triggering and time correlated measurement

Protocol Analysis



Initialization commands

Sync Events
Delta Time critical

Data Traffic
Long packets (Pixel Stream)

Low Level view of the packets

Agenda

Introduction, Smart Device Overview

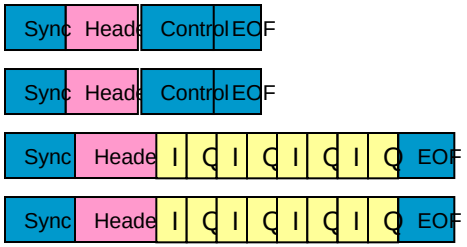
MIPI Interfaces in Smart Devices

Validating MIPI Interfaces

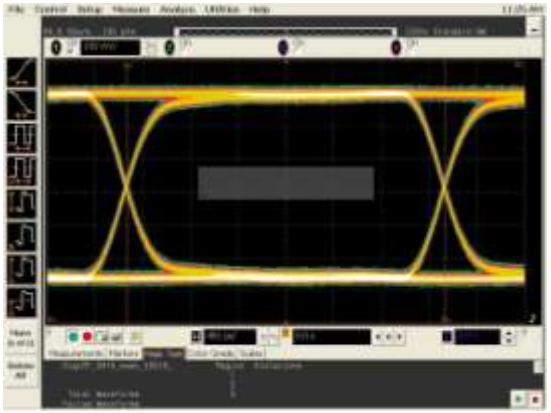
- Testing Overview
- D-PHY Testing
- **M-Phy Testing**

Outlook

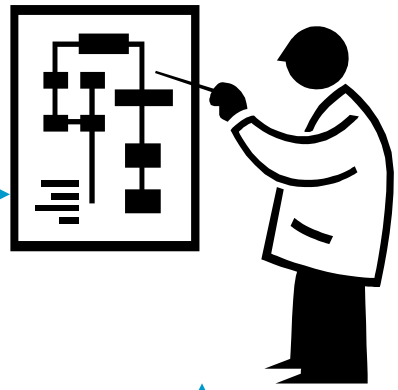
Knowledge/Techniques Required for DigRF Analysis

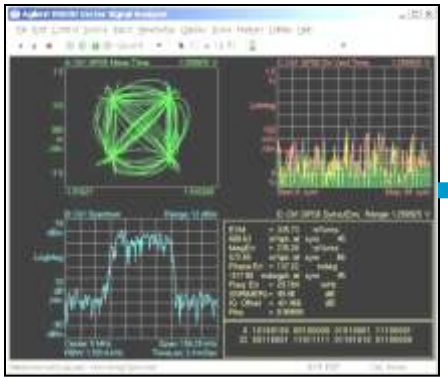


Logical Analysis Technique



Signal Integrity Knowledge





Digital I/Q Analysis Technique

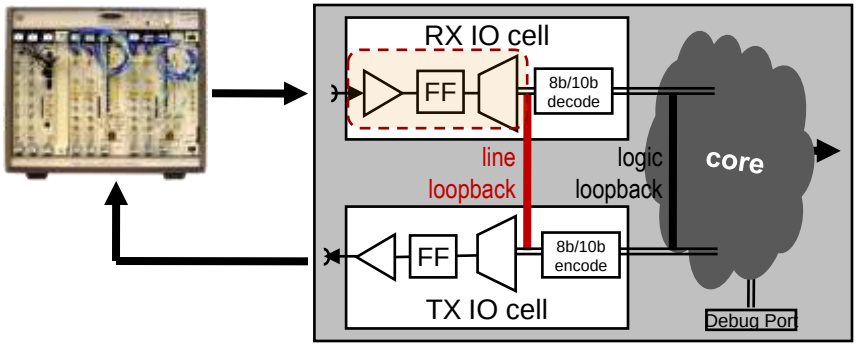
Various knowledge/techniques are required for DigRF analysis.
In particular there are new *high speed digital physical layer* and *protocol level* testing and validation required.

Receiver Test With BERT Generator and BERT Error Detector

Focus on receiver characterization and R&D level debugging

Utilizes the line loopback mode

Test pattern: all kinds of test pattern supported

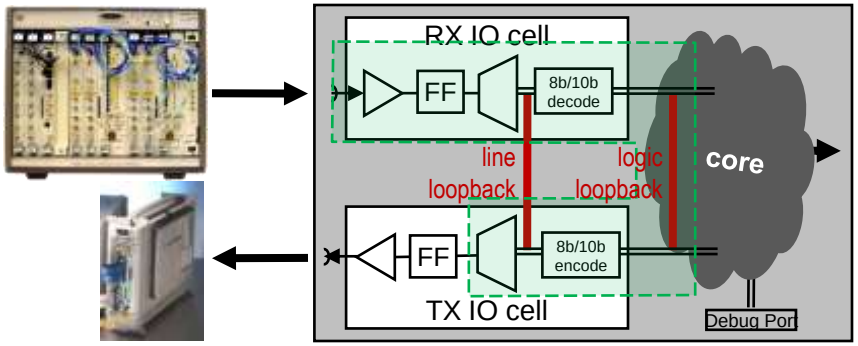


Receiver Test With BERT Generator and DigRFv4 Exerciser

Receiver characterization and system timing stress test

Utilizes the logic loopback mode with additional limited support for line loopback

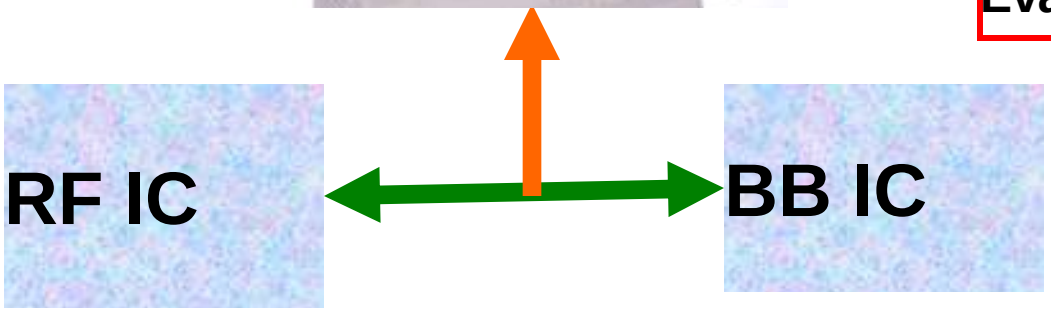
Test pattern:
DigRF4 commands with payload and checksum in logic loopback mode, and PRBS 7 and PRBS 15 in line loopback mode



Digital Signal Integrity Evaluation

DSO90000B Infiniium Series Oscilloscope

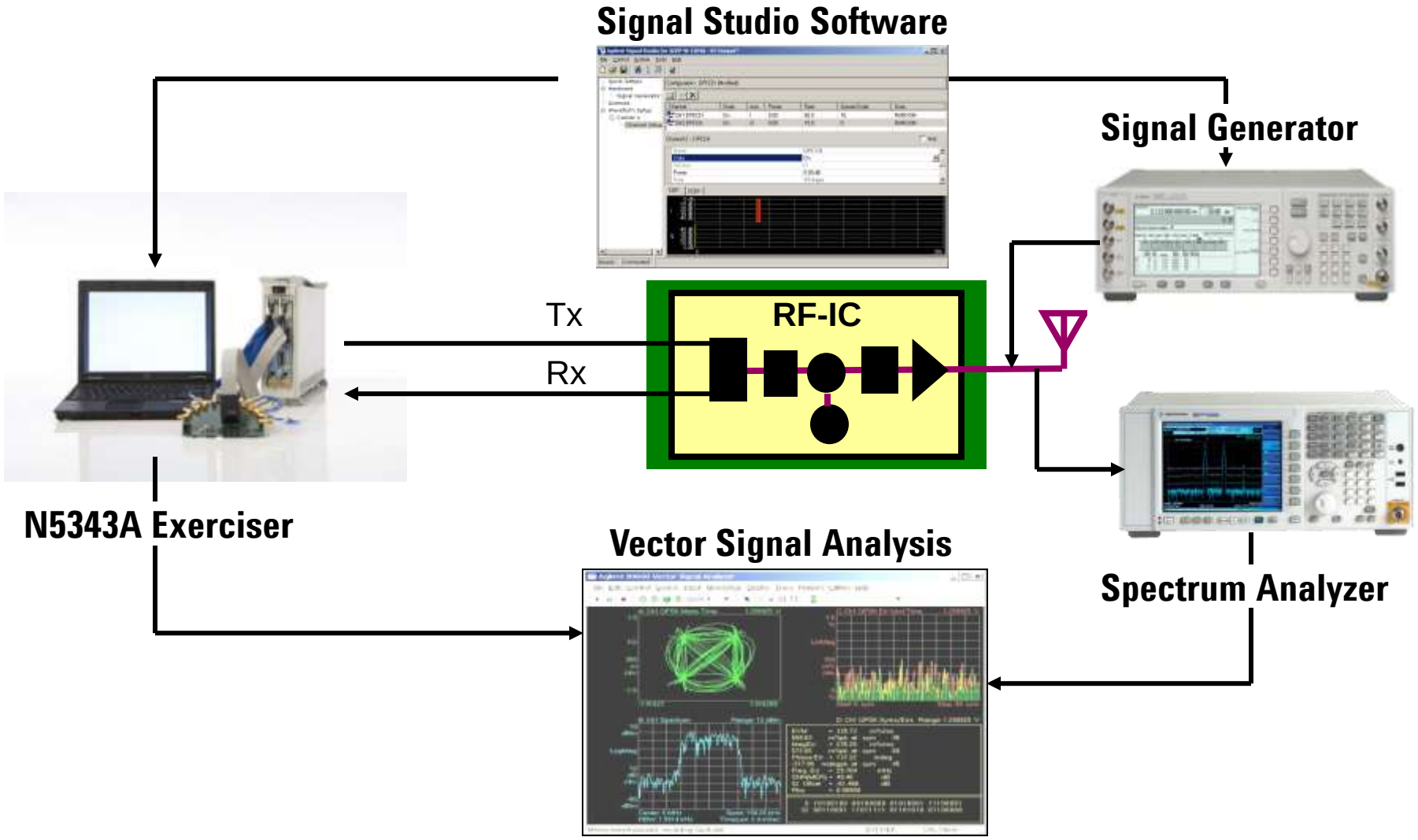
Signal Integrity Evaluation



DigRF evaluation begins with the digital physical layer evaluation. Digital quality is tied directly to the final RF quality

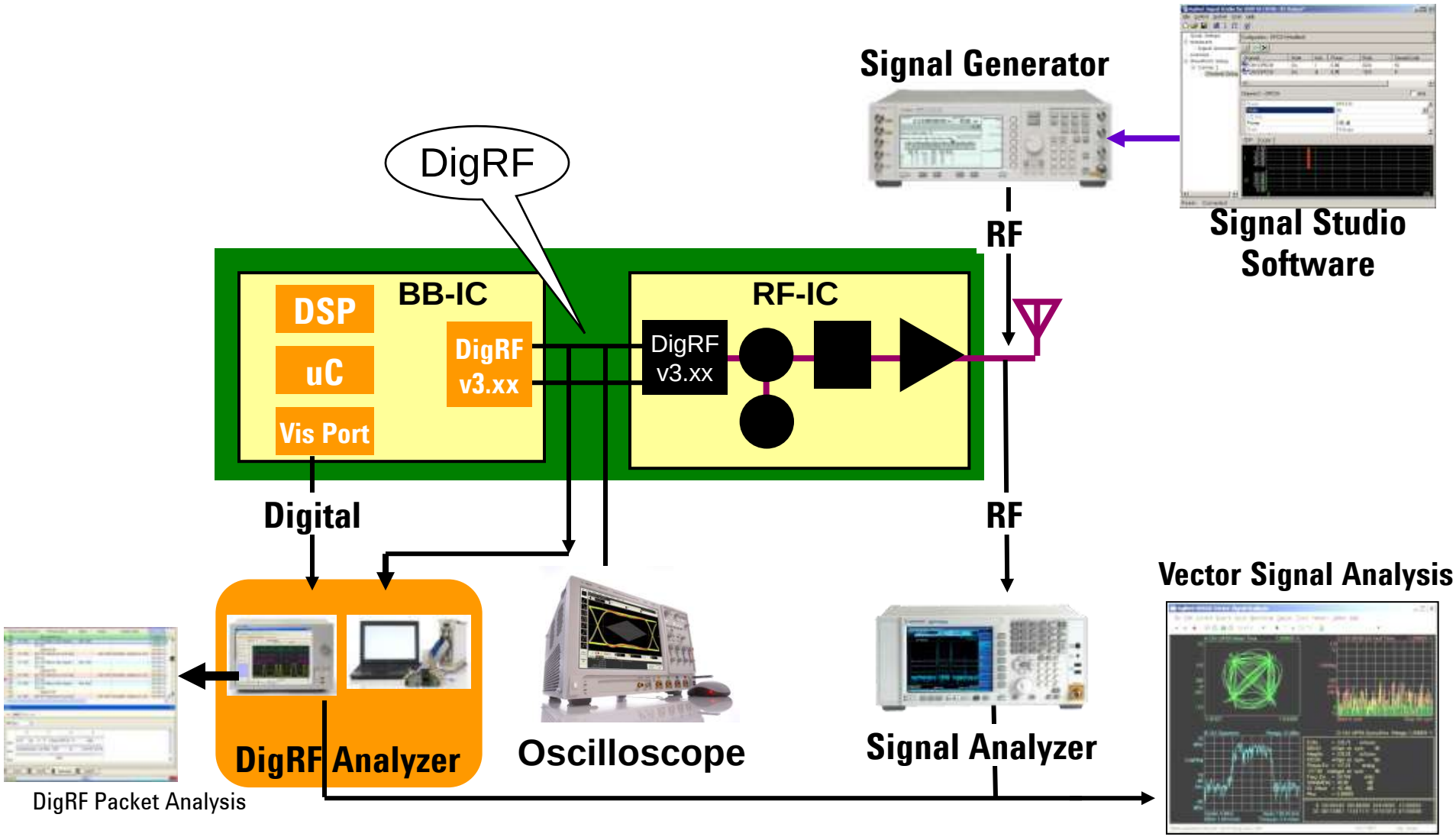
Preliminary Compliance test with UDA

DigRF v3/v4 RF-IC Unit Testing Environment



Modulation Analysis and C/N Measurement

RF-IC, BB-IC, Integration Testing Environment



Agenda

Introduction, Smart Device Overview

MIPI Interfaces in Smart Devices

Validating MIPI Interfaces

Outlook

What will happen in 2011 / 2012?

D-PHY evolving towards 1.3 .. 1.5 Gbit/s bandwidth

M-PHY Gear 2 followed by Gear 3

3D support for Display and Camera

CSI-3, DSI-2 and UFS on UniPro 1.4 / M-PHY Gear 2

Low Latency Interface 1.0

- UniPro based applications and LLI will require protocol aware stimulus as both protocols are implementing real-time handshaking.
- Agilent will ensure appropriate test equipment availability at the right time.

Do you have any questions?