8. How to operate IMX219PQH5-C

8-1 Power on sequence

Power on sequence of IMX219PQH5-C is below figure.

Startup Sequence in 2-wire Serial Communication Mode

Perform power-on according to the following sequence.
The XCLR pin must be released (Low → High) after all the power supplies (VANA,VDIG,VDDL) are completed.

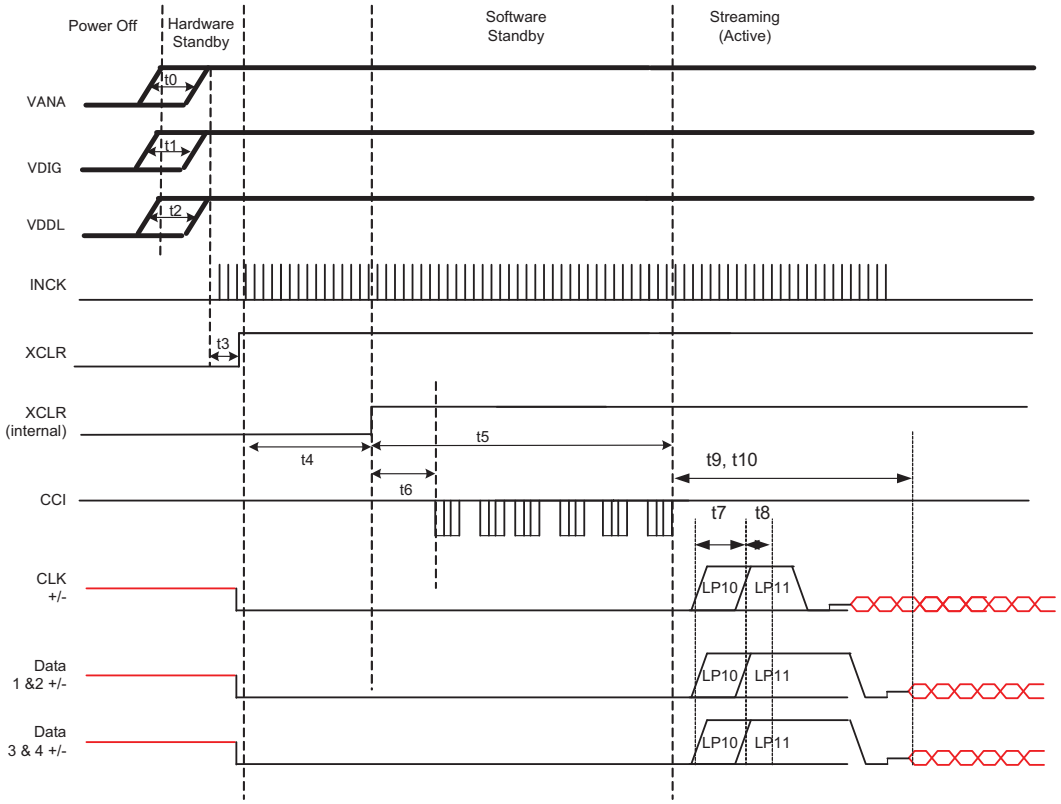

Fig. 38 Power-on Sequence in 2-wire Serial Communication Mode

Table 36 Operation Specifications 2-wire Serial Communication Mode

Constraint	Label	Min.	Max.	Units	Comment
Sequence free of VDDs rising	t0, t1, t2	VANA, VDIG, VDDL may rise in any order.		ns	
XCLR rising	t3	0.5	—	μs	
Internal XCLR is Low to High after VDDs & XCLR supplied	t4		200	μs	
releasing software standby after XCLR Low to High	t5	6	—	ms	charge up VRL
Initializing time of silicon	t6	—	32000	clocks	clock is INCK Case of INCK = 6[MHz], 5.3[msec]
D-PHY power-up	t7	1	1.1	ms	
D-PHY init	t8	100	110	μs	
After releasing software standby to data streaming time	t9	1.2 ms + exposure time	—		
Quick launch up time	t10	—	1	frame	stable time until optimal image quality

Start streaming sequence with 2-wire serial communication

IMX219PQH5-C requires the command sequence below to output image data.

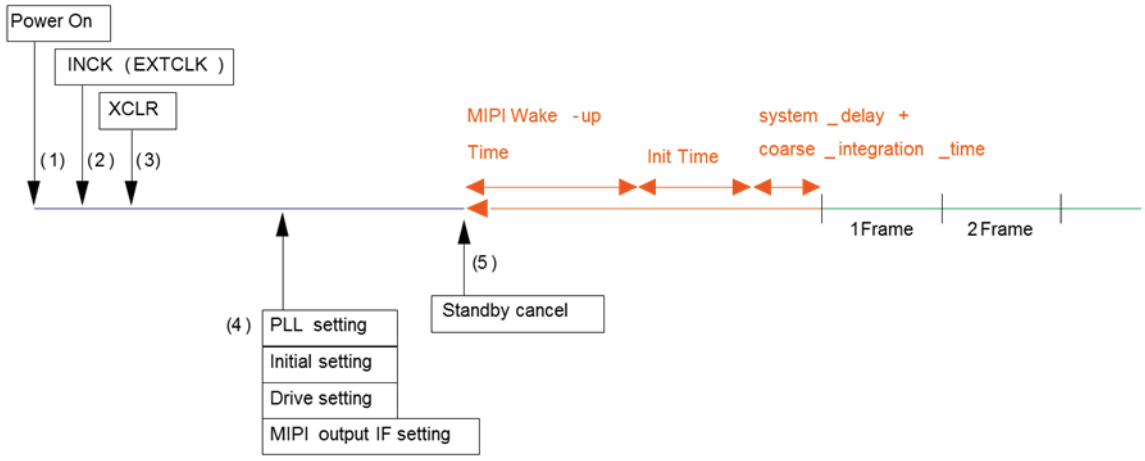

Fig. 39 Start streaming sequence with 2-wire serial communication (external reset)

Table 37 Initialization sequence with XCLR

(1) to (3)	Refer power up sequence timing diagram
(4)	Set PLL parameters
	Basic setting (operation-critical setting)
	Set Readout mode (start/end position, size, mode, integration time, and gain)
	Set MIPI interface parameters
(5)	Start streaming with 0x0100 (mode_select = 1)
	After “Wake Up Time” + “Init Time”, 1st frame starts and images come out

8-2 Power off sequence

Perform the power-off in the sequence shown below.

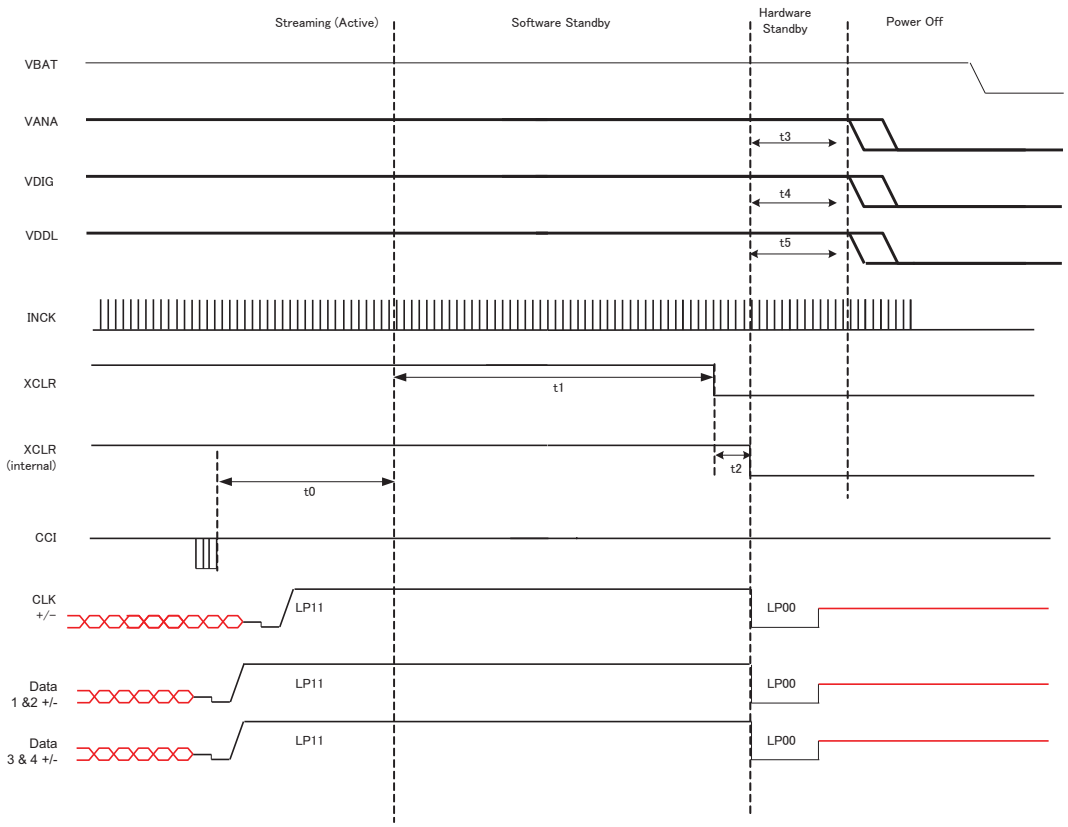

Fig. 40 Power-off Sequence in 2-wire Serial Communication

Table 38 Operation Specifications in 2-wire Serial Communication

Constraint	Label	Min.	Max.	Units	Comment
Communication end – Software standby	t0		One frame time (*1)	s	Until frame output
Software standby - XCLR H → L	t1	0		ns	
Falling time of internal XCLR after XCLR H → L	t2		10	μs	
VANA falling - VDIG falling - VDDL falling	t3,t4,t5	VANA, VDIG and VDDL may fall in any order.		ns	

(*1) One frame time = 1/(Frame_Rate[frame/s])

Can set fast standby mode when fast standby register (0x0106)] set to enable (0x01).
Sequence for fast standby mode;
(1) 0x0106 set to 0x01 (fast standby mode is enable)
(2) 0x0100 set to 0x00 (SW standby)
(3) Can change to SW standby after read out of current line.

To in power-off sequence varies depending on the CCI communication end timing as shown below.

1. When the CCI communication is performed with Software Standby between SOF and EOF, all communicated frame data is output and the status is converted to Software Standby.

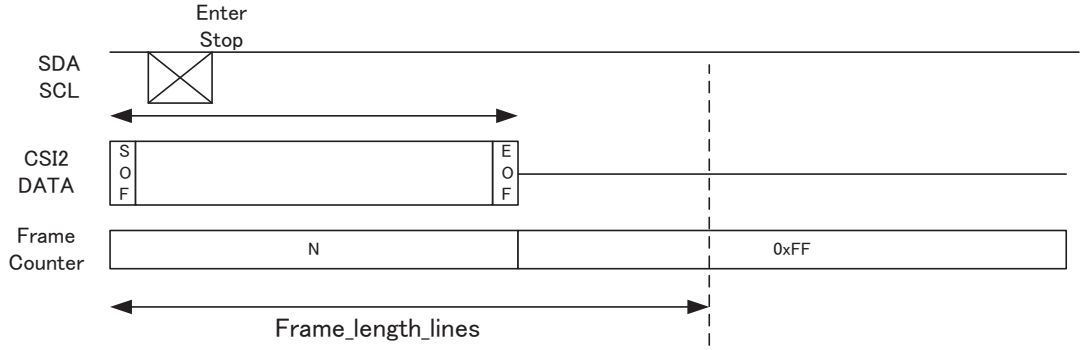

Fig. 41 Software Standby Operation Pattern 1

2. When the CCI communication is performed with Software Standby during FrameBlanking, the status is converted to Software Standby immediately after communication.

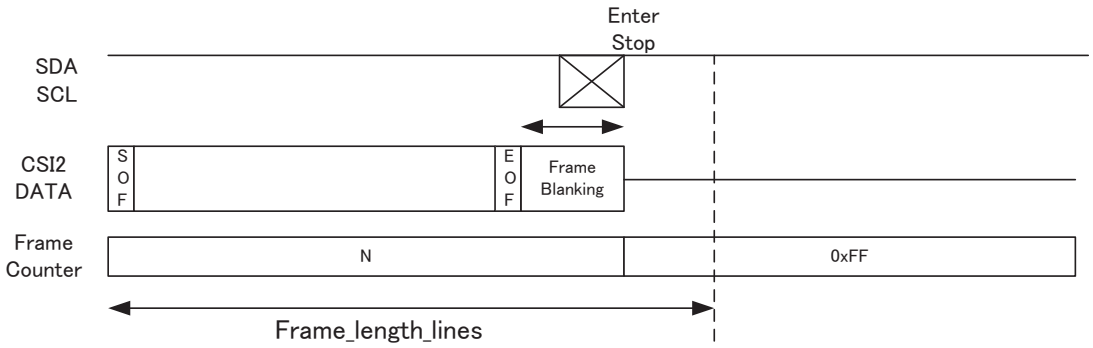

Fig. 42 Software Standby Operation Pattern 2