

# Conquering Mobile Computing Validation Challenges

## AGENDA

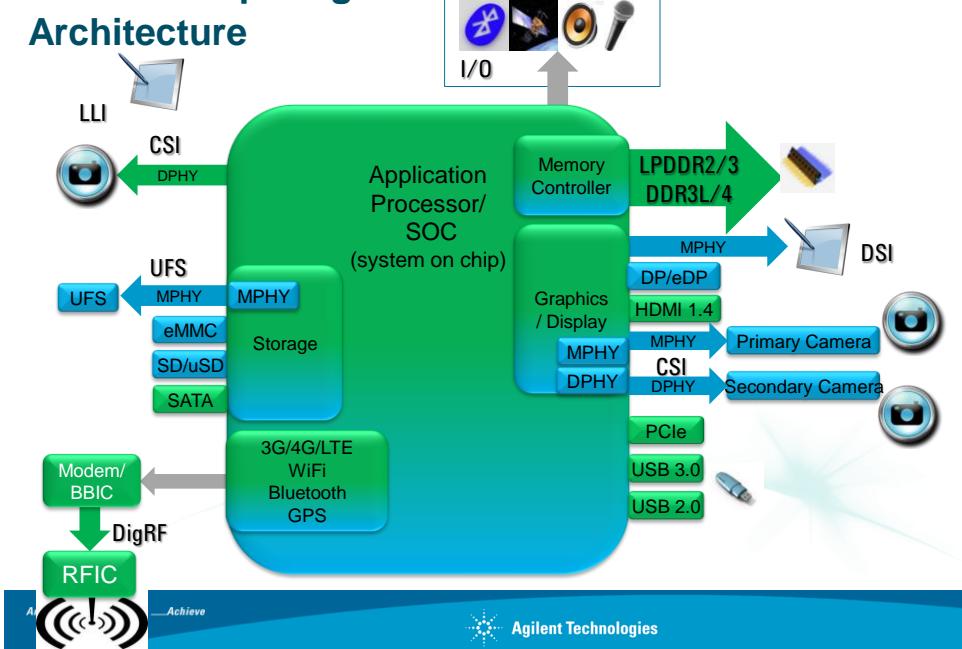
- Overview of Mobile Challenges
- LPDDR2/3 Debug and Validation Techniques
- Bringing MIPI D-PHY CSI-2 and DSI-1 Designs to Market Faster

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## Mobile Computing Architecture



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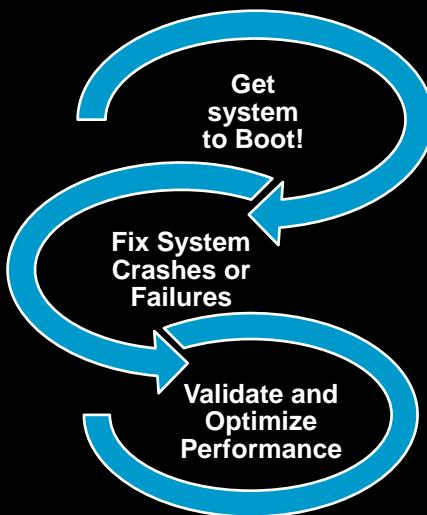
## Mobile Debug and Validation Challenges:



- Power management
  - *Saving power – sleep cycles*
- Time-to-Market
  - *Accelerate debug and validation*
- Rapidly evolving technologies
  - *Requires new probing and tools*
- Extreme space constraints
  - *Challenging probing*



## Simplified Debug and Validation Process:



## AGENDA

- Overview of Mobile Challenges
- **LPDDR2/3 Debug and Validation Techniques**
  - Overview of logic analysis for LPDDR2/3
  - Probing solutions for LPDDR2/3
  - Boot issues examples
  - System failures examples
  - System Validation and optimizing performance
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## Benefits of Logic Analysis

### Logic Analyzer Modes

**View when events happened.**  
Timing mode and Transitional Timing Modes  
Asynchronous to system under test.

### Follow what happened

State Mode  
Synchronous to clock from system  
Enables most powerful SW tools

**High resolution around trigger event.**  
Timing Zoom  
Simultaneous with State or Timing modes

### Bus Level Signal Integrity Insight – Eye Scan

Qualitative comparison of eye diagrams relative to each other

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## Benefits of Logic Analysis *continued*

**Logic Analyzer Software**

**LPDDR2/3 Specific Tools:**

- + LPDDR2/3 Decoder (Includes MRS)
- + LPDDR Compliance Toolset

Real Time & Post Process Compliance Tools  
Performance Tool & Physical Address Tool

**Trigger Macros**

- \* LPDDR specific (default configs)
- \* 21 general purpose macros

**General Purpose SW Tools:**

- \* Filter tool
- \* Colorize
- \* Hide
- \* Show

Plus many more including:

- \* Compare tool for State mode
- \* Find tool
- \* Up to 1024 global markers
- \* View Scope

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## Logic Analyzer LPDDR2/3 or DDR4 Mobile Memory Measurements

**Connect**

- Interposer for DDR4 SODIMM
- LPDDR BGA Probes
- LPDDR Mid-Bus Probing

**Acquire**

- Captures highest data rates!  
4 Gb/s
- Capture smallest eyes.  
100mV x 100ps at probe point.
- Sequential Triggers up to  
2.5GHz!

**View & Analyze**

- LPDDR Decoders
- LPDDR Protocol Compliance
- Performance Analysis
- Trigger
- Bus Level Signal Integrity Insight

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## Bus Level Signal Integrity Insight:

- Bridging a measurement gap

The slide is divided into three main sections: Design, Signal Integrity, and Functional Analysis and Validation.

- Design:** EEsof EDA tools showing a circuit board layout and simulation results.
- Signal Integrity:** Infiniium 90000 Series Scope and InfiniiMax Probes.
- Functional Analysis and Validation:** U4154A Logic Analyzer Module in M9502A Chassis, featuring 5ps x 2mV Sample position resolution.

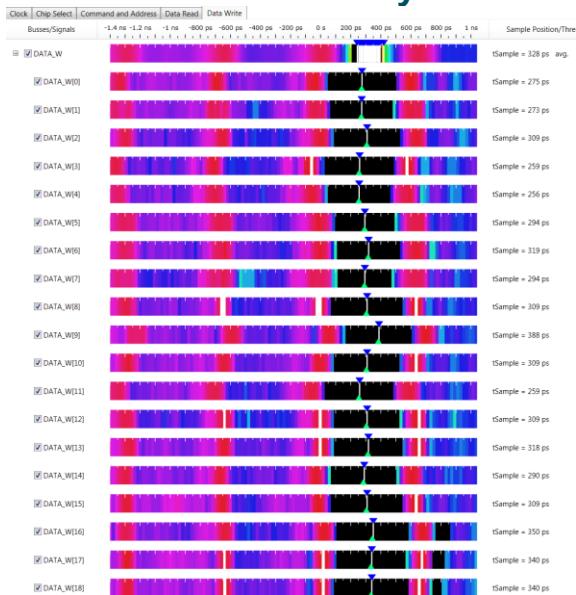
**Bus Level Signal Integrity Insight**

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## LPDDR3 1600 Write Eyefinder

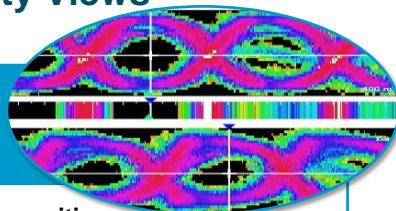


- Write eyes on LPDDR3 are time aligned ----- because all DQ are routed to one DRAM.
- Scroll through all DQ and DQS scanned under the same conditions for qualitative insight.

## Two Bus Level Signal Integrity Views

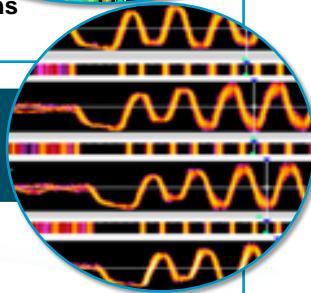
### Overlay Mode

- Required to set State mode sampling positions
- Rapid Bus level signal integrity insight



### Burst Scan Mode (Signal Trace Mode)

- Unique qualified scan views
- Simultaneous views of all DQS
- Bubble Scans



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## AGENDA



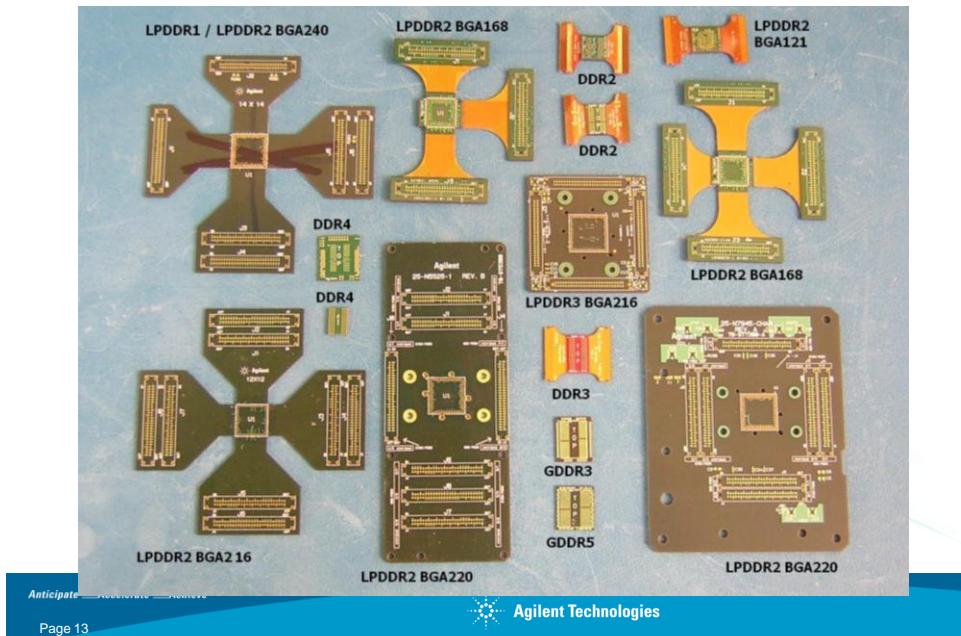
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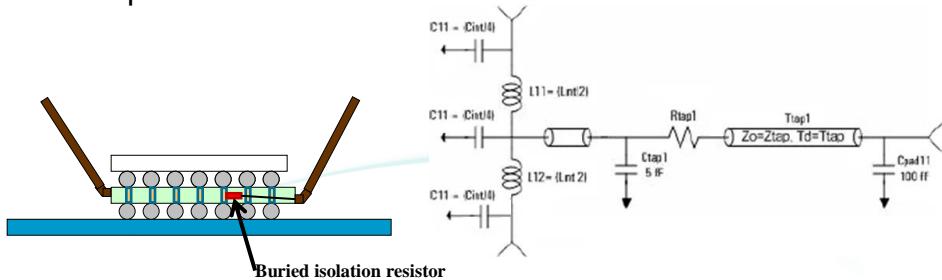
## BGA interposers examples:



## Interposer Architecture Meets Probing Challenges

### Proven architecture

- Interposer contains buried damping resistor
- For Scope - probe head connects to the interposer
- For Logic Analyzer - ZIF cable or Soft Touch Pro cable connects to the interposer
- Interposer load models for simulations



## Custom Interposer Guidelines

Construction	Best Application	Signal Count	typical Schedule	Advantages	Notes
Rigid Only 	Compliance, Solder-down scope probing	Low (<25)	8-15 weeks,	Small probe size; fastest development cycle; best SI; least expensive	Not re-usable; requires solder-down scope probes
Rigid/Flex, ZIF 	Scope (with flying leads) Logic Analyzer (with cables)	Medium (up to 24 per flex wing)	12-20 weeks,	Smallest PCB footprint, works best with existing PCB layout	Signal count limited by wing width; not re-usable; requires ZIF to 90-pin cable
Rigid, Soft Touch Pro (STP) 	Scope or Logic Analyzer; socketed DUT	Very high (up to 34 per STP) Multiple STP per wing	14-25 weeks,	Highest signal count	Re-usable; requires socket; (more board space)
Rigid/Flex/Rigid STP 	Scope or Logic Analyzer; socketed DUT or solder down	High (up to 34 per STP) One STP per wing	16-25 weeks,	High signal count	Re-usable when socketed

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## AGENDA

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## Test Tools and Techniques for Boot Challenges

**System boot Challenges:**

- \* Doesn't boot
- \* Intermittent boot
- \* Incorrect settings during boot (initialization)

**Timing Modes: Standard and Transitional**

- \* Time out triggers
- \* Timing Zoom – up to 256k deep
- \* View signal timing relationships

**State Mode**

- \* Decode Initialization
- \* Use store qualification to conserve LA memory
- \* Follow signal flow

**Compare Window to debug intermittent boot**

**Eyescans of CA and Data signals**

- \* Quickly identify abnormalities

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## Timing Modes: Standard vs. Transitional Timing w/ 1M Memory

**Buses/Signals Sampling**

**Acquisition**

Timing - Asynchronous Sampling

State - Synchronous Sampling

**Timing Options**

Sampling Options: **Full Channel, 2.5 GHz**

Sampling Period: 400 ps

Trigger Position: 99 % Poststore

Force Poststore:

Acquisition Depth: 1M

**Beginning Of Data to End Of Data = 425.72352 us**

**Buses/Signals Sampling**

**Acquisition**

Timing - Asynchronous Sampling

State - Synchronous Sampling

**Timing Options**

Sampling Options: **Transitional / Store qualified, Full channel, 2.5 GHz**

Sampling Period: 400 ps

Trigger Position: 99 % Poststore

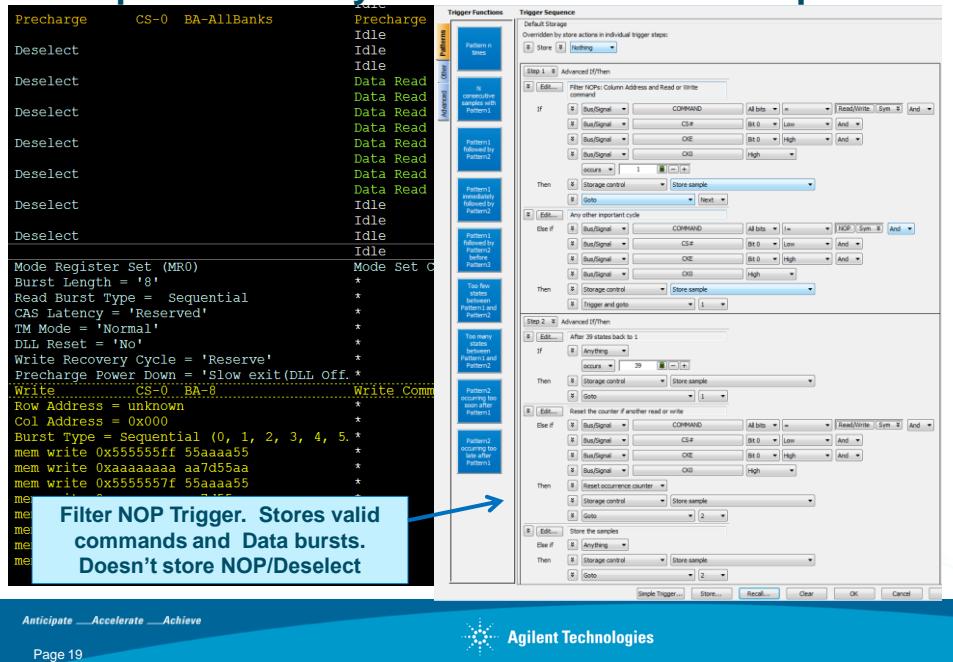
Force Poststore:

Acquisition Depth: 1M

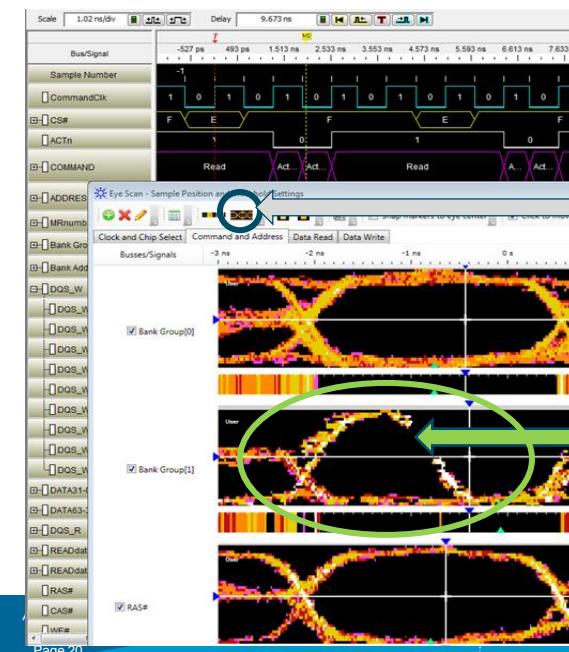
**Beginning Of Data to End Of Data = 2.1074711252 s**

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## Example # 1: Easily Follow Initialization Sequence



## Example #2: Incorrect Signal Transition



## Easily Gain

## Full Eye Scan View

- Select Full Eye Scan hot button
  - Run scan

## **Eye Scan Insight Shows**

## DDR4 Bank group 1

## Test Tools and Techniques for System Failures:

**System failures- What Happened?**  
System crashes or non-crash system failures.

Case Study #1  
High Level Views of Traffic

Case Study #2:  
Bus Level Signal Integrity Insight  
\* DQS2 Read eye collapsed

Case Study #3: Bus Level Signal Integrity.  
\* See issues with lower power

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### Case Study #1: High Level View of Traffic

#### Symptoms of case study issue:

- Actual write bandwidth on a DDR3 system was much slower than calculated BW. (*Same issue could occur on DDR4 systems.*)
- **System performance was unacceptable, the product could not ship.**
- Without a trace showing what the system was actually doing, designers were blind to the cause of the symptom.
  - Time to Market slipped away...
- The following trace showed the system beginning to write.
  - FPGA designer looked at the trace.
  - Immediately saw the root of the problem
    - **Fixed the issue quickly after seeing the traffic**

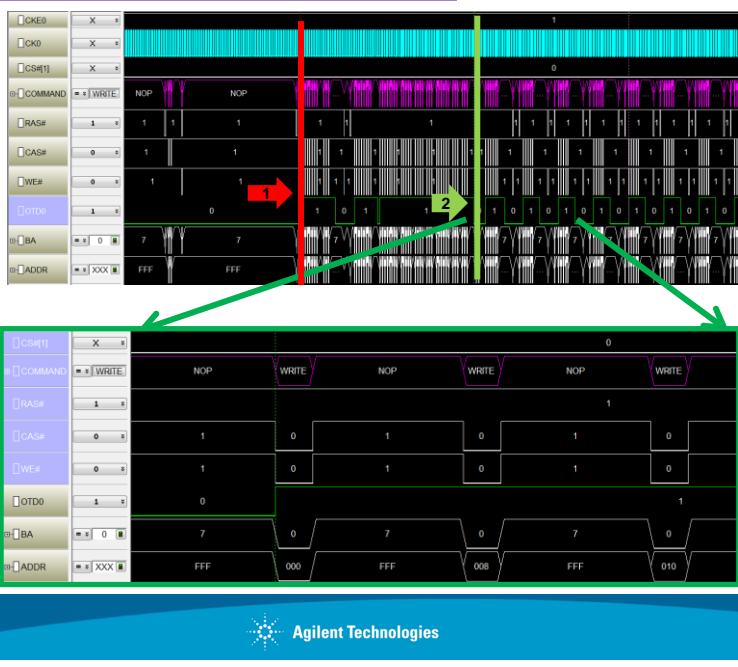


## Case Study #1: What Designer Saw

- 1) Started out streaming writes (ODT high)

- 2) Something wrong, ODT started toggling – should have been high > 90% of the time

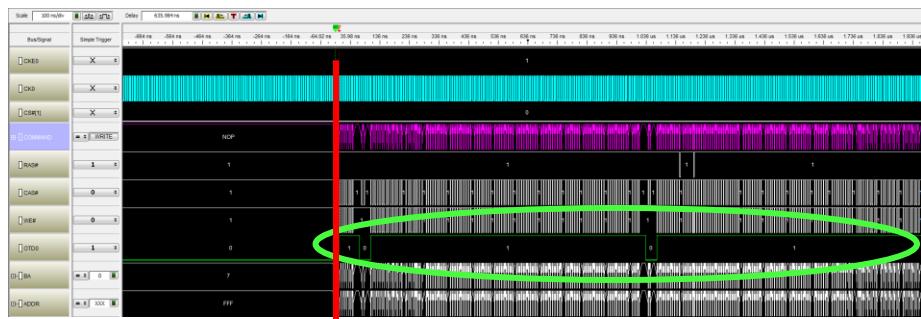
Zoom in:  
See NOP  
instead of  
streaming  
Writes



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## Case Study #1: Issue Resolved

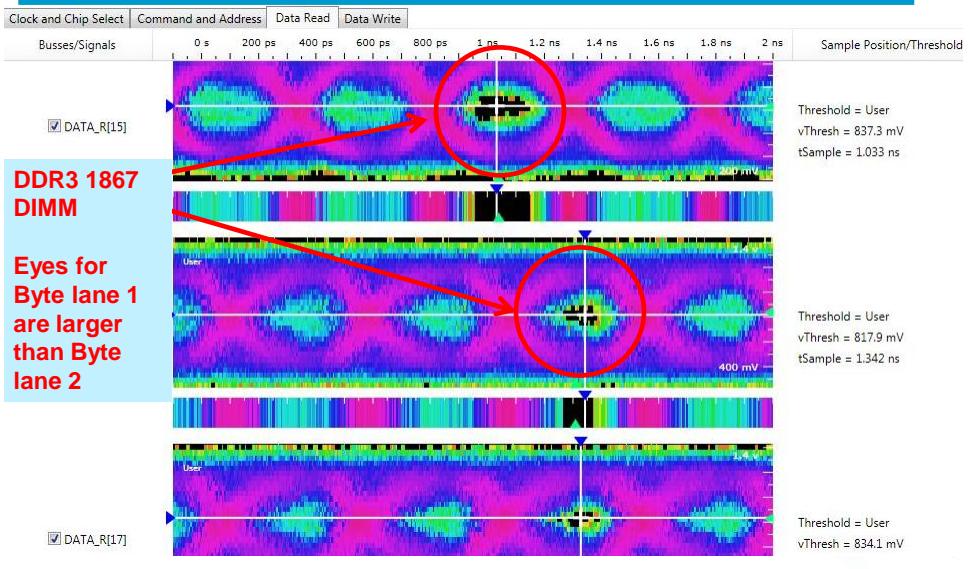


FPGA code corrected  
System Streaming Writes!

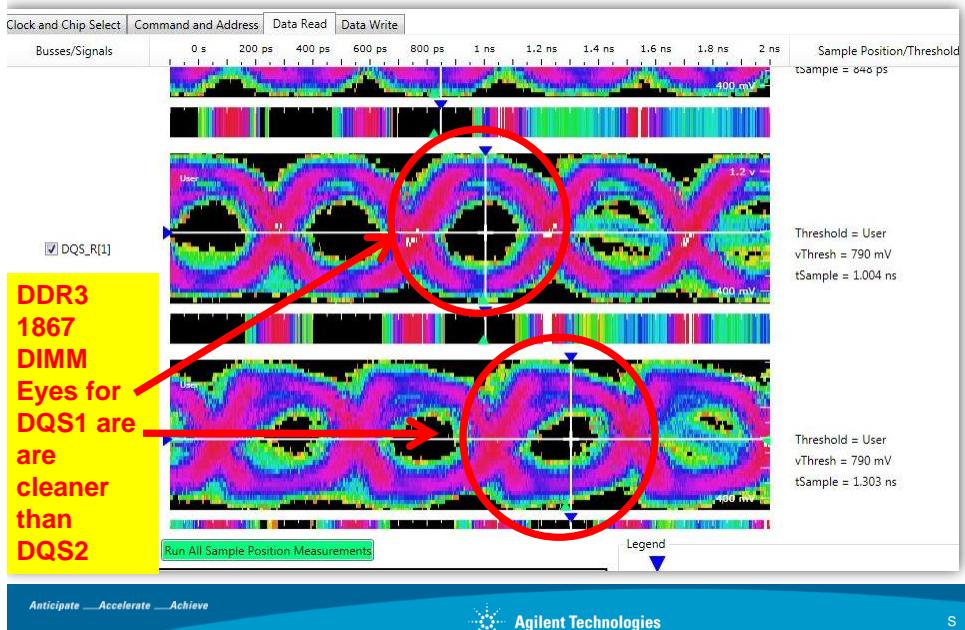
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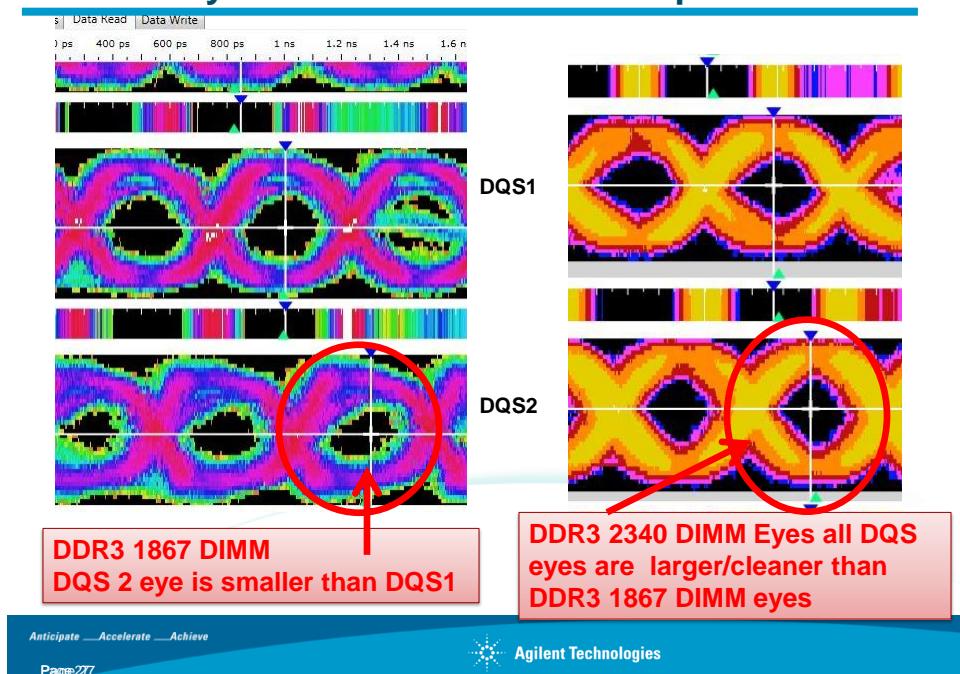
## Case Study #2: Bus Level Signal Integrity Insight



## Case Study #2: DQS2 Read Eye Collapsed



## Case Study #2: Which shows better performance?



## Case Study #3: Power savings 1.6V vs. 1.2V

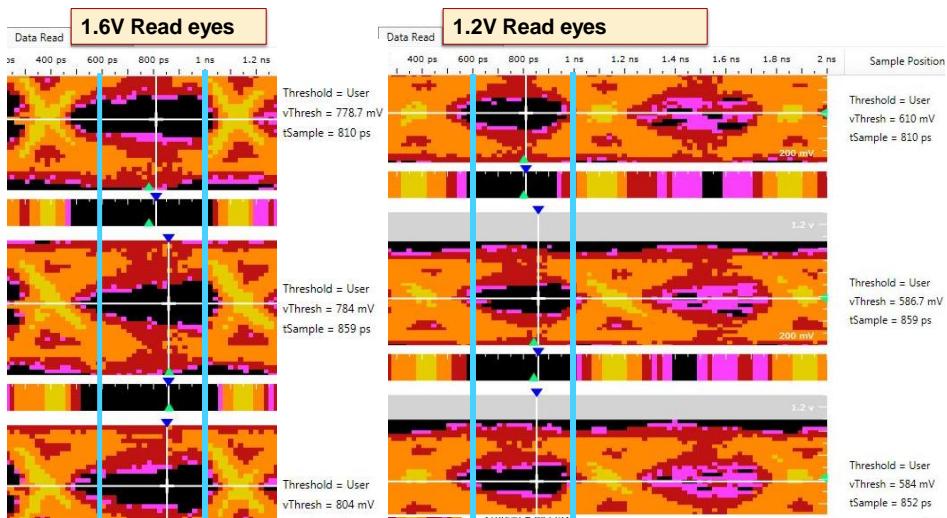


Fall time on CAS at 1.2V appears to be sluggish compared to the scan at 1.6V.



Comparing 1.6V vs. 1.2V operation of the same signals on the same system at the same data rate helps identify areas of weakness for achieving higher signal swings at lower voltages.

## Case Study #3: Read Data 1.6 V vs. 1.2 V

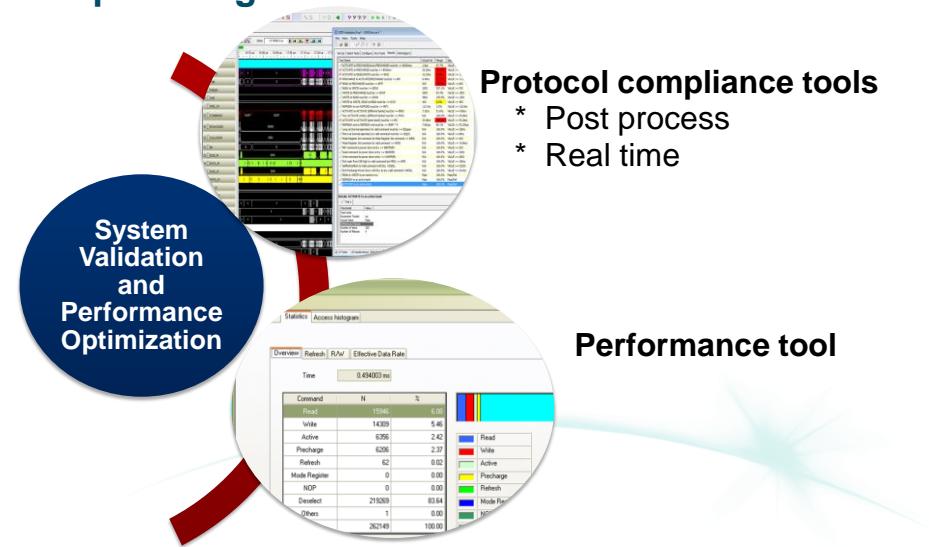


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## Test Tools and Techniques for System Validation and Optimizing Performance



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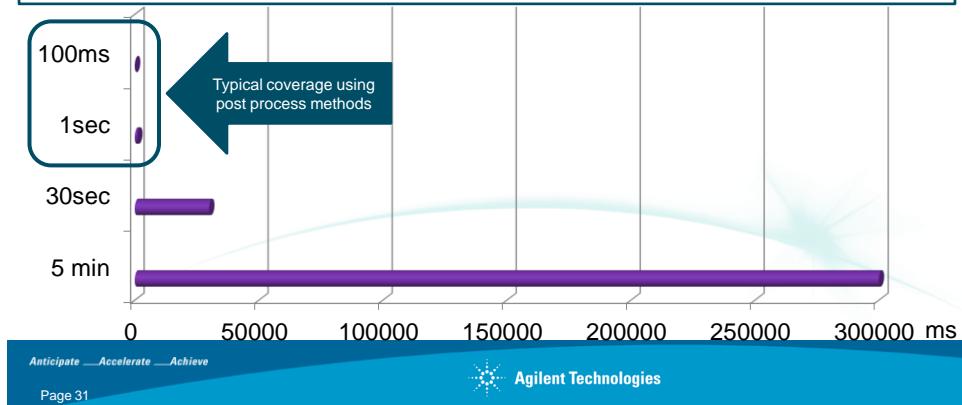
## Post Process vs. Real-Time Violation Detection

**Biggest difference:** Post process is limited to trace depth.

- Typically milliseconds to maximum of a few seconds

**Real-Time:** user selects coverage time

- seconds, minutes, hours .....



## Post Process vs. Real-Time Violation Detection ...

### Post Process Benefits

#### ... Why use if Real-Time is available?

- Quick check of Logic Analyzer trace for possible violations
- Easy method to check a trace of a system crash
- Typically optional SW tool on logic analyzer

Example:  
**Time out trigger**  
captures trace  
leading up to  
system crash

*DDR system  
stops writing to  
memory when  
system crashes*

## Post Process vs. Real-Time Violation Detection...

The screenshot shows the DDR ValidationTool interface. On the left, a logic analyzer displays multiple bus signals over time, with waveforms for CKD, CSB, CKE, OKE, COMMAND, ROWADDR, COLADDR, BA, DQS\_R, DATA\_R, DQS\_W, DATA\_W, DRW, RESET#, RAS#, CAS#, WE#, CKD, CK1, QSR, and RDYPN. A central window titled "DDR ValidationTool -- DDR Device 1" shows a table of test results. The table includes columns for Test, Actual Val, Margin, and Spec Range. Most entries are green checkmarks, except for a few red X's indicating violations. Below the table is a "Details" section for the "ACTIVATE to an active bank" test. At the bottom, status bars show "27 Tests" and "27 results shown". A callout box highlights two features:

- Post Process results example
- Run on logic analyzer trace

## Real-Time Compliance SW tool on Logic Analyzer

The screenshot shows the Real-Time Compliance Tool interface. It includes a main window for selecting logic analyzer modules and running tests, and a detailed customization dialog for DDR3 specifications. The customization dialog lists parameters like tRASMin, tRASMax, tRCD, and tRP. A yellow box highlights the "Edit Parameters..." button. Another yellow box points to a table where values for target speed and CAS latency are listed. A third yellow box points to a note about overriding tRCD and tRP. Callout boxes explain these features:

- Select technology
- Edit Parameters
- Load Data Rate tests
- Create custom tests
- Select time to run

**Customization Details:**

The values of any of the listed DDR3 specification parameters can be overridden. Enter all values as an integer representing twice the number of clocks (CKD) (This is because there are two logic analyzer states per clock).

For example, to set a parameter to 10 clocks, enter a value of 20.

**View details on specific violations.**

**Option to customize specific violations.**

NOTE that for all defined combinations of target speed and CAS latency, tRCD and tRP are simply equal to the CAS latency.

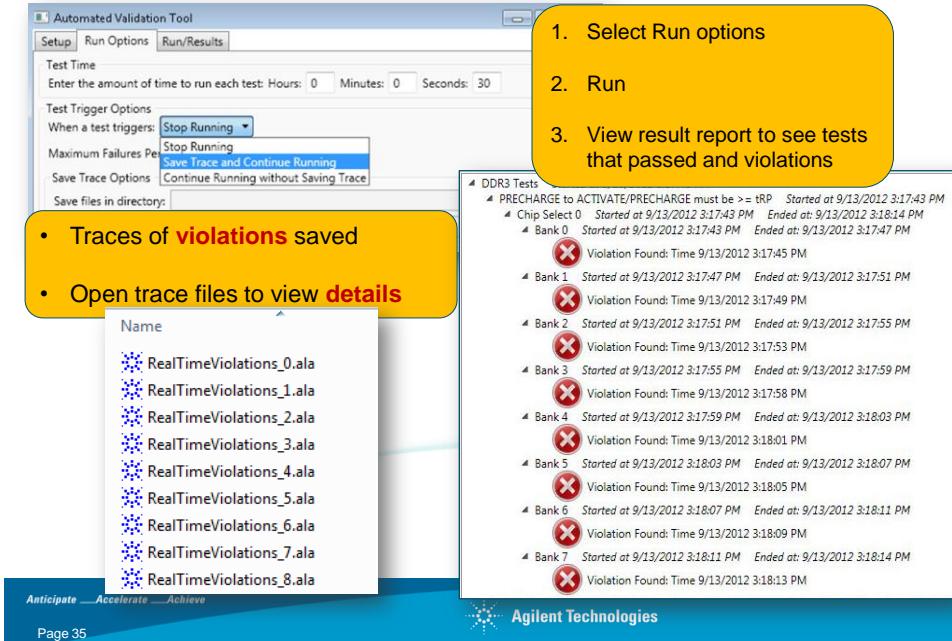
To override this setting, either apply the appropriate test group parameter values file, or manually override the value below. The default choice here is for a CAS latency of 14 at 2133MHz.

Default value: 28

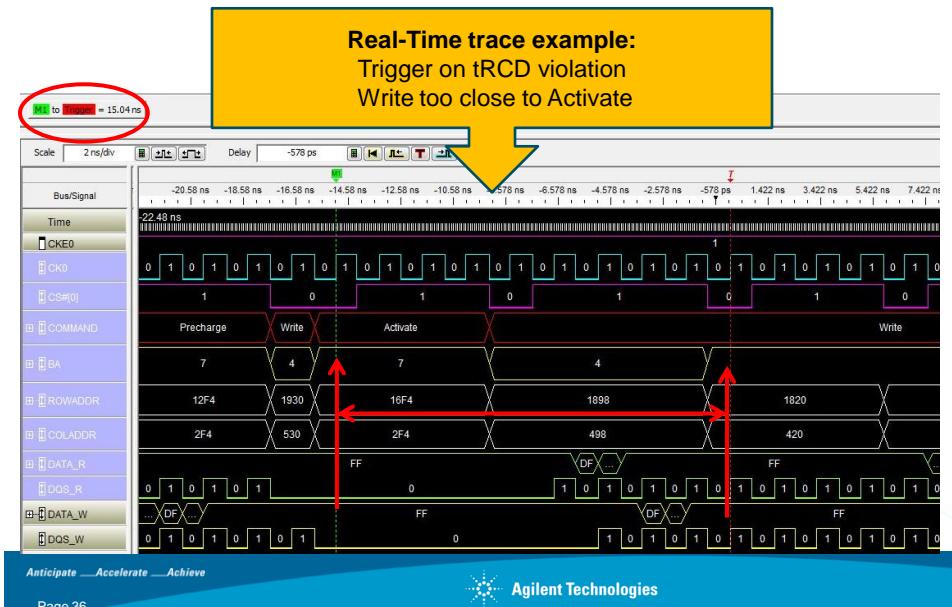
Manually override value of tRCD and tRP

(Enter value for tRCD and tRP (in LA states): 28)

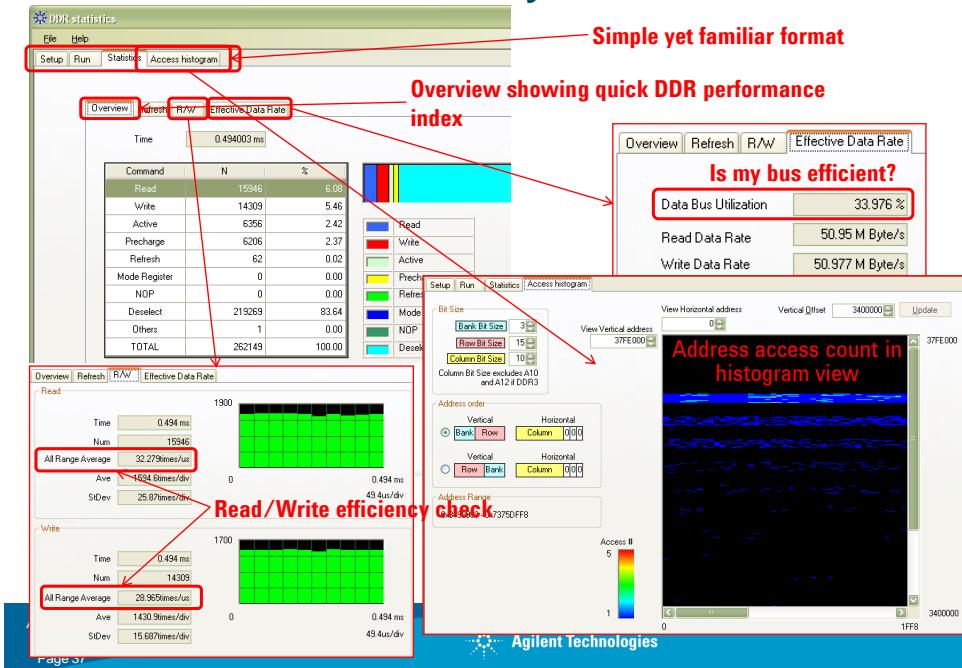
## Real-Time Compliance SW tools on Logic Analyzer



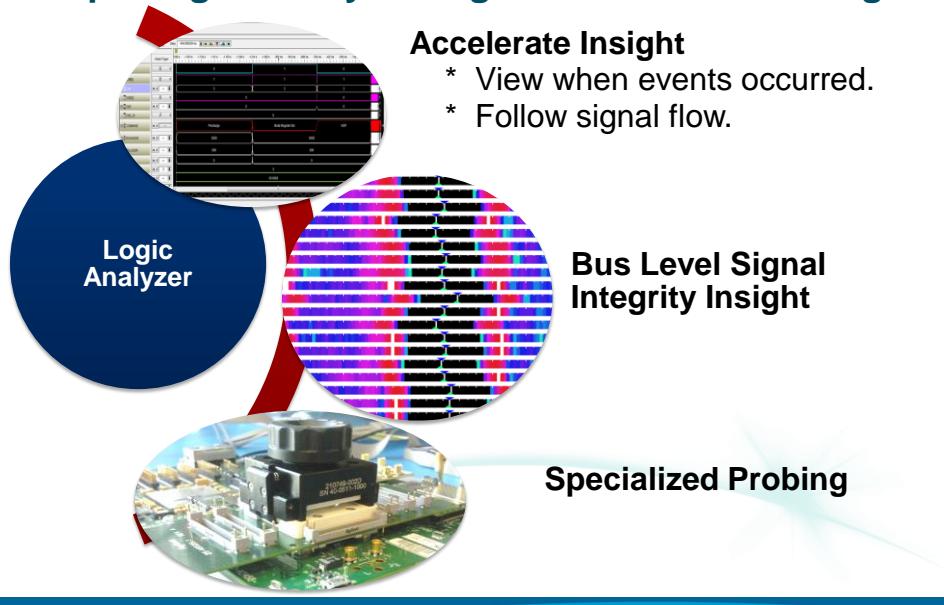
## Real-Time Compliance SW tools on Logic Analyzer



## B4622B: Performance Analysis Tool



## Conquering Memory Debug & Validation Challenges



## Simplified setup with DDR Setup Assistant

### Tune LPDDR State Mode measurements in minutes

The screenshot shows the 'DDR Setup Assistant' software interface. At the top, it says 'Setting up: DDR 4 -> DIMM Interposer -> FS2501'. Below this, there's a list of steps: 'Specify Input Parameters' (which is checked), 'Verify Software Installation', 'Load Configuration File', 'Do Hardware Setup', 'Set Initial Thresholds', 'Set Sample Positions of Clk/CS Signals', 'Set Sample Positions of Command/Addr Signals', 'Find Latency Values', 'Set Sample Positions of Data Read/Write', and 'Save Setup'. A red box highlights the first step, 'Specify Input Parameters'. To the right of the list, there are dropdown menus for 'Which logic analyzer module will you be using?' (set to U4154A-1), 'What is the DDR bus type?' (set to DDR 4), 'What probing solution are you using?' (set to DIMM Interposer), and 'DIMM Interposer Model Number' (set to FS2501). A callout box on the right says 'Easily and quickly' with three bullet points: 'Input your system parameters', 'Make selections', and 'Connect cables.' Another callout box below says 'Complete View of LPDDR traffic including simultaneous R/W DATA' with three bullet points: 'Accurate', 'Reliable', and 'Repeatable'. At the bottom of the software window, there are 'Completed -->' and 'Skip This Step -->' buttons.

**Easily and quickly**

- Input your system parameters
- Make selections
- Connect cables.

**Complete View of LPDDR traffic including simultaneous R/W DATA**

- Accurate
- Reliable
- Repeatable

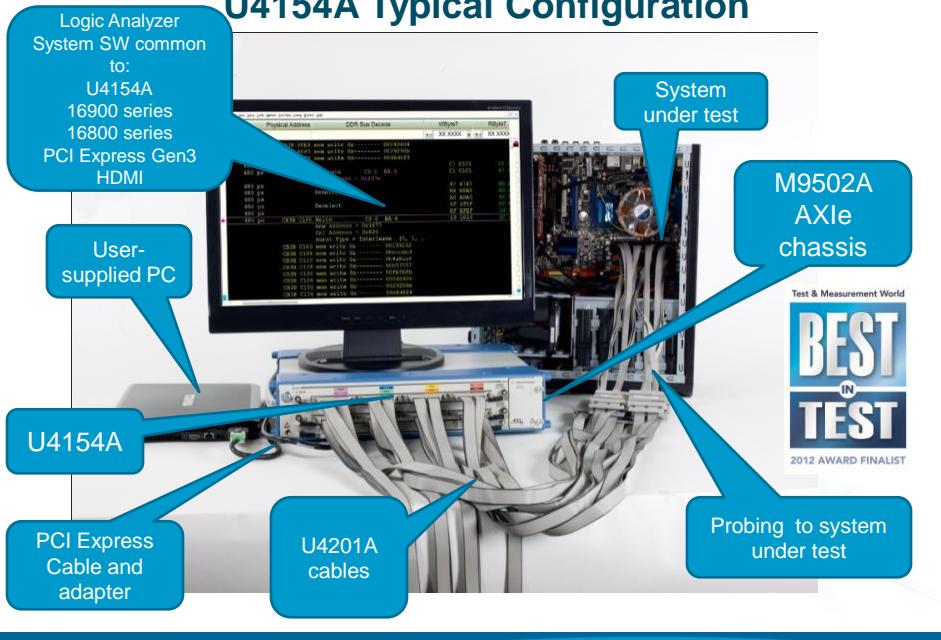
10 simple semi-automated steps

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## U4154A Typical Configuration

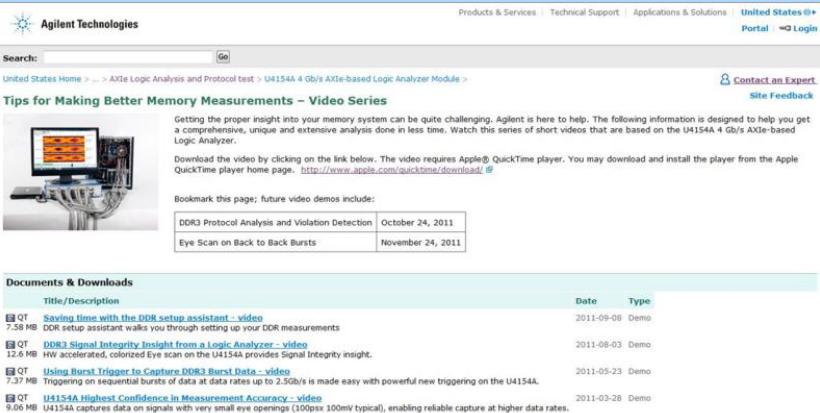


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**For video Demo series:**  
[www.agilent.com/find/logic-analyzer-videos](http://www.agilent.com/find/logic-analyzer-videos)



The screenshot shows the Agilent Technologies website with a search bar and navigation links for Products & Services, Technical Support, Applications & Solutions, United States Portal, and Login. A banner at the top says "For video Demo series: www.agilent.com/find/logic-analyzer-videos". Below it, a section titled "Tips for Making Better Memory Measurements – Video Series" features a thumbnail of a logic analyzer setup. Text explains that getting proper insight into memory systems can be challenging, and Agilent provides short videos for the U4154A 4 Gb/s AXIe-based Logic Analyzer Module. It includes links for "DDR3 Protocol Analysis and Violation Detection" (October 24, 2011) and "Eye Scan on Back to Back Bursts" (November 24, 2011). A "Documents & Downloads" section lists several video files with their titles, sizes, dates, and types.

**Test & Measurement World**  
**BEST IN TEST**  
2012 AWARD FINALIST

To learn more about the U4154A logic analyzer go to:  
[www.agilent.com/find/U4154A](http://www.agilent.com/find/U4154A)

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# Conquering Mobile Computing Validation Challenges

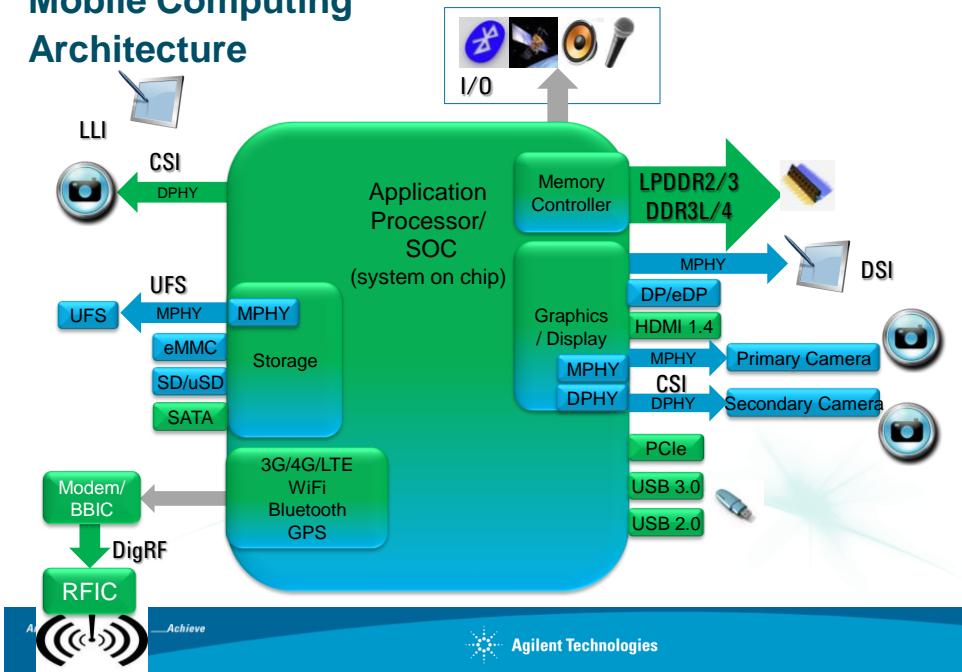
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## Mobile Computing Architecture



## Scope of this discussion

### Mobile Computing

### D-PHY Protocols

- D-PHY Layers
- Signaling and Traffic
- HS and LP Modes
- D-PHY States
- CSI and DSI idiosyncrasies

### Early view of MIPI M-PHY

### Demonstration of D-PHY Protocol Tools

Demand is shifting from client /laptop devices to smart devices.

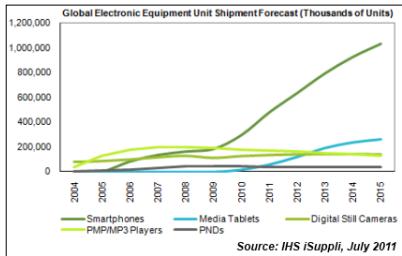
Meanwhile, laptop devices will start to look more like smart devices.

– PC demand is flattening

and moving to mobile computing

PC Shipment Growth by Region and Form Factor, 2010-2015							
Region	Form Factor	2010	2011*	2012*	2013*	2014*	2015*
Mature Markets	Desktop PC	3.2%	-4.9%	2.1%	-2.7%	-2.0%	-0.1%
Mature Markets	Portable PC	8.5%	-3.2%	10.7%	9.0%	11.0%	8.8%
Mature Markets	Total PC	6.6%	-3.7%	7.8%	5.2%	7.1%	6.3%
Emerging Markets	Desktop PC	9.8%	-4.3%	4.8%	3.9%	2.6%	2.2%
Emerging Markets	Portable PC	34.7%	18.2%	18.6%	21.0%	21.6%	20.5%
Emerging Markets	Total PC	21.3%	11.5%	12.2%	13.7%	14.2%	14.1%
Worldwide	Desktop PC	7.1%	0.8%	3.6%	1.4%	1.0%	1.4%
Worldwide	Portable PC	19.1%	6.7%	14.7%	15.2%	15.0%	15.5%
Worldwide	Total PC	13.7%	4.2%	10.2%	10.0%	11.3%	11.0%

Source: IDC Worldwide Quarterly PC Tracker, May 2011



*"The cloud computing market is heading into the stratosphere as companies seek to offer services designed to serve tablets, smartphones and other mobile devices. ... projected to surge to \$110 billion in 2015, up from \$23 billion in 2010."*

iSuppli December 22, 2011



## MIPI Layered Protocols



Application



Protocol Standard



Physical Standard

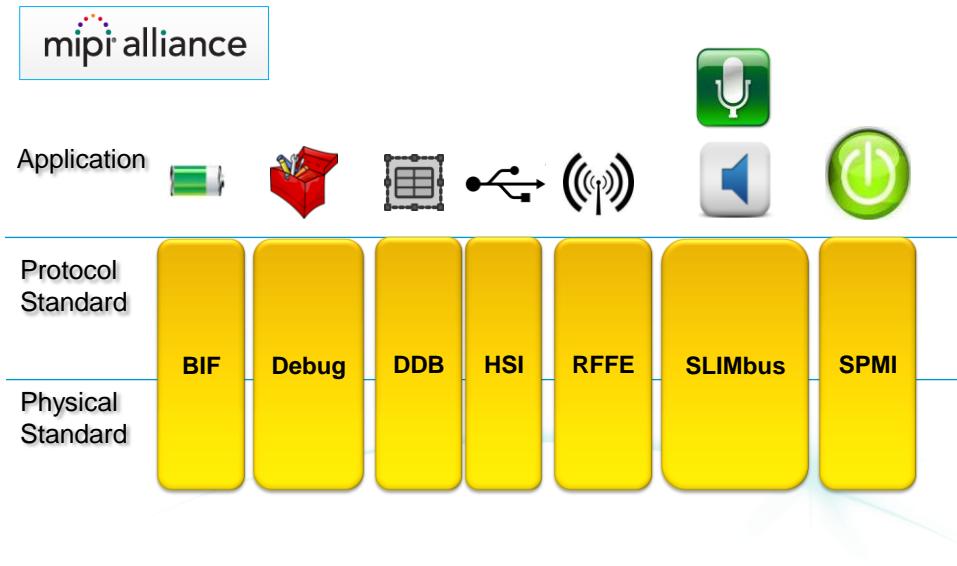


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## MIPI Monolithic Protocols & Applications



## About the MIPI Alliance



**Coordinate technology across the mobile computing industry**

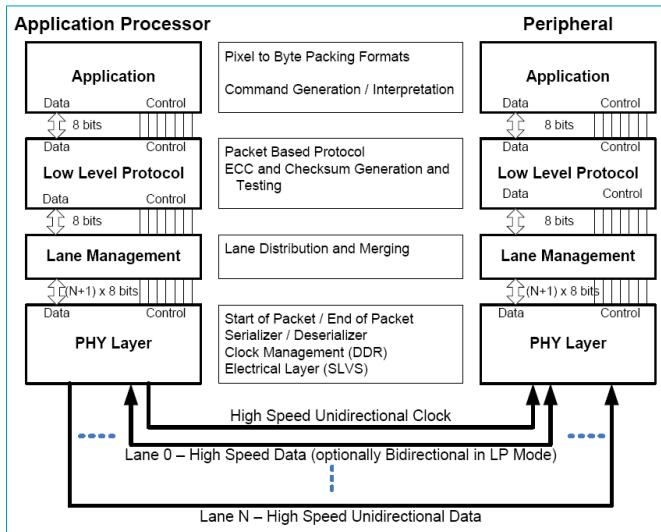
- Over 240 member companies
- 100% penetration of MIPI specs in smartphones by 2013

**Develop specifications that ensure a stable, yet flexible technology ecosystem**

- 17 official working groups (14 active) and growing
- Partnerships with other industry organizations (JEDEC, USB-IF, Open Mobile Alliance, 3GPP, MEMS, etc.)
- Only members have access to specifications
- All members can participate and vote in discussions; higher levels of membership required to lead.



## D-PHY layers (DSI example)



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## D-PHY Signaling Highlights

1-4 Data Lanes (trying to push the spec to x8)

- 1 lane clock for all data lanes

2 types of signaling LP and HS

- LP P & N signals are driven independently
- HS is differentially driven

Primarily a unidirectional link

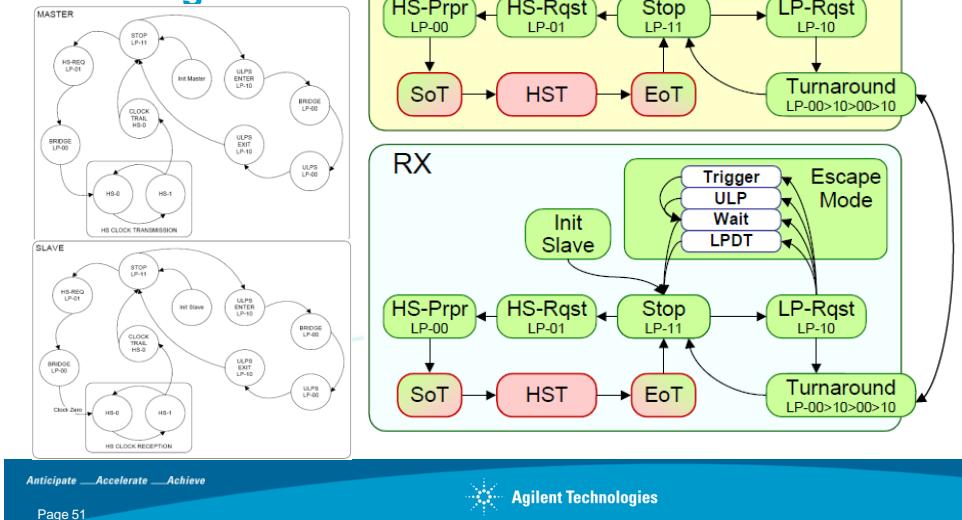
Can get reverse communication through a Bus Turn Around (BTA) for DSI

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## D-PHY Global Operation Flow Diagram



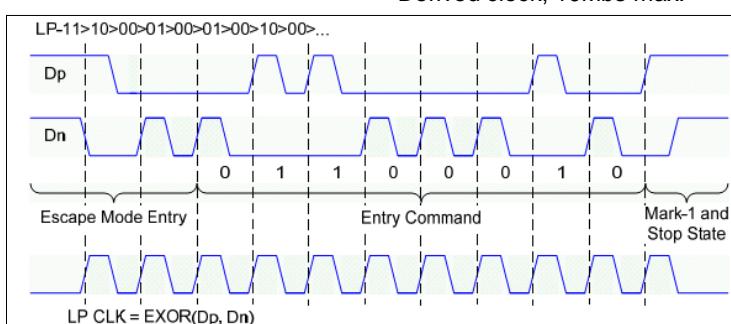
## D-PHY Low Power Signaling

### LP Control

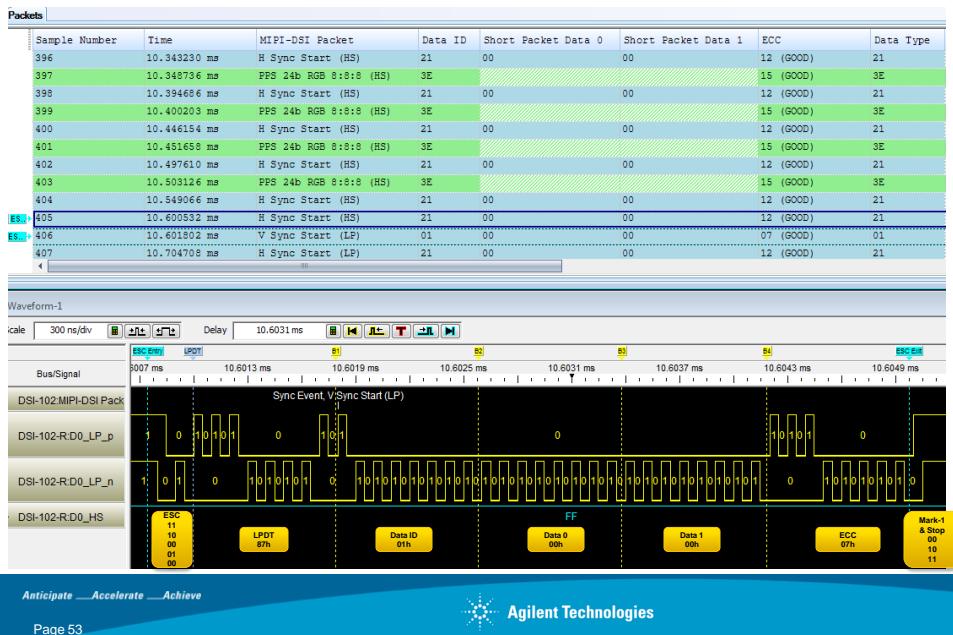
- 1.2V Nominal
- Stop state LP-11
- Escape Mode & HS Mode Entry/Exit
- Bus Turnaround (BTA), [DSI]

### Escape Entry Codes

- Trigger/Modes (generic protocol messaging)
  - Ultra Low Power (ULP – 78h)
  - Low Power Data Transmission (LPDT – 87h)
  - Derived clock, 10Mbs max.
- } Binary opposites

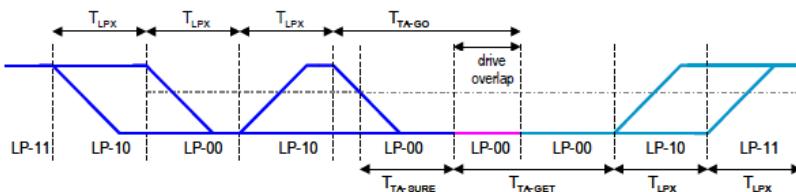


## High-speed to Low-power transitions in action



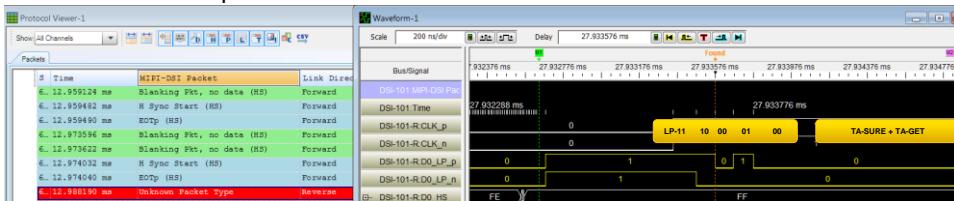
## Bus Turnaround Procedure

- Only used on DSI
- Restricted to LP mode
- One lane only

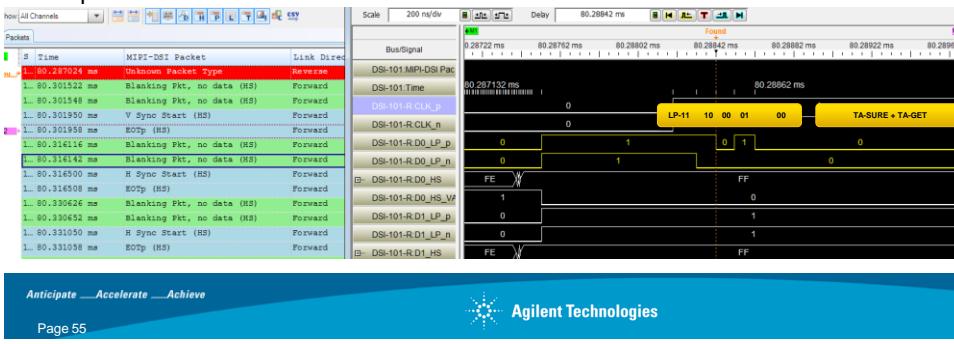


## BTA in action

### Processor to Peripheral

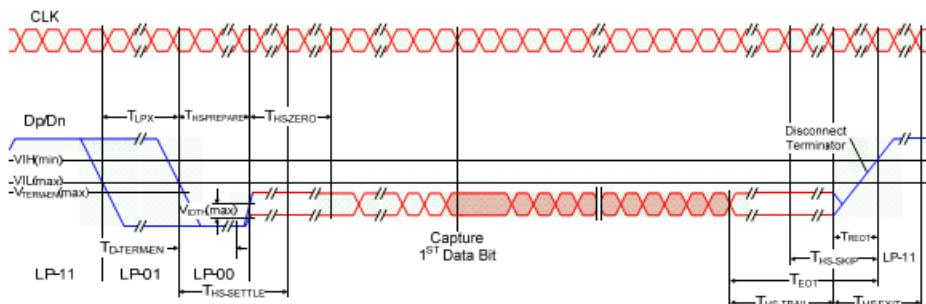


### Peripheral to Processor is identical

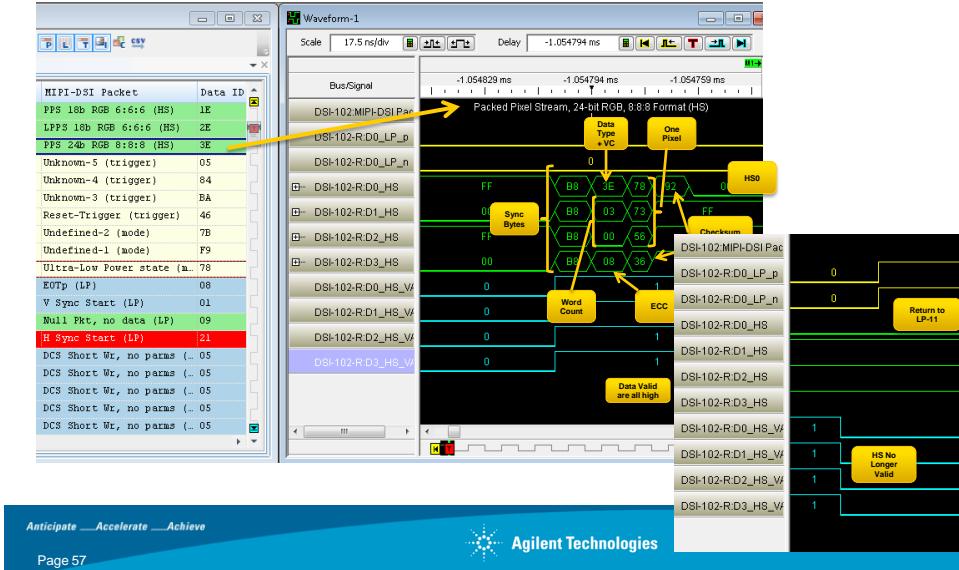


## D-PHY High Speed Signaling

- Source-synchronous clocking, dual data rate
- Differential 200mV Nominal, Common Mode 200mV, nominal
- 80Mbs to 1.5Gbs (clock rates from 40MHz to 750MHz)
- Used for payload transmission



## HS Burst in action



## ECC error correction (both short and long packets)

Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the **Packet Header**.

- Includes both the Data Identifier and Word Count fields
- Hamming Code
  - Detects 2-bit errors
  - Recover 1-bit errors

## Checksum (long packets only)

### Payload portion of long packets

#### Functionality:

- 16-bit field (covers 64k payload)
- Can only indicate the presence of one or more errors in the payload.
- Cannot be used to correct errors.

#### Usage:

- Mandatory for processor to peripheral communication (DSI).
- Optional for peripheral to processor. If not used, “0000h” checksum must be sent.
- If the payload length is 0, checksum is “FFFFh”



## Packet Formats

### Short Packets:

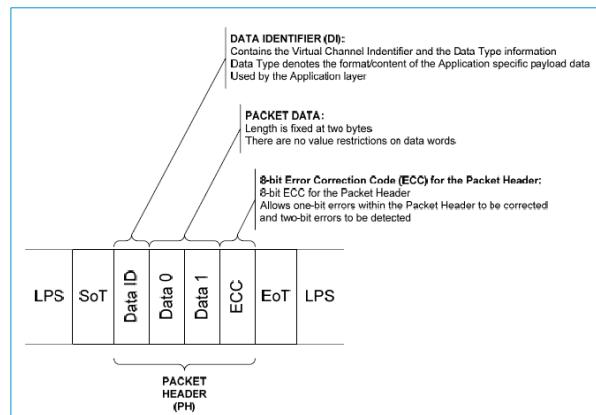
- 4-byte packets

### Data Identifier lists different types of packets:

- Sync Events
- EoT
- Commands
- Generic Short Writes
- Generic Short Reads
- Short DCS command data (DSI)
- ACKs and Error Reports

Can be HS or LP

Many codes are reserved for future use



## Packet Formats

### Long Packets:

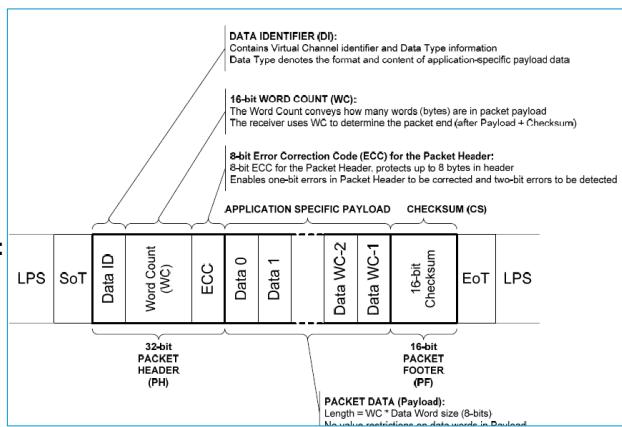
- 4-byte header
- Up to 64k byte payload
- Word Count identifies length.

### Data Identifier lists different types of packets:

- Blanking
- Generic Long Writes
- Image Data
- DCS command data (DSI)
- Response from Peripheral (DSI)

Can be HS or LP

Many codes are reserved for future use



## Example: DSI Packets

Data Type, hex	Data Type, binary	Description	Packet Size	Data Type, hex	Data Type, binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short	24h	10 0100	Generic READ, 2 parameters	Short
11h	01 0001	Sync Event, V Sync End	Short	05h	00 0101	DCS WRITE, no parameters	Short
21h	10 0001	Sync Event, H Sync Start	Short	15h	01 0101	DCS WRITE, 1 parameter	Short
31h	11 0001	Sync Event, H Sync End	Short	06h	00 0110	DCS READ, no parameters	Short
08h	00 1000	End of Transmission (EoT) packet	Short	37h	11 0111	Set Maximum Return Packet Size	Short
02h	00 0010	Color Mode (CM) Off Command	Short	09h	00 1001	Null Packet, no data	Long
12h	01 0010	Color Mode (CM) On Command	Short	19h	01 1001	Blanking Packet, no data	Long
22h	10 0010	Shut Down Peripheral Command	Short	29h	10 1001	Generic Long Write	Long
32h	11 0010	Turn On Peripheral Command	Short	39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
03h	00 0011	Generic Short WRITE, no parameters	Short	0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
13h	01 0011	Generic Short WRITE, 1 parameter	Short	1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
23h	10 0011	Generic Short WRITE, 2 parameters	Short	2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
04h	00 0100	Generic READ, no parameters	Short	3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
14h	01 0100	Generic READ, 1 parameter	Short				

## Example: CSI Packets

Data Type	Description	Data Type	Description
0x00 – 0x07	Synchronization Short Packet Data Types	0x00	Frame Start Code
0x08 – 0x0F	Generic Short Packet Data Types	0x01	Frame End Code
0x10 – 0x17	Generic Long Packet Data Types	0x02	Line Start Code (Optional)
0x18 – 0x1F	YUV Data	0x03	Line End Code (Optional)
0x20 – 0x27	RGB Data	0x04 – 0x07	Reserved
0x28 – 0x2F	RAW Data		
0x30 – 0x37	User Defined Byte-based Data		
0x38 – 0x3F	Reserved		



## CSI-2 Particulars

### CCI – Camera Control Interface

- I2C subset used to configure camera interface (instead of BTA)
  - CCI is the protocol layer
  - Multiple-devices, single controller
- No BTA

### Only HS transmissions

### Simple Low-Level Protocol packet formats

- Long** – for transmitting Application Specific Payload data
- Short** – for transmitting Frame and Line synchronization data, and other image-related parameters.

**Virtual Channel** – independent data stream for one of up to four peripherals

### 1 packet per HS frame

- Frame Start/ Frame End
- Optional Line Start/ Line End
- LP State between frames



## DSI Particulars

**LPDT (on D0 only)**

**Low-power burst**

**Greater variety of packet types**

- Short packets
- Long packets
- Processor commands (BTA)
- Great variety of image traffic
  - Burst (asynchronous)
  - Non-burst (synchronous, with and without sync events)
  - Display commands



## Pixel Stream Types

**CSI**

RGB888

RGB666

RGB565

RGB555

RGB444

YUV422

YUV420

RAW 6/7/8/10/12/14

**DSI**

RGB 12-12-12

RGB 10-10-10

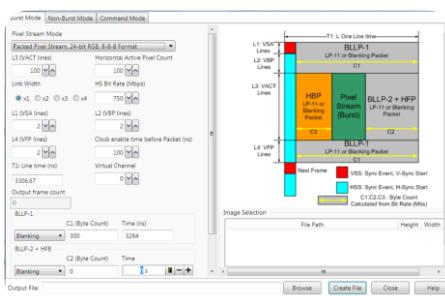
RGB 8-8-8

RGB 6-6-6

RGB 5-6-5

YCbCr 4-2-2

YCbCr 4-2-0



## Common pitfalls

### Seldom related to signal integrity

## Protocol timing

- Capturing data during settling time
  - BTA collisions
  - Adapting to bus speed changes

## Lane misalignment

## Non-burst image synchronization



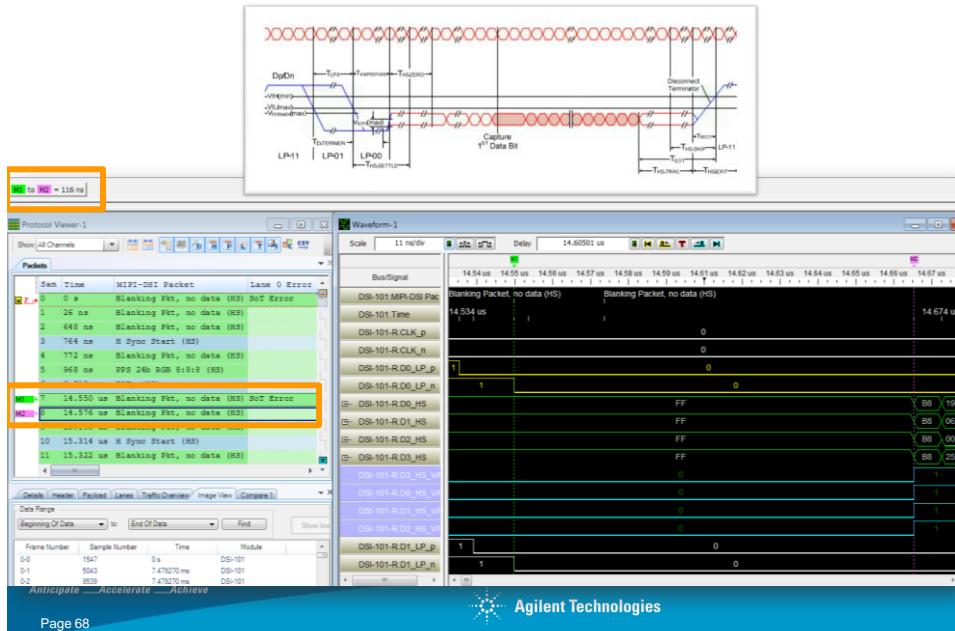
## Mitigation

- Intimate specification knowledge
  - Corner case testing
  - Protocol “omniscience”



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## Example: Start of Transmission timing error



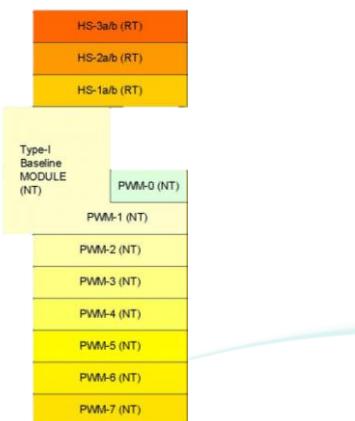
## Look ahead at M-PHY

	D-PHY	M-PHY
Minimum configuration	1-way or half-duplex CLK + DATA (4 pins)	dual-simplex DATA (4 pins)
Min. pins for 6 Gbps	10	4 (Gear 3)
Data rate per lane	HS: 80 Mbps to 1.5 Gbps LP: <10 Mbps	HS: ~ 1.25/1.5; 2.5/3.0; 5/6 Gbps LP: 10k-600Mbps
Electrical signaling	HS LP	SLVS-200 LVCMOS1.2V
HS Clocking method	DDR Source-Sync Clk	Embedded
HS Line coding	None or 8b/9b	8b/10b
Power – Energy/bit	Low	Lower (YMMV)
Repeater/optical	No	Yes
LP only PHY's	Disallowed	Allowed



## Power Saving

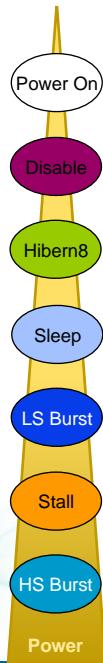
### Variable Gear Rates



### Power Saving Modes

State	Recovery Latency	~ Power
HIBERN8	0.1 – 1ms	10uW
Sleep	μs	100uW
LS Burst		1mW
Stall	ns	10mW
HS Burst		25mW

MIPi estimate for one M-TX and one M-RX  
including clock multiplication – v1.0



## M-PHY Introduces a Transport Layer

### Transport Layer

- Logical multiplexing of several communication channels (CPorts)
- E2E Flow Control

### Network Layer

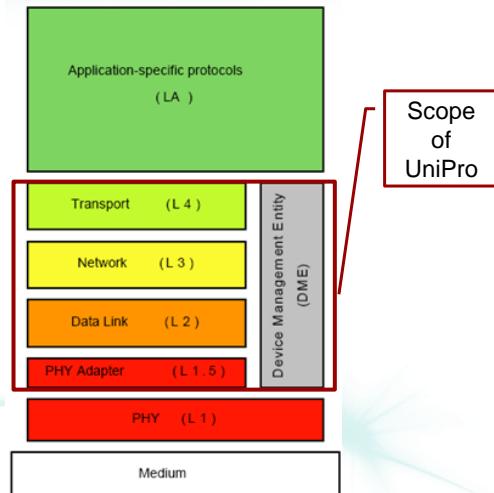
- Fully compatible with future Switched Network

### Data Link Layer

- Link reliability
- Traffic Classes (TC0/TC1)

### PHY Adapter Layer

- Abstraction of M-PHY
- Lane Discovery, downgrading
- Link Configuration (#lanes, gear etc.)
- Handling of multiple LANEs
- Native support for OMC



Anticipate Accelerate Achieve

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Agilent Technologies

## Agilent U4421A MIPI D-PHY Protocol Exerciser/Analyzer

Two instruments in one module



**Opt 601**  
MIPI D-PHY Analyzer  
See ALL system behavior

Fully protocol-aware  
Performance for today and tomorrow

- Up to 1.5Gb data rate
- Up to 16GB trace depth
- 1-4 data channels + CLK

“Raw” view of state traffic for additional insight

Flexible probing options

Integrated image extraction

**Opt 602**  
MIPI D-PHY Exerciser  
Characterize and Optimize

Generate user-defined D-PHY traffic  
Change speed, slew rate, voltage levels and lane skew

Flexible pattern creation

- GUI
- Packet inserter
- Image inserter

High-bandwidth SMA cables

Anticipate Accelerate Achieve

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