Assumption : The values on CDB are used by the other registration stations in the same clock cycle

Instruction	Issue	ROB/ResStat	FU/EX	MEM	CDB	Commit
MUL.D F1,F2,F3	1	#1/FMUL1	FM1/2-6	--	7	8
L.D F2,8(R1)	1	#2/LD1	A1/2-2	3	4	8
S.D F2,32(R2)	1	#3/ST1	A2/2-2	--	--	8
LW R3,48(R1)	1	#4/LD2	A1/3-3	4	5	8
L.D F3,0(R1)	5	#5/LD1	A1/6-6	7	8	9
ADD.D F4,F3,F1	5	#6/FAD1	FA1/8-10		11	12
DIV.D F5,F2,F11	5	#7/FMUL2	FM1/8-15		16	17
DADDIU R1,R1,#8	5	#8/ ALU1	A2/8-8		9	17
LW R5,0(R2)	9	#1/LD1	A1/10-10	11	12	17
BNE R1,R5,LAB1	9	#2/BR1	BU/12-12	--	12	17
SUB.D F6,F1,F2	9	#3/FAD2	FA2/10-12	--	13	18
MUL.D F7,F2,F6	9	#4/FMUL1	FM1/16-20	--	21	22
S.D F7,0(R8)	10	#5/ST1	A2/21-21	--	--	22

Explanation for Assumption:

In the above chart, the value of F3 is available on the data bus in the 8^{th} cycle(from L.D F3, 0(R1)) and we are using this value required by ADD.D F4,F3,F1 in the same cycle i.e. we are assuming the addition starts in the same cycle.

In the next chart, we assume that the addition started from next cycle and hence the difference.

Assumption : The values available on the common data bus are available after one cycle

Instruction	Issue	ROB/ResStat	FU/EX	MEM	CDB	Commit
MUL.D F1,F2,F3	1	#1/FMUL1	FM1/2-6	--	7	8
L.D F2,8(R1)	1	#2/LD1	A1/2-2	3	4	8
S.D F2,32(R2)	1	#3/ST1	A2/2-2	--	--	8
LW R3,48(R1)	1	#4/LD2	A1/3-3	4	5	8
L.D F3,0(R1)	5	#5/LD1	A1/6-6	7	8	9
ADD.D F4,F3,F1	5	#6/FAD1	FA1/9-11	--	12	13
DIV.D F5,F2,F11	5	#7/FMUL2	FM1/8-15	--	16	17
DADDIU R1,R1,#8	5	#8/ ALU1	A2/9-9	--	10	17
LW R5,0(R2)	9	#1/LD1	A1/10-10	11	12	17
BNE R1,R5,LAB1	9	#2/BR1	BU/13-13	--	14	17
SUB.D F6,F1,F2	9	#3/FAD2	FA2/10-12	--	13	18
MUL.D F7,F2,F6	9	#4/FMUL1	FM1/17-21	--	22	23
S.D F7,0(R8)	10	#5/ST1	A1/23-23	--	--	23