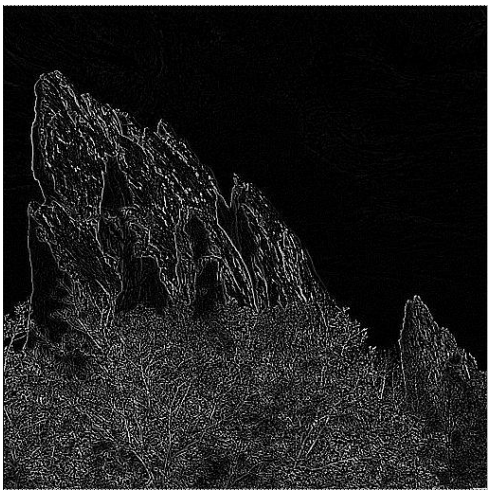
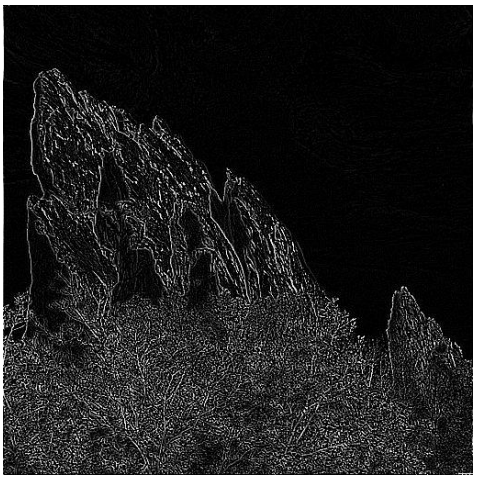
ECE 1195 Lab 6

Software Convolution Image:

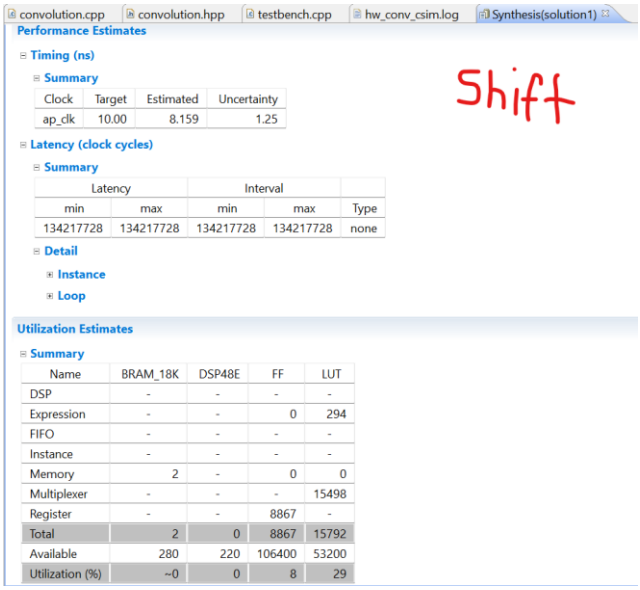


Hardware Convolution Image:



Utilization and Timing reports of HW Convolution:

Shift Register Implementation:



convolution.cpp | convolution.hpp | testbench.cpp | hw_conv_csim.log | Synthesis(solution1)

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.159	1.25

Shift

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
134217728	134217728	134217728	134217728	none

Detail

Instance

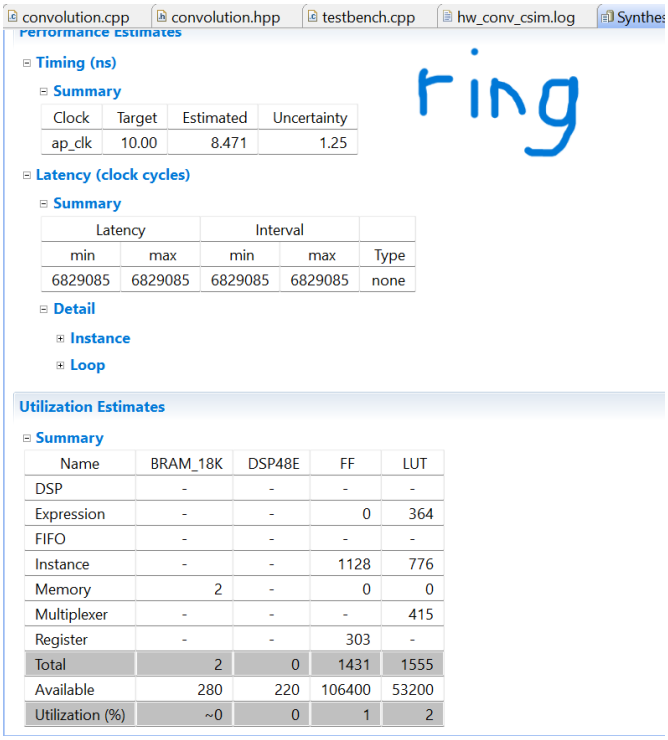
Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	294
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	2	-	0	0
Multiplexer	-	-	-	15498
Register	-	-	8867	-
Total	2	0	8867	15792
Available	280	220	106400	53200
Utilization (%)	~0	0	8	29

Ring Buffer Implementation:



convolution.cpp | convolution.hpp | testbench.cpp | hw_conv_csim.log | Synthes

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.471	1.25

ring

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
6829085	6829085	6829085	6829085	none

Detail

Instance

Loop

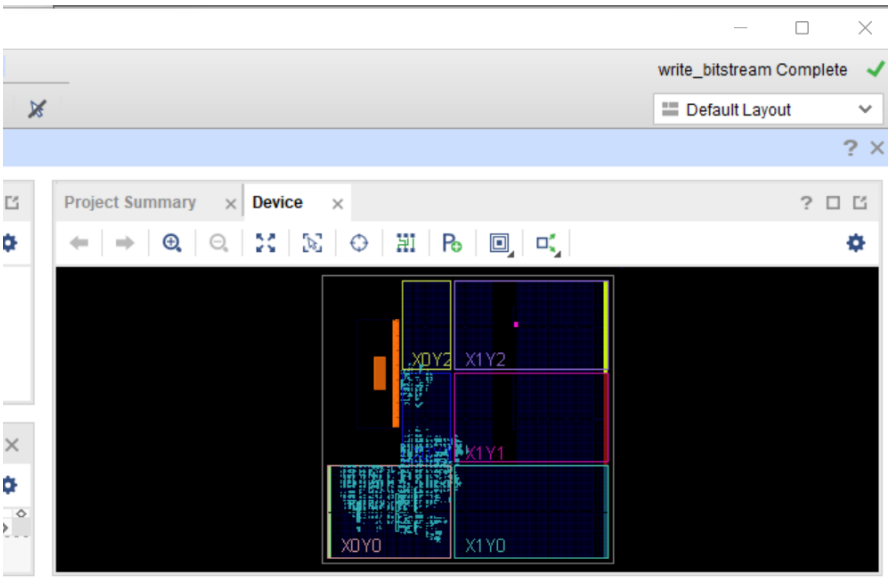
Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	364
FIFO	-	-	-	-
Instance	-	-	1128	776
Memory	2	-	0	0
Multiplexer	-	-	-	415
Register	-	-	303	-
Total	2	0	1431	1555
Available	280	220	106400	53200
Utilization (%)	~0	0	1	2

The Ring Buffer Implementation took about half as many clock cycles as the shift register implementation and took just a bit more time, with less utilization.

Successful Bitstream Generation:

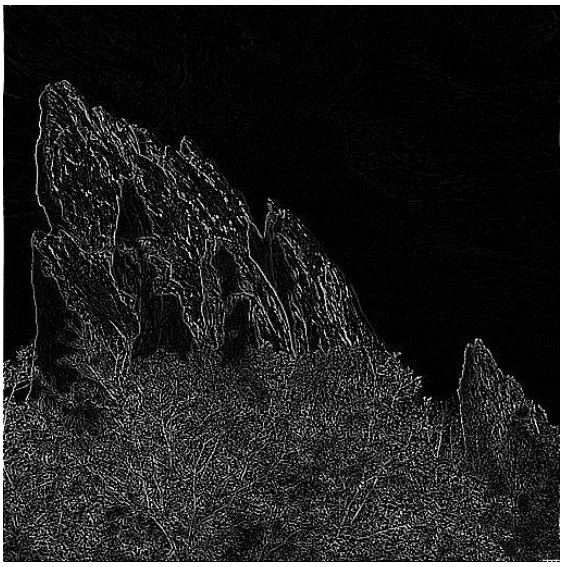


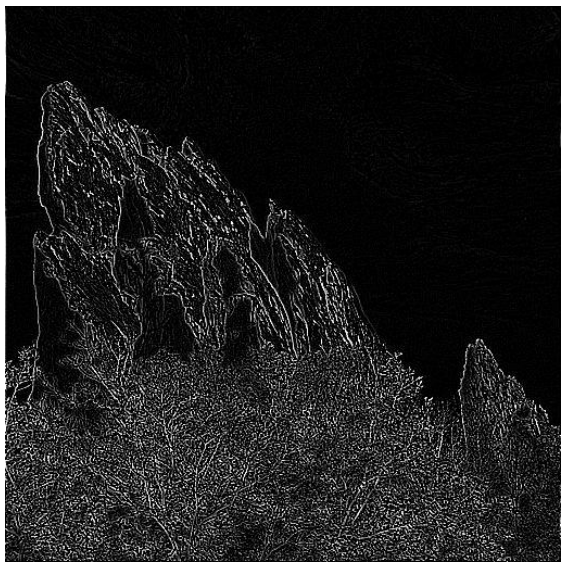
Putty Output:

```
Starting Dropbear SSH server: random: dropbearkey: uninitialized urandom read (3
2 bytes read)
random: dropbearkey: uninitialized urandom read (32 bytes read)
Generating 2048 bit rsa key, this may take a while...
haveged: haveged: ver: 1.9.4; arch: generic; vend: ; build: (gcc 8.2.0 CTV); col
lect: 128K

haveged: haveged: cpu: (VC); data: 16K (D); inst: 16K (D); idx: 12/40; sz: 15012
/57848

haveged: haveged: tot tests(BA8): A:1/1 B:1/1 continuous tests(B):  last entropy
 estimate 7.99676

haveged: haveged: fills: 0, generated: 0

random: crng init done
Public key portion is:
ssh-rsa AAAAB3NzaC1yc2EAAAADAQABAAABAQCzk0zhT7qyFAfpe13GYZKKFiy9deV3HV9mUvv44
MRRPRcgagigYh3eBLQOaKYD30gU7RmMyEoWm7r4wAvn3Ct+L1aNuoA2FHD95BEFDr/FswUDJnh9tu
mPVZSSVCY0ved58pwm9GyBjXfrPS2O/nq43XDj4aUgDXIQey4+5J5X11l6Iqde9mgVta2LFxgSuhE
KnNZCBlVjcSkavz593UkqjOQrj8AryMKoBT1rPI7sBvkJVtQUDLYe9qxG+Xn0/tC7d8mJjp2hJLW7
nNFmIzb3Y3dvQgDnHzaB0crtJcqglLKRaeGuHzQFzEjeePV/Iqnv7uYC4s6mjJoa6ubhas2B root
@zynqpeta
Fingerprint: sha1!! 2f:5a:42:b2:f6:f0:33:de:e5:5d:38:27:90:3d:c2:5c:d2:f2:34:
c4
dropbear.
hwclock: can't open '/dev/misc/rtc': No such file or directory
Starting internet superserver: inetd.
Starting syslogd/klogd: done
Starting tcf-agent: OK

root@zynqpeta:~# exit #DNE
logout

Last login: Sat Oct 24 03:22:35 UTC 2020 on tty1
root@zynqpeta:~# axidma 1 /dev/axidma0 ./rock512.pgm ./output_accel.pgm 512 5
12 1
time:  0.068339
root@zynqpeta:~# mount /dev/mmcblk0p1 /mnt
root@zynqpeta:~# cp output_accel.pgm /mnt/output_accel.pgm
root@zynqpeta:~# sync
root@zynqpeta:~# umount /mnt
root@zynqpeta:~#
```

As can be seen in the image, the convolution process took 0.0683 seconds.

Comparison of the HW_conv sim image (left) and accelerated image (right):





Reflection:

The software convolution simulation and hardware convolution simulation all provided identical images even though they were done in different ways. The efficiencies in terms of latency, runtime, and clock cycles vary between implementations of the Hardware Solutions. By being more creative and optimizing code, I could probably improve the run time and latency in the design, but both implementations are still reasonably fast. The accelerated hardware on the FPGA worked flawlessly in producing an identical image to the one the simulation provided.